

**OPERATING MANUAL FOR THE
L. J. ELECTRONICS
MODEL SA 1 ANALYSER**

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1. INTRODUCTION

The model 632 Logic Analyser has been designed to provide a high performance, low cost instrument, capable of trouble shooting synchronous logic systems. The analyser has sixteen data channels, two qualifiers and a clock input, which, coupled with its integral hexadecimal display, allows it to be used, 'free standing', in the analysis of microprocessor systems.

The unit also provides oscilloscope outputs, which are used to generate the familiar timing diagram. These can be used to view the data flows for pattern comparison, or to inspect binary data.

The design of this instrument is subject to continuous development and improvement, consequently this instrument may incorporate minor changes in detail from the information contained in this manual. This would, in the main, affect the components list and circuit diagrams.

2. INSTALLATION

2.1 Unpacking

The instrument should be inspected as soon as it is unpacked. If there is any damage notify the carrier immediately.

2.2 Power Connection

When shipped from the factory the unit is ready to operate from 210V - 255V, 50 - 60Hz supply. This is connected to the instrument via a 2 metre detachable three core P.V.C. sheath cable, permanently moulded to a fully shrouded three pin socket. It is fitted at the rear of the instrument and should be pushed home into the mains receptacle.

The supply lead should be connected to a three pin plug (fused at 1 amp) ensuring that the instrument is earthed via the green/yellow earth wire. The instrument is protected by a 160mA slow blow fuse located on the rear panel. (300mA in 120V versions).

2.3 Alteration for 120V

For operation on supplies in the range 110V - 130V, 50 - 60Hz, it is necessary to alter the connections to the primary windings of the mains transformer as shown below, and change fuse to a 300mA slow blow type. This is available only on those models supplied with a dual primary winding on the transformer.

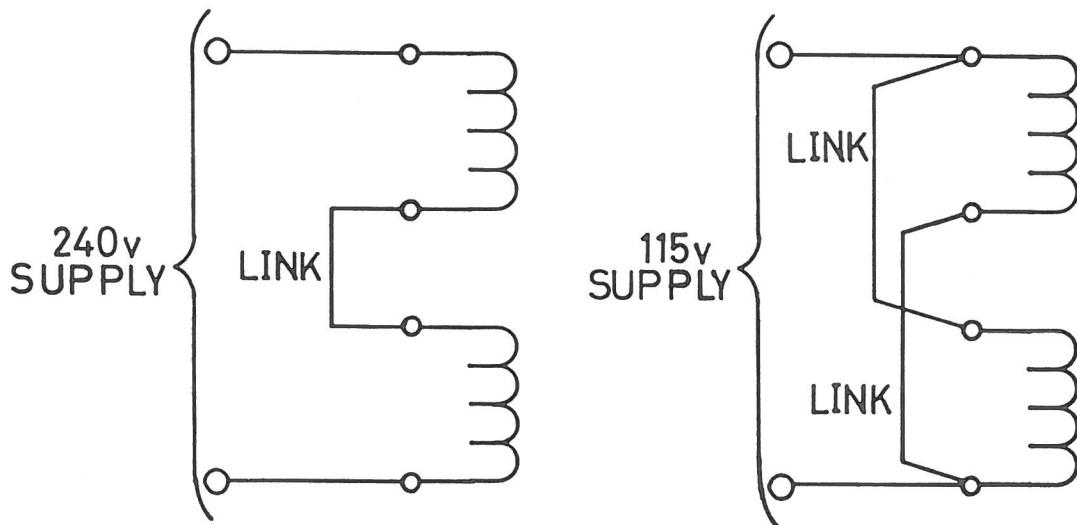


Fig 2.1 Mains Transformer Connection

3. SPECIFICATIONS

3.1 Clock, Data and Qualifier Inputs

Number: 16 data inputs, 2 qualifier inputs, 1 clock input.

Input threshold: TTL fixed at approximately 1.4V.

Maximum input: $\pm 10V$.

Logic level 1: between +2.0V and +5.5V.

Logic level 0: between -0.5V and +0.6V.

Minimum Clock pulse width: 40ns

Minimum data set up time: 35ns

Minimum data hold time: 0ns

Input impedance: 1 LSTTL load ($<400\mu A$ source $<10\text{pf}$)

3.2 Clock

Source: external up to 4MHz. Positive or negative active edge selectable.

Qualifier: selectable 1 - X - 0.

No clock indication: front panel LED will flash if armed when no clock is present.

3.3 Trigger

Source: word recognition with qualifier.

Word recogniser: 4 digits of hexadecimal thumbwheels, each digit with separate enable/disable switch.

Qualifier: selectable 1 - X - 0.

Delay: data recorded is 64 words pre-trigger and 63 words post trigger.

Output: rear panel TTL level which goes to a logic 0 whenever the input data agrees with the selected trigger condition.

3.4 Memory

Size: 16 x 128 bits

3.5 Display

Data: 4 hexadecimal digits displaying data in hexadecimal code at the memory position indicated by the cursor display.

Cursor: three digit display identifying the position of the data word in relation to the trigger word (at +00). Variable -64 to +63 using front panel INC/DEC switch.

3.6 Display Outputs

Display trigger: nominal +5V to zero pulse, $0.5\mu s$ wide at 1.2ms interval to trigger oscilloscope.
LSB: 8 channels, each 100mV amplitude at 300mV interval, staircase ramp. Data corresponds to input data lines D0 - D7.

MSB/LSB: 8 channels each 100mV amplitude at 300mV interval, staircase ramp. Data is selectable by front panel switch between LSB (D0 - D7) and MSB (D8 - D15).

Trigger marker: marker on LSB and MSB/LSB outputs which identifies the trigger position, at cursor location 00.

Cursor marker: flashing marker on LSB and MSB/LSB outputs identifies the cursor position as shown by the front panel display.

3.7 Miscellaneous

Operating temperature: 0 - 40°C

Power: 20VA, 105 - 125, 210 - 255V, 50 - 60Hz.

Size: height 100mm (4.0")

width 255mm (10.0")

depth 323mm (12.75") including carrying handle.

Weight: approx. 1.8Kg (4.0lbs)

3.8 Accessories Supplied

1 x data input cable.
1 x mains lead.
1 x user manual.

3.9 Options

High impedance data pod.
Fast memory, 12MHz.
IEEE 488 Bus pod.

3.10 Warranty

The logic analyser is warranted against defect in materials and workmanship for one year, from date of delivery.

4. METHOD OF OPERATION

4.1 Basic Operation

Logic analysers are designed to record a series of logic levels at several points. These points are called channels. The data are not continuously recorded, but are sampled and stored in memory under control of the clock input. The sample period is defined as the data set up time (the time the data must be stable prior to the clock edge) plus the data hold time (the time that the data must remain stable after the clock edge). Because user systems vary, the analyser allows the active clock edge to be selected as either the positive or negative going edge of the incoming waveform. In practice the sample period is short (35ns) compared to the minimum time between clock edges (250ns at 4MHz). In some applications not all clock edges are required to store data, and by using the clock qualifer signal, the unwanted clock edges can be prevented from storing data in the analyser.

To enable users to monitor particular data areas, an event selection feature is provided. When the analyser is ARMED data is continuously fed into the machine and compared to the selected event. This monitoring state will exist until the trigger event is identified, when this happens the ARM lamp is extinguished, and a further 63 events are clocked into memory. As the memory is 128 words long, the final record consists of 64 words prior to the trigger, the trigger event, and 63 words after the trigger. To give the trigger selection more flexibility a trigger qualifer is also available. Only when both the event selection switches agree with the incoming data, and when the trigger qualifer switch agrees with the data on the qualifer line will a trigger event be said to have occurred.

4.2 Data Inputs

The rear panel data input connector will accept the data input cable assembly (Zicon part no. 40022/40025) or the 603 Data Probe. The simple data input cable has to be short as it carries TTL signals, and the Analyser input loading is 1 LS-TTL gate. The 603 data probe is a single pod containing all 16 data lines, clock, qualifiers and ground. Inside the pod is an active buffer circuit for each input with an input impedance of 1 Megohm, 10pF. The input threshold is fixed at 1.4V (TTL) and the inputs are fully protected to $\pm 50V$. The 603 data probe thus enables the 632 to be used with several different logic families at one time including CMOS supplied off any voltage.

If required, the user can assemble their own input cable. The pin connections for the 632 and 603 are listed in section 5.7 and 5.8 respectively.

4.3 Arm/Abort Control

Depressing the ARM control initiates a data recording sequence to capture a new set of data. While recording is in progress the displays are blanked, the ARM LED is illuminated, and data is stored in memory using the external clock. This state remains unchanged until the trigger event is encountered, when the ARM LED will be extinguished. Sixty three clock cycles later the recording mode will be terminated. Alternatively if the trigger event does not occur, the ABORT control can be operated, this will immediately terminate the recording mode, which returns the analyser to the display mode.

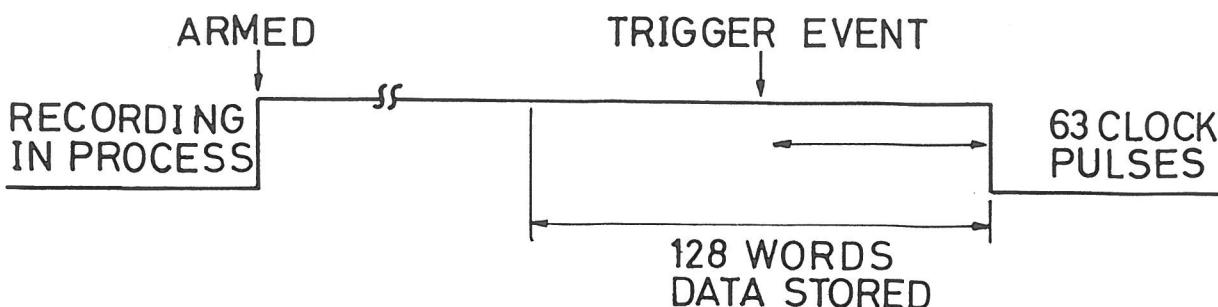


Fig 4.1 Recording Sequence

4.4 Trigger and Trigger Qualifier Controls

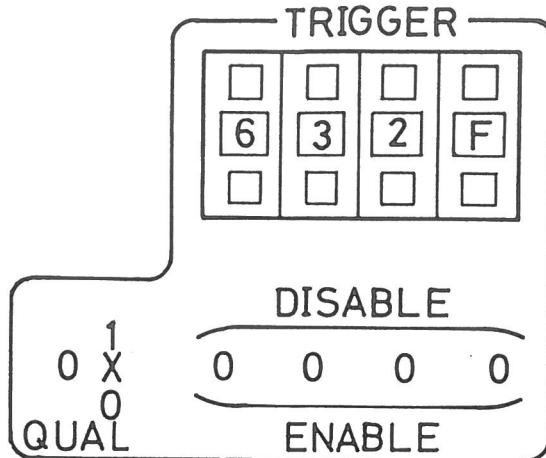


Fig 4.2 Trigger Controls

These controls are used to select the particular event that will cause the analyser to trigger and therefore define the section of input data which is stored in memory.

The trigger event is set by the 4 thumbwheel switches and the single line trigger qualifier switch. Each digit can be set in hexadecimal code (0 - F) and enabled or disabled depending upon the required trigger condition.

The trigger qualifier can be used as a 17th bit extension of the trigger word, as a bit mask on one of the trigger digits, or as an external trigger input by completely disabling the 4 digit trigger.

The data stored in memory contains 64 words of pre-trigger data and 63 words of post-trigger data.

4.5 Clock and Clock Qualifier Controls

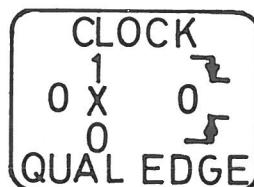


Fig 4.3 Clock Controls

The 632 requires a clock to strobe data into the memory. It accepts an external clock at rates from DC to 4MHz with an active edge selectable between \overline{L} and \overline{F} . If the active edge of the users system clock is \overline{L} then the analyser should be run on \overline{F} so that the system data is stable and meets the required set-up and hold times of the instrument. The ANDed clock qualifier enables data to be selectively recorded during valid memory addresses or during read or write operations in microprocessor circuits.

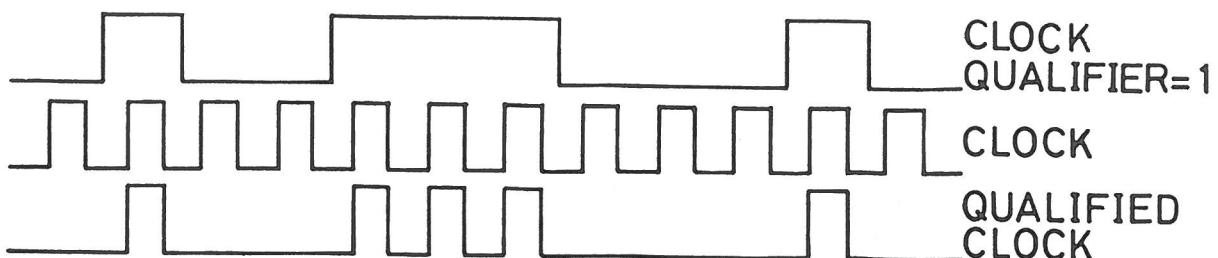


Fig 4.4 Qualified Clock Generation

Should recording be attempted when there is no clock signal present, or when the clock is present but not qualified, then an LED in the cursor window will flash.

4.6 Data Display

The 632 has two separate yet complementary display media: the 4 digit display with hexadeciml readout; and a timing diagram output for display on an oscilloscope.

The hexadecimal data display shows one word at a time with its position in memory, relative to the trigger word, indicated by the two digit cursor display. This has a range of -64 to +63. The INC/DEC switch is used to examine the data one word at a time.

To view the data in timing format an oscilloscope is required. Connect up the oscilloscope as in section 4.7. The timing diagram displays the whole of the memory contents (16 x 128 bits) with the trigger event identified in the centre of the display. The hexadecimal data word displayed on the front panel is indicated on the timing display by a flashing cursor marker.

4.7 Connection to an Oscilloscope

- a) Connect the display trigger output to the external trigger input of the oscilloscope. Select the external trigger function.
- b) Set the internal time base to $100\mu\text{s}/\text{div}$ and the trigger mode to D.C. coupled.
- c) Connect the display output (MSB/LSB) to the vertical amplifier input (Y) of the oscilloscope.
- d) Select 0.5 volts/div, D.C. coupled on the vertical amplifier.
- e) Centralize the trace on the screen.
- f) Use the INC/DEC switch to position the cursor at +63, then using the display output frequency adjust, (located on the rear panel) position the flashing cursor at the extreme right hand side of the display.
- g) If it is required to display all 16 channels of data, connect the display output LSB, to the second vertical amplifier input (Y) of the oscilloscope. Set the gain to 1V/DIV on both amplifiers, select chopped trace and re-position the displays using the Y offset adjusts.

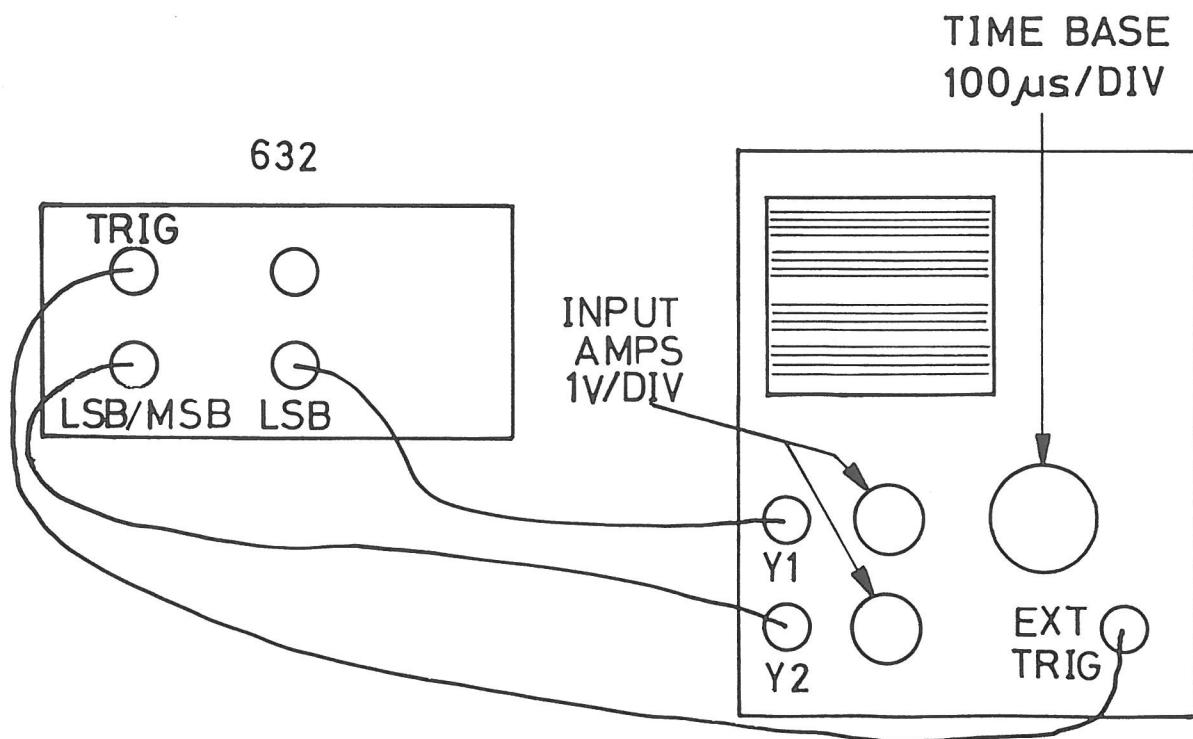


Fig 4.5 Oscilloscope Connection

5.7 Rear Panel Input Socket Connections

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	+5V	2	+5V
3	TRIGGER QUALIFIER	4	GND
5	MSB 7	6	GND
7	MSB 6	8	GND
9	MSB 5	10	GND
11	MSB 4	12	GND
13	MSB 3	14	GND
15	MSB 2	16	GND
17	MSB 1	18	GND
19	MSB 0	20	GND
21	CLOCK QUALIFIER	22	GND
23	CLOCK	24	GND
25	LSB 7	26	GND
27	LSB 6	28	GND
29	LSB 5	30	GND
31	LSB 4	32	GND
33	LSB 3	34	GND
35	LSB 2	36	GND
37	LSB 1	38	GND
39	LSB 0	40	GND

Note: The 5V connections are an internal function, and should not be used as a supply.

Pin 1 and Pin 40 are marked on the connector, next to the pins themselves. (Pin 1 is in the upper right hand corner when viewed from the rear).

Suitable input connector 3M part No. 3417 6040.

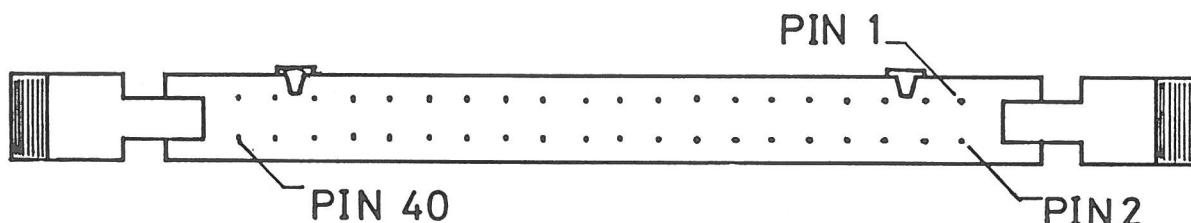


Fig 5.1 Rear Panel Connector

5.8 High Impedance Pod Connections

The 40 way cable from the pod is designed to be totally compatible with the rear socket on the analyser. A socket is terminated on the cable and may be plugged directly into the rear of the instruments.

The input to the pod is accomplished by a 26 way socket (3M type 3399-6000 and 3448-3026 retaining clip). The connections for this socket are shown below and on the pod itself:-

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	GND	8	TRIG QUAL
9	CLOCK QUAL	10	CLOCK
11	D15 (MSB 7)	12	D14 (MSB 6)
13	D13 (MSB 5)	14	D12 (MSB 4)
15	D11 (MSB 3)	16	D10 (MSB 2)
17	D9 (MSB 1)	18	D8 (MSB 0)
19	D7 (LSB 7)	20	D6 (LSB 6)
21	D5 (LSB 5)	22	D4 (LSB 4)
23	D3 (LSB 3)	24	D2 (LSB 2)
25	D1 (LSB 1)	26	D0 (LSB 0)

5.9 IEEE 488 Pod Connections

The 40 way ribbon cable from the pod is designed to be totally compatible with the rear socket on the analyser. A socket is terminated on the cable and may be plugged directly into the rear of the analyser.

The input to the pod is in two forms, firstly an independent uncommitted input. This is a ten way Molex type (mating connector RS No. 467-633), the connections are shown on the pod label itself. The other input is a 24 way connector fully compatible with the IEEE 488 standard.

CONNECTOR PIN NO.	FUNCTION
1	DIO 1
2	DIO 2
3	DIO 3
4	DIO 4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD
13	DIO 5
14	DIO 6
15	DIO 7
16	DIO 8
17	REN
18	GND (6)
19	GND (7)
20	GND (2)
21	GND (9)
22	GND (10)
23	GND (11)
24	GND, LOGIC

5.10 Miniature Clip Identification

The analysers are supplied with cables that have colour coded clips, which are used to identify the different functions.

Red – Data inputs (16 channels)

Yellow – Clock

Green – Clock Qualifier

Blue – Trigger Qualifier

Black – Grounds:— It is necessary for the proper functioning of the instrument that all ground probes be connected.

6. OPTIONS

6.1 High Impedance Pod

6.1.1 Introduction

The high impedance pod is designed to be used in applications where the users circuitry is susceptible to the normal LSTTL loading of the analyser. The pod presents a higher impedance to the user, thereby reducing significantly the loading on the circuitry under test, and also has a much higher input protection rating.

6.1.2 Connections

Inputs to the pod are made by means of a 26 way ribbon cable connector, and are detailed in section 5.8. The pod is connected directly to the rear socket of the analyser as detailed in section 5.7.

6.1.3 Specifications

The specifications of the data pod are the same as section 3.1 except for the following:

Maximum input: $\pm 50V$

Input Impedance: 1 Megohm, 10pF

6.2 IEEE 488 Bus Pod

6.2.1 Introduction

This option allows the IEEE 488 Bus to be directly connected to the 632 analyser, and its coded data transactions to be directly interpreted by the analyser.

6.2.2 Inputs

The probe has two sets of inputs; a 24 way ribbon cable, with a 24 way IEEE 488 compatible connector; a 10 way cable assembly for user defined connections (detachable from probe).

6.2.3 Outputs

A 40 way ribbon cable terminated with a 40 way socket, the connections are compatible with the 40 way data input socket of the 632.

6.2.4 Specifications

6.2.4.1 Input

Number: Defined 24 way connector, plus 9 user defined inputs (8 data, 1 clock).

Input load: 2 LSTTL gates

Input Threshold: TTL fixed at approximately 1.5V with 800mV hysteresis for noise rejection.

Maximum Input: $\pm 10V$

Minimum clock pulse width: 40ns

Minimum data set up time: 35ns

Minimum data hold time: 0ns

Maximum clock frequency: 4MHz

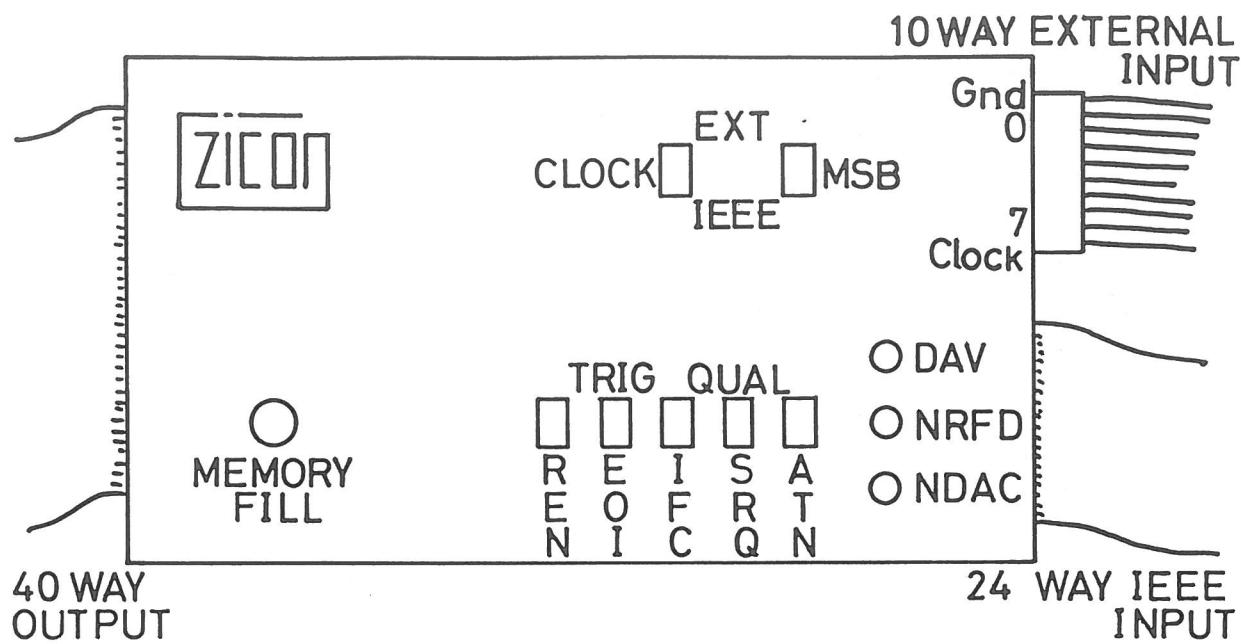


Fig 6.1 IEEE 488 Pod Front Panel

6.2.4.2 Controls

Clock: Selectable between External and IEEE 488 Bus (DAV). The edge of which is selected on the 632 front panel.

MSB Data: Selects whether the user data or the IEEE 488 management lines are recorded in the MSB of memory.

Trigger Qualifier Select: This group of slide switches selects one of five management lines as the trigger qualifier. If more than one is selected then the top one in a priority order is taken (ATN, SRQ, IFC, EOI, REN), ATN having top priority. The required level is set using the front panel qualifer switch.

Memory Fill: The momentary action button connects a 200KHz oscillator to the clock line, and is used to fill the memory if bus transactions have finished. For short data transactions, there may not be enough DAV transitions to finish recording (63 bytes after trigger). The operating sequence in this case is as follows.

Firstly set the trigger word, and clock mode settings on the front panel. Then fill the memory with the quiescent state by depressing the memory fill button. Then initiate the data transaction sequence and wait for the unit to be triggered. Finally once the unit is triggered, but the recording has not finished, fill the remainder of memory again using the memory fill button.

The analyser will then have captured a burst of transactions (synchronously recorded) with the quiescent conditions shown before and after the active data period.

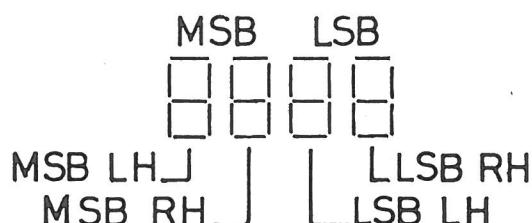
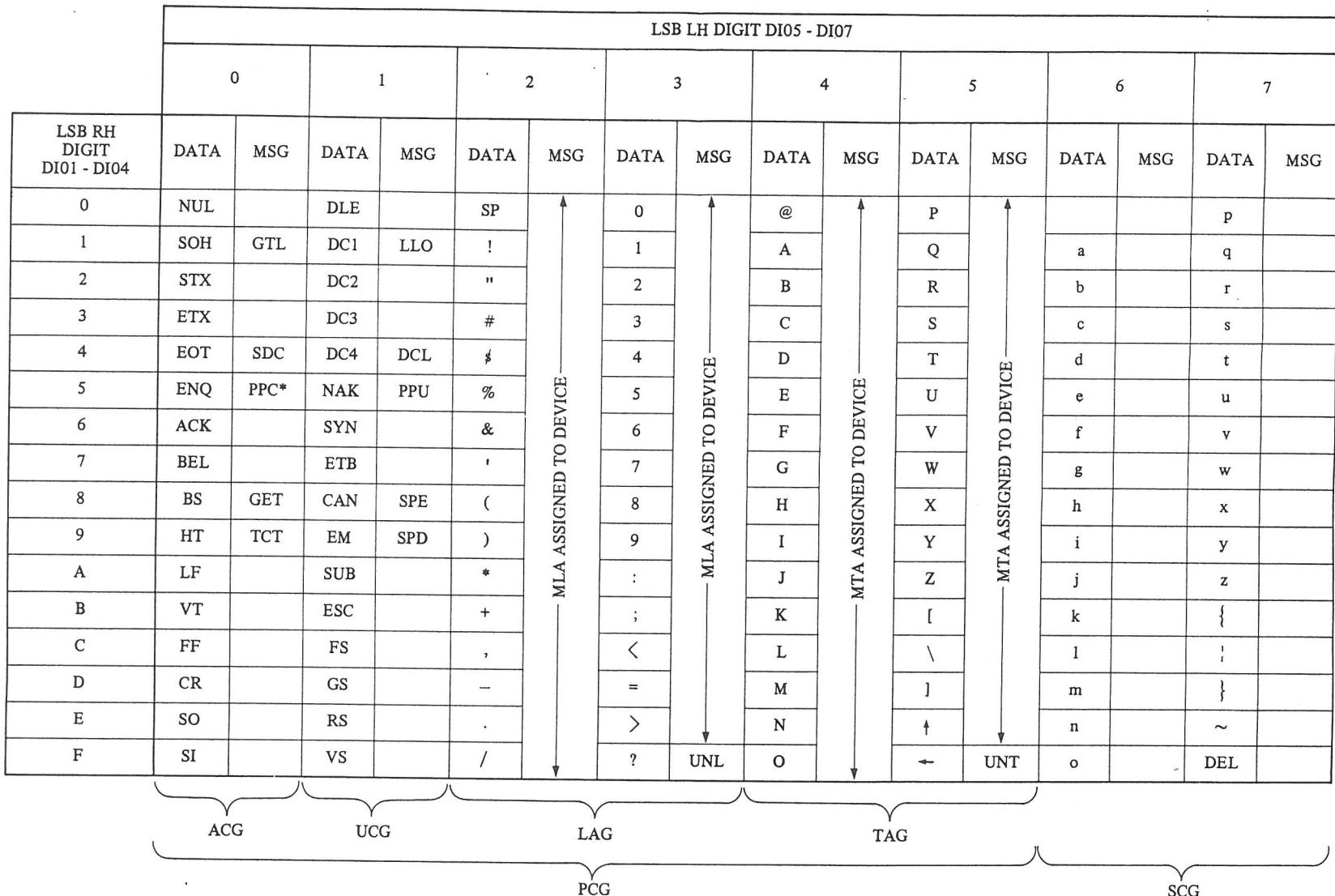


Fig 6.2 Data Display

Fig 6.3 Multiline Interface Messages



MSG – Interface message, sent with ATN true

*--- PPC requires a secondary command

MLA – My Listen Address sent, eg. ‘C’ sent with ATN true forces device 8 to listen

MTA – My Talk Address sent, eg. ‘[’ sent with ATN true forces device 27 to become talker when ATN goes false

PCG – Primary Command Group

SCG – Secondary Command Group, the meaning of the MSG in this group is defined by the PCG

ACG – Addressed Command Group

UCG – Universal Command Group

LAG – Listen Address Group

TAG – Talk Address Group

HEX DIGIT	MSB L.H. DIGIT TRUE STATES	HEX DIGIT	MSB R.H. DIGIT TRUE STATES
0	NONE	0	NONE
1	DAV (1)	1	SRQ
2	NRFD	2	REN
3	NRFD, DAV (2)	3	REN, SRQ
4	NDAC (3)	4	EOI
5	NDAC, DAV	5	EOI, SRQ
6	NDAC, NRFD	6	EOI, REN
7	NDAC, NRFD, DAV	7	EOI, REN, SRQ
8	IFC	8	ATN
9	IFC, DAV (1)	9	ATN, SRQ
A	IFC, NRFD	A	ATN, REN
B	IFC, NRFD, DAV (2)	B	ATN, REN, SRQ
C	IFC, NDAC (3)	C	ATN, EOI
D	IFC, NDAC, DAV	D	ATN, EOI, SRQ
E	IFC, NDAC, NRFD	E	ATN, EOI, REN
F	IFC, NDAC, NRFD, DAV	F	ATN, EOI, REN, SRQ

- Notes:
- 1 This is an invalid condition for normal handshake operation using any clock source.
 - 2 These are valid conditions for negative clock edges when clocked from DAV (IEEE clock).
 - 3 These are valid conditions for positive clock edges when clocked from DAV (IEEE clock).

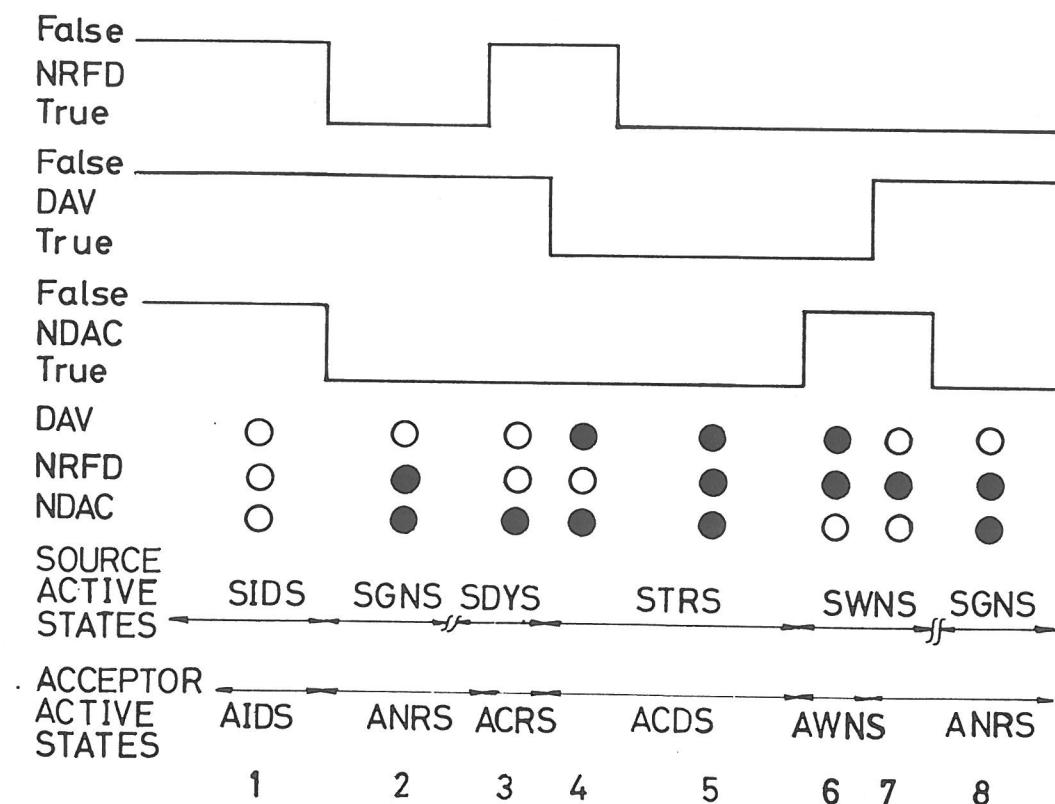


Fig 6.4 Handshake and LED States

Handshake Sequence:

- 1 Handshake is in idle state, waiting for controller to initiate a data transfer.
- 2 One or more of the acceptors is not ready for data, and is holding NRFD TRUE.
- 3 The source has not yet set DAV TRUE, a new byte of data is not available.
- 4 All of the acceptors have not seen the transition of DAV, and have yet to set NRFD TRUE.
- 5 One or more of the acceptors has not yet accepted the data, and has not allowed NDAC to go false.
- 6 The source has not set DAV false in response to NDAC going false.
- 7 The acceptors have not set NDAC true in response to DAV going false.

6.3 12 MHz Memory

This is a factory fitted option which allows data to be clocked into memory at clock frequencies of 12MHz. This option is for use when the analyser is being used with discrete logic, or with a fast microprocessor.

6.3.1 Specification

Minimum clock pulse width: 40ns
Minimum data set up time: 35ns
Minimum data hold time: 0ns
Maximum clock frequency: 12MHz
Memory size: 16 x 128 bits

7. TECHNICAL DESCRIPTION

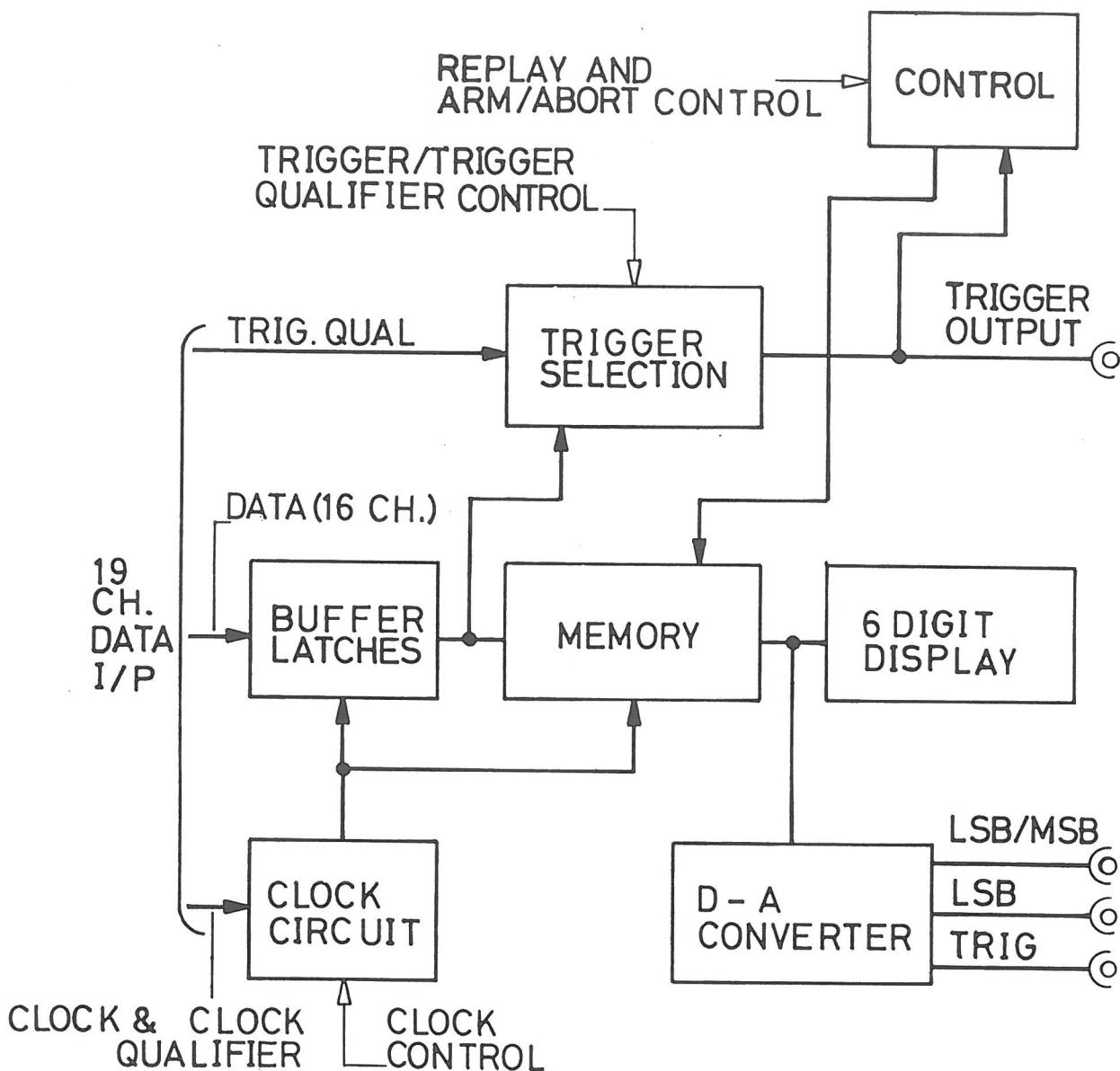


Fig 7.1 Simplified Block Diagram

7.1 Buffer Latches

This part of the circuit consists of all of the data inputs up to U15 - U18. It is provided to synchronise the data inputs and to provide fast set-up and hold times. The 270Ω input resistors (R15 - R18, R21 - R32) are used to give some protection to the logic analyser. The $1M\Omega$ pull up resistors (R9 - R12, R34 - R44) bias unconnected inputs to the high state. The two input LS14 gates are used to buffer incoming data and to provide some hysteresis. Because they are inverting gates the overall delay from input to the LS163 (U15 - U18) is the same for both edges. The capacitor between the gates (C41 - C56) is used to delay the data signal such that the set up and hold times of the latch are adhered to.

The latches take the data and transfer it to the output when a clock edge occurs. This causes the data at the input of the trigger comparator (U21 U23 U24 U26) to change coincidentally, therefore not generating spurious trigger events.

The latches are isolated from memory by the tri-state gates (U30 - U33). This allows the trigger comparator to be free running, generating valid outputs on the 'TRIGGER OUTPUT' connector even when the unit is not ARMed.

7.2 Clock Circuitry

This is used to generate a clock pulse which is then used to transfer data from block to block inside the analyser.

The input circuit for the clock and clock qualifier is similar to that of the data paths, except that there is no trimming capacitor and the second LS14 is replaced by an exclusive OR gate (U6/11 - 13). For the clock lines the other input to this gate is connected to switch S9, the edge selection switch. Depending upon the state of this switch the output of the LS86 (U6/11) is either inverted, or not inverted. This is then used to clock a 7474 latch (U11). For the clock qualifier line the other input is connected to switch S8, the level selection switch. This controls the polarity of output U6/8 which is taken to the data input of the latch via a second pole on S8. The Q output of the latch (U11/9) can only go high when the D input (U11/12) is high and a positive transition occurs on the clock input (U11/11). Thus a 'qualified clock' is generated only when the selected qualifier level is present during the selected clock edge.

When the Q output (U11/9) goes high, the \bar{Q} output (U11/8) goes simultaneously low. This causes the latch to be reset after about 80ns. C12 is used to control the length of the output pulse. U6/1 - 3 buffers the reset pulse.

7.3 Trigger Event Selection

This circuitry is used to select a particular event from a stream of events that takes place upon the 16 data lines and the trigger qualifier line. When this event occurs the 'trigger bus' line goes high. As the 'trigger bus' is a common collector 'wired OR' line, it can only go high when all the outputs connected to it go high. These are the result of the trigger qualifier comparator (U21, U23, U24, U26); and the output of U10/8. The last part is driven from the ARM signal and makes sure that the trigger bus has a low to high transition (to clock U3/3 which is edge active) should the other contributors already be high.

The trigger qualifier comparator consists of switch S2 and an exclusive OR gate (U10/11 - 13). The first pole of S2 and the logic gate controls the polarity of the qualifier signal, while the second pole of S2 releases the 'trigger bus' in the don't-care position.

The data qualifier is divided into four separate parts, each consists of a 16 position thumbwheel switch, an ENABLE/DISABLE switch (S3 - S6) and four exclusive OR gates (U21, U23, U24, U26). The exclusive-OR gates compare the incoming data to the thumbwheel setting, the result then contributes to the trigger bus through the ENABLE/DISABLE switch.

The trigger bus drives the latch U3/3, which resets the ARM mode, and allows the record mode to end 63 clock cycles later.

7.4 Memory and Address Counter

The memory in a logic analyser serves two functions – firstly to record data from the user under his control at varying speeds, secondly to output this data to a display device under cursor control. These two functions are reflected in the block diagram, where the memory is shown to have separate input and output functions. The circuit diagrams show the memories to be static RAM's organised as 128 x 8 and connected in parallel. The separate functions are achieved by using tri-state gates to isolate the input from the memory, and latched function to isolate the output.

As soon as the unit enters the record mode the displays are blanked and the display trigger is turned off. The 'qualified clock' is connected to the control circuitry by U20/11 - 13. The rising edge of the output U20/11 advances the address counter (U38, U46) and triggers the write monostable which generates a write pulse. This pulse enables the isolating gates U30 - U33 (which places the incoming data at the memory inputs) and drives the read/write input of the memories themselves.

In the replay mode the memory is continuously outputting data, and the address counter is clocked from the 'internal clock' via U20/8 - 10.

7.5 Control Circuitry

This circuitry is used to direct the flow of data during both record and replay modes. The mode is controlled by the outputs U5/5, U5/6. The record mode is set by action of the ARM control, replay mode is either automatically restored, or restored by action of the ABORT control. Other parts of the control circuitry are; the cycle counter, the cursor position control; the cursor display counter.

7.5.1 Cycle Counter (U34, U42)

This counter is an eight bit binary counter that controls the flow of data to the A-D converter, and also synchronises the flyback period and generates the display control signals.

When in the record mode the counter is forced to count state 64 by action of the ARM line on the load inputs (U34, U42/9). This is released when a trigger event occurs and the count continues to count state 128, when U27/10 goes low. This stops the memory address counter from advancing and restores the replay mode by resetting U3/13.

In the replay mode the counter counts from state 0 to 192, and then repeats. States 0 to 127 are used to output data, states 128 to 192 are used as the flyback period. At count state 64 the UP/DOWN input of the cursor counter changes state, causing it to count up. The same signal is used to generate the trigger position marker in the A-D circuitry.

When count 128 is reached output U27/10 goes low this stops the memory address counter and advances the staircase generator U55.

When count 192 is reached U28/6 goes low, causing a synchronous reset of the cycle counter, preloading the cursor counter to 64, and generating an output trigger pulse. These events are synchronised to the next clock edge.

7.5.2 Cursor Position Control (U35, U36, U43, U44)

This circuitry is to enable the display to show the desired data word. It does this by comparing a cursor counter (U36, U43) with the cycle counter. The comparator consists of eight open collector exclusive OR gates (U35, U43) with their outputs connected together. The output will only go true, when all the cycle counter outputs are the inverse of the cursor counter outputs. When this happens, U53/11 will generate a strobe pulse which will enter the desired data from the memory into the displays. This output also generates the cursor marker on the oscilloscope waveforms. U43/9 is taken high to prevent strobe pulses occurring during the fly-back period.

7.5.3 Cursor Display Counter (U57 U45)

This is a simple decimal counter that counts in synchronism with the cycle counter. However instead of counting in binary, from 0 to 192, it does so in decimal from 64 down to 0 and then up to 63. This is accomplished by loading 64 when the cycle counter is reset, and changed from down, to up count when the cycle counter reaches 64. The outputs from this counter are latched into the cursor display (U57 and U58) by the same signal that latches the data into the data displays.

7.6 D-A Converter

The object of the D-A converter is to modify data stored in the memory so that it can be displayed on an oscilloscope. The converter consists of a staircase generator, two data multiplexers and two summing amplifiers.

The staircase generator (U55) is a twelve bit binary counter that is advanced after each completed cycle of the cycle counter. The lower three outputs Q1-3 are used to generate the eight levels required for the eight channels in the LSB and MSB outputs. They also drive the multiplexers (U47, U48) which select one data line from eight inputs, and via U51 and R77 R78 R80 generate the eight level staircase waveform. U51 is a summing amplifier, and also adds to the staircase the trigger position marker (via R79) and the cursor marker (via R82). The staircase waveform is then added to the selected data train, using two more summing amplifiers U49, U50. The data used by U49 can be selected by switch S1 between LSB and MSB. This is for oscilloscopes which can only display one output, but where both sets of data need to be examined.

TRIGGER WAVEFORM.

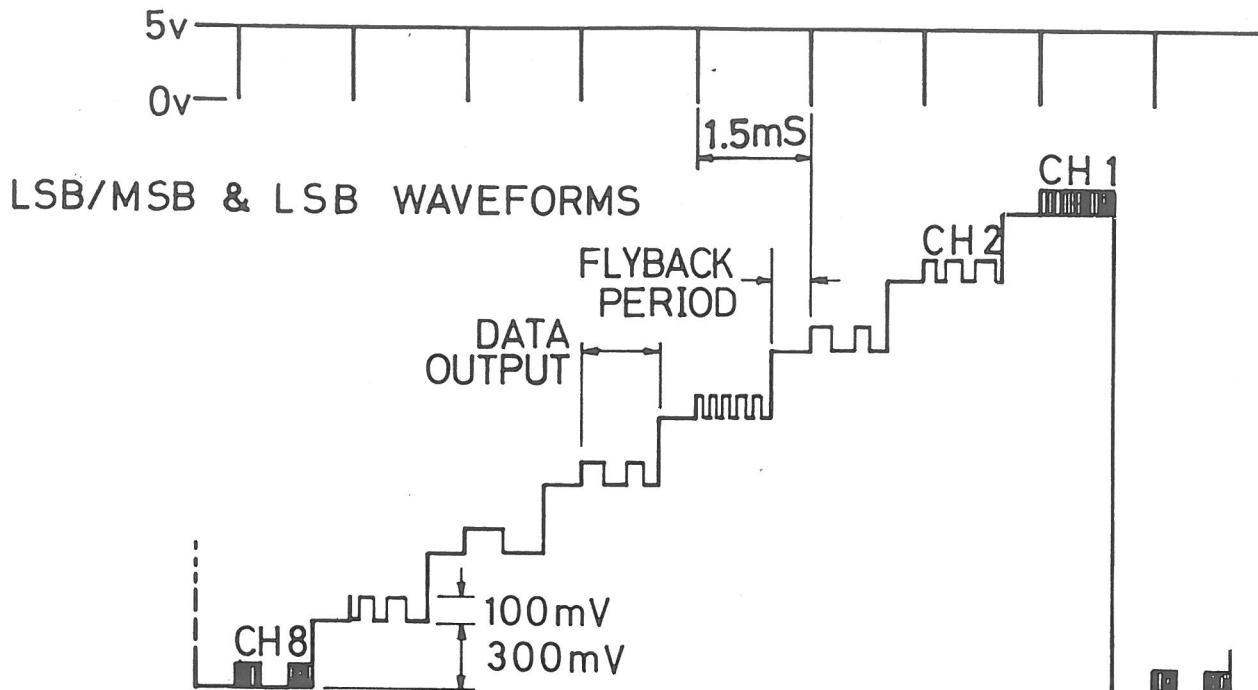


Fig 7.2 Output Display Waveforms

7.7 High Impedance Data Pod

The data probe consists of 19 identical data paths. These are used to present a high input impedance to the user's circuit. Each path consists essentially of two transistors arranged as emitter followers. This generates the high input impedance, with a voltage gain of 1 and an input/output offset of $<100\text{mV}$. This means that the AND gate (LS08) input is effectively connected to the user signal, without loading the user circuit. The output of the LS08 is used to transmit the signal (via a ribbon cable) to the rear input socket of the analyser proper.

To ensure a faithful buffering of the input signal when it is close to ground ($<600\text{mV}$) the transistors are referenced to -3.3V , ensuring that they always conduct.

The -3.3V is generated by two voltage mirror chips from the 5V supply.

7.8 The IEEE Pod

The object of this pod is to take data from the standard IEEE 488 data bus and store it in the logic analyser and then present it to the user in a convenient manner. On this data bus signals that are low, i.e. less than 0.6V , are considered to be logically true i.e. '1'. Therefore all IEEE lines are inverted inside the pod before being transmitted to the analyser, so that they can be displayed in the more convenient form of 'true' being logic '1'.

The data paths are divided into two halves with LSB being permanently connected via LS14's to the IEEE 488 D10 - D17 lines. The LS14's provide the required inversion and also present some hysteresis to the incoming signal. MSB can be connected to either the management lines of the IEEE 488 bus, or to the independent data inputs. This selection is accomplished by a dual set of tri-state gate and the front panel switch (MSB).

The clock qualifier is permanently connected to the ATN management line. This allows the user to capture either data transfers, or command transfers, if both are required then this function can be disabled on the analyser front panel.

The trigger qualifier can be selected to be either of five management lines. Although more than one of these can be selected simultaneously only the highest one in the following priority will actually be connected to the trigger qualifier (highest – ATN, SRQ, IFC, EOI, REN). This function is controlled, or disabled using the front panel trigger qualifier switch.

The clock is selected from one of three sources. The DAV line from the IEEE, or the external clock line from the independent data inputs. The memory fill button connects an internal clock source to the clock line, which overrides the other clocks.

APPENDIX 1

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
U1	24006	POSITIVE 5V REG.	MOTOROLA	MC7805CP	1
U2	24004	TIMER	FAIRCHILD	555TC	2
U3	20005	DIG. I.C.	FAIRCHILD	74LS74	2
U4	24004	TIMER	FAIRCHILD	555TC	
U5	20005	DIG. I.C.	FAIRCHILD	74LS74	
U6	20006	DIG. I.C.	FAIRCHILD	74LS86	1
U7-U9	20004	DIG. I.C.	FAIRCHILD	74LS14	6
U10	20011	DIG. I.C.	FAIRCHILD	74LS136	7
U11	20021	DIG. I.C.	FAIRCHILD	7474	1
U12-U14	20004	DIG. I.C.	FAIRCHILD	74LS14	
U15-U18	20012	DIG. I.C.	FAIRCHILD	74LS163	8
U19	23004	DIG. I.C.	FAIRCHILD	14069	1
U20	20010	DIG. I.C.	FAIRCHILD	74LS125	5
U21	20011	DIG. I.C.	FAIRCHILD	74LS136	
U22	02004	S.I.L. RESISTOR PACK 10K	BECKMAN	764-1-R10K	2
U23	20011	DIG. I.C.	BECKMAN	74LS136	
U24	20011	DIG. I.C.	BECKMAN	74LS136	
U25	02004	S.I.L. RESISTOR PACK 10K	BECKMAN	764-1-R10K	
U26	20011	DIG. I.C.	BECKMAN	74LS136	
U27	20014	DIG. I.C.	BECKMAN	74LS02	1
U28	20001	DIG. I.C.	BECKMAN	74LS00	1
U29	20009	DIG. I.C.	BECKMAN	74LS123	2
U30-U33	20010	DIG. I.C.	BECKMAN	74LS125	

NOTES:

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
U34	20012	DIG. I.C.		74LS163	
U35	20011	DIG. I.C.		74LS136	
U36	20015	DIG. I.C.		74LS193	2
U37	20016	DIG. I.C.		74LS190	2
U38	20012	DIG. I.C.		74LS163	
U39	25002	RAM 128x8	FAIRCHILD	68810	2
U40	25002	RAM 128x8	FAIRCHILD	68810	
U41	20009	DIG. I.C.		74LS123	
U42	20012	DIG. I.C.		74LS163	
U43	20011	DIG. I.C.		74LS136	
U44	20015	DIG. I.C.		74LS193	
U45	20016	DIG. I.C.		74LS190	
U46	20012	DIG. I.C.		74LS163	
U47	20017	DIG. I.C.		74LS151	2
U48	20017	DIG. I.C.		74LS151	
T1	26004	TRANSISTOR NPN		BC184C	1
D1	26001	DIODE		IN914	4
D2	26002	TRANSIENT PROTECTOR	GENERAL ELECTRIC	ICTE-5	1
D3-D6	26005	3R RECTIFIER DIODE		S401	4
D7	26001	DIODE		IN914	
D8	26001	DIODE		IN914	
D9	26001	DIODE		IN914	

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DESIGNATOR	PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No	No USED Per Assy
R1	00562	5K6 ±5% 1/4W	MULLARD	CR25	1
R2	00103	10K "	"	"	17
R3	01003	20K CERMET MULTITURN	SPECTROL	43P	1
R4-R6	00103	10K ±5% 1/4W	MULLARD	CR25	
R7-R13	00105	1M "	"	"	19
R14-R32	02001	270R "	NEOHM	RGP 0207	19
R33-R44	00105	1M "	MULLARD	CR25	
R45	00223	22K "	"	"	1
R46	00183	18K "	"	"	1
R47	00474	470K "	"	"	1
R48	00103	10K "	"	"	1
R49	00103	10K "	"	"	1
R50	00681	680R "	"	"	1
R51	00102	1K "	"	"	1
R52-R54	00103	10K "	"	"	1
R55	00332	3K3 "	"	"	1
R56-R58	00103	10K "	"	"	2
R59	00471	470R "	"	"	1
R60	00103	10K "	"	"	1
R61	00822	8K2 "	"	"	1
R62	00103	10K "	"	"	1
R63	00103	10K "	"	"	1
R64		NOT USED			

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R65	00103	10K $\pm 5\%$ $\frac{1}{4}$ W	HULLARD	CR25	
R66	00103	10K " "	"	"	
R67	00394	390K " "	"	"	
R68	00471	470R " "	"	"	2
R69	00394	390K " "	"	"	
R70	00222	2K2 " "	"	"	
R71	00151	150R " "	"	"	
R72	00181	180R " "	"	"	
C1	12002	4700 μ 16v ELECTROLYTIC	ITT	21108-0472	
C2	10104	10nF CERAMIC	HULLARD	629 06103	13
C3	11102	10 μ F 16v TANT	DUBILIER	100 880	4
C4	10104	10nF CERAMIC	HULLARD	629 06103	
C5	10222	220pF CERAMIC	"	632 58221	20
C6	11102	10 μ F 16v TANT	DUBILIER	100 880	
C7	10104	10nF CERAMIC	HULLARD	629 06103	
C8	11102	10 μ F 16v TANT	DUBILIER	100 880	
C9	10104	10nF CERAMIC	HULLARD	629 06103	
C10	11101	1 μ F 35v TANT	DUBILIER	100 900	1
C11	11102	10 μ F 16v TANT	"	100 880	
C12	10222	220pF CERAMIC	HULLARD	632 58221	
C13	10104	10nF CERAMIC	"	629 06103	

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C14	114-71	4.7μF/35V TANT	DUBILIER	100 807	1
C15-C17	10104	10nF CERAMIC	MULLARD	G29 OG103	1
C18	10103	1nF CERAMIC	"	G29 OZ102	1
C19	11220	0.22μF/35V TANT	DUBILIER	100 896	1
C20	10351	33pF CERAMIC	MULLARD	G32 34279	2
C21-C22	10104	10nF CERAMIC	"	G29 OG103	
C23-C24	10222	220pF CERAMIC	"	G32 58221	
C25	11221	2μ2F/35V TANT	DUBILIER	100 902	2
C26	10152	150pF CERAMIC	MULLARD	G32 34151	1
C27	11221	2μ2F/35V TANT	DUBILIER	100 902	
C28-C30	10104	10nF CERAMIC	MULLARD	G29 OG103	
C39	10681	68pF CERAMIC	"	G32 34689	1
C40	10351	33pF CERAMIC	"	G32 34279	
C41-C5G	10222	220pF CERAMIC	"	G32 58221	
J1	60022	40 WAY HEADER	3M	3417-6000	1
J2-J3	60005	5 WAY P.C.B. PLUG	MOLEX	A-4030-5A	3
J4-J5	60008	10 "	"	A-4030-10A	8
J6	60005	5 "	"	A-4030-5A	
J7	60006	7 "	"	A-4030-7A	1
J8	60008	10 "	"	A-4030-10A	

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
J9	60008	10 WAY PCB PLUG	MOLEX	A-4030-10A	
J9	"	" " " "	"	"	
J9	"	" " " "	"	"	
J9	"	" " " "	"	"	
J9	"	" " " "	"	"	
	60018	8 WAY I.C. SKT	ROBINSON NUGENT	ICY-083-S3T	2
	60002	14 "	"	ICY-143-S3T	25
	60003	16 "	"	ICY-163-S3T	16
	60024	24 "	"	ICY-246-S4T	2
TR1	30002	9V 2.2A TRANSFORMER	R.S.	207-122	1
	41015 REV B	PCB	S.P.C.	41015 REV B	1
	51001	H15 BLACK SLEEVE	R.S.	399-580	10
	60025	CONNECTOR PIN	R.S.	433-624	8
	62016	M2.5 x 10 SCREW P.H.			2
	62018	M2.5 NUT			2
	62018	M2.5 WASHER			2
	62009	M4x12 SCREW P.H.			2
	62011	M4 NUT			2
	62012	M4 WASHER			2
		22 AWG COPPER WIRE			
		7/0.2 mm WIRE			

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy.
U49-U51	24005	HOS/FET OP. AMP	NATIONAL	3140	3
U52	20014	DIG. I.C.		74LS02	1
U53	20001	DIG. I.C.		74LS00	1
U54	20002	DIG. I.C.		74LS04	1
U55	23003	DIG. I.C.		14040	1
U56	80005	±1 LED DISPLAY	R.S.	586-891	1
U57-U62	80004	HEXADECIMAL LED DISPLAY	TEXAS	TIL 311	6
D10	80006	L.E.D.	R.S.	586-475	1
R73	00562	5K6 ±5% 1/4W	MULLARD	CR25	3
R74	00224	220K "	"	"	2
R75	00562	5K6 "	"	"	
R76	00224	220K "	"	"	
R77	00822	8K2 "	"	"	1
R78	00562	5K6 "	"	"	
R79	00473	47K "	"	"	1
R80	00153	15K "	"	"	1
R81	02005	30K "	"	CR37	1
R82	00683	68K "	"	CR25	1
R83	00181	180R "	"	"	1
R84	00681	680R "	"	"	
R85	00681	680R "	"	"	2

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy.
R86-R89		NOT USED			
R90	00102	1K ±5% 1/4W	MULLARD	CR25	1
C31	11102	10μF/16V TANT	DUBILIER	100 880	1
C32	10681	68pF CERAMIC	MULLARD	632 34689	2
C33	10681	68pF "	"	632 34689	
C34		NOT USED			
C35	10222	220pF CERAMIC	MULLARD	632 58221	2
C36	10104	10nF "	"	629 06103	1
C37	10103	1nF "	"	629 02102	1
C38	10222	220pF "	"	632 58221	
S1	70001	TWO WAY PCB SWITCH	C+K	7201 L2 D9 V30B	6
S2	70002	THREE " " "	"	7203 L2 D9 V30B	2
S3-S6	70001	TWO " " "	"	7201 L2 D9 V30B	
S7					
S8	70002	THREE WAY PCB SWITCH	C+K	7203 L2 D9 V30B	
S9	70001	TWO " " "	"	7201 L2 D9 V30B	
J8	60010	10 WAY PCB SKT	MOLEX	A-4455-10A	6
J9	"	" " " "	"	"	
J9	"	" " " "	"	"	
J9	"	" " " "	"	"	

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DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy.
	60014	MAINS FILTER SKT	ROXBURGH	SDP 031	1
	60015	BNC SKT	GREENPAR	GE 35027	4
	60011	5 WAY CONNECTOR HOUSING	MOLEX	6471-5	1
	60017	CRIMP TERMINAL	MOLEX	2759	5
	65016	REAR PANEL	N.I.C.	65016	1
	65009	20mm FUSEHOLDER	BELLING LEE	E6011B	1
	65010	20mm x 160mA FUSE	R.S.	412-857	1
	65017	HEATSINK	REDPOINT	1.25GY	1
	65024	VENT PLUG	HEYCO	VP-875	2
	51003	MAINS SKT INSULATOR	R.S.	544-112	1
	51004	FUSEHOLDER INSULATOR	R.S.	544-106	1
	51001	H15 BLACK SLEEVE	R.S.	399-580	8
	51002	TRIBBON CABLE CLIP	R.S.	544-134	1
	62004	M3 x 10 SCREW CSK			2
	62005	M3 x 12 SCREW P.H.			3
	62007	M3 WASHER			5
	62008	M3 WASHER SH/PROOF			5
	62006	M3 NUT			5
	62014	M3 SOLDER TAG			2
	50002	5 WAY RIBBON CABLE	R.S.	FROM 357-025	300 mm

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APPROVED		DRAWING NUMBER	40017
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ISS										DRAWN	I.M.	TITLE
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CHKD										DATE		
										DRAWING NUMBER	40019	SHEET 2 OF 2

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No	No USED Per Assy.
	50002	3 WAY RIBBON CABLE	R.S.	FROM 357-025	200mm
	51001	HIS BLACK SLEEVE	R.S.	399-580	3
	60011	5 WAY CONNECTOR HOUSING	MOLEX	6471-5	1
	60017	CRIMP TERMINAL	MOLEX	2759	3
	70009	3 WAY BIASED SWITCH	C+K	7205-J61-ZQ-2-2	1

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ISS								DRAWN	I.M.	TITLE		
ECO								CHECKED		ARM/ABORT SWITCH ASSY.		
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CMKO								DATE		DRAWING NUMBER	40020	SHEET 2 OF 2

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy
	50002	10 WAY RIBBON CABLE	R.S.	357-025	455mm
	60013	10 WAY CONNECTOR HOUSING	MOLEX	6471-10	1
	60017	CRIMP TERMINAL	MOLEX	2759	20
	70010	HEXADECIMAL THUMBSCREW	CHERRY	T56-13RM	4
	71004	SPACER	"	609-0760	3
	71005	L.H. END CHEEK	"	609-0754	1
	71006	R.H. END CHEEK	"	609-0756	1

NOTES

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SHEET 2 OF 2									

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	60021 50005	40 WAY SOCKET 40 WAY FLAT CABLE	3M 3M	3417 6040	1 800 mm
	60023	8 WAY HOUSING	MOLEX	22-01-2086	2
	60017	CRIMP TERMINAL	RS	467 59B	16
	65012	BLACK CLIP	RS	424 181	3
	65022	GREEN CLIP	RS	424 204	1
	65018	BLUE CLIP	RS	424 197	1
	65019	YELLOW CLIP	RS	424 210	1
	51005 65025	HEATSHRINK 15mm x 21mm D.S. P.C.B.	RS	399 748	2 x 30 mm 2
	45011	BLACK WIRE 7/0.2 mm NUMERAL SET	I.P.S.		300 mm 1 SET

NOTES.

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER	PART No.	No. USED Per Assy
R1-R19	00125	1M2	MULLARD	CR25		19
R20-R38	00103	10K	"	"		19
R39-R57	00331	330	"	CR1G		19
R68-R76	00682	6KB	"	CR25		19
R77-R95	00272	2K7	"	"		19
C1-C19	10332	300pF	MULLARD	632 58331		19
C20-C25	10104	10nF	"	629 06103		6
C26-C27	12003	100μF	ELEC.	103 496		2
C28-C31	11102	10μF	TANT	DUBILIER	100 800	4
C32	11472	47μF	TANT	"	100 873	1
C33	10104	10nF	MULLARD	629 06103		
T1-T19	26004	TRANSISTOR NPN		BC 184C		19
T20-T38	26006	TRANSISTOR PNP		2N 3906		19
D1-D19	26001	G.P. DIODE		IN 4148		19
U1-U5	20018	DIG I.C.		74LS08		5
UG-U7	24007	VOLTAGE MIRROR	INTERSIL	ICL 7660 CPA		2
J1	26027	26 WAY HEADER	3M	3429 1303		1
J10	60026	40 WAY TRANSITION	3M	3418 0000T		1
	60021	40 WAY SOCKET	3M	3417 6000		1
	50005	40 WAY CABLE	3M	8000 MM		

NOTES										DATE 3-4-81		TITLE ZICON		
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TITLE 16 CHANNEL DATA POD											
SHEET 3 OF 3											

DESIGNATOR	PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANU. ACTOR/REF PART No	No USED Per Assy	
U1	20004	DIG. I.C.	FAIRCHILD	74LS14	4	
U2	20004	DIG. I.C.	"	74LS14	-	
U3	20002	DIG. I.C.	"	74LS04	1	
U4	20019	DIG. I.C.	"	74LS240	1	
U5	20020	DIG. I.C.	"	74LS241	1	
U6	20004	DIG. I.C.	"	74LS14	-	
U7	23004	DIG. I.C.	MOTOROLA	14069B	1	
U8	20004	DIG. I.C.	FAIRCHILD	74LS14	-	
D1-D3	80006	RED LED	RS	58G 475	3	
R1	00102	1K ±5%	1W	MULLARD	CR25	2
R2	00102	1K "	"	"	-	-
R3, R4	00103	10K "	"	"	-	2
R5-R7	00121	120 "	"	"	-	3
R8-R16	00472	4K7 "	"	"	-	9
S1	70012	MOMENTARY ACTION P/B	C & K	8121Z 7089 (BLACK)	1	
S2-S8	70011	SINGLE POLE C/O SLIDE	C & K	1101 M2 CQ (BLACK)	7	

NOTES

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SHEET
2 OF 3

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	11222	22MF TANT	DUBILIER	100 882	1
C2	10104	10nF CER	MULLARD	629 OG103	5
C3	10222	220PF "	"	632 58221	2
C4	10222	220PF "	"	632 58221	-
C5-C8	10104	10 nF "	"	629 OG103	-
J1	G0026	40 WAY TRANSITION CON.	3M (IDC)	3418 0000T	1
J1	G0021	40 WAY SOCKET	"	3417-6040	1
J12	G0029	26 WAY TRANSITION CON.	"	3434 0000T	1
J11	G0034	24 WAY IEEE CON.	"		1
J13	50009	10 WAY RIGHTANGLE CON.	MOLEX	5046 10A	1
	50005	40 WAY RIBBON CABLE	3M		800 MM
	50006	20 WAY RIBBON CABLE	"		300 MM
	60002	14 WAY IC SOCKET	ROBINSON NUGENT	ICY-143-S3T	6
	60030	20 WAY IC SOCKET	"	ICY-203-S3T	2
	G5023	POP CASE	PACTEC		1
	41024 RevB	P.C.B.	S.P.C.		1
	45008	LABLE	I.P.S.		1
	5100G	NYLON TUBE	PACTEC		4x5mm
	G2021	SELF TAP. SCREW			4

NOTES.

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DATE	13-4-81	ZICON
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DATE	DRAWING NUMBER 40024	SHEET 3 OF 3

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy
	60021	40 WAY SOCKET	3M	3417 6040	1
	50005	40 WAY FLAT CABLE	3M		800mm
	G5012	BLACK CLIP	RS	424 181	3
	G5011	RED CLIP	RS	424 175	16
	G5022	GREEN CLIP	RS	424 204	1
	G5018	BLUE CLIP	RS	424 197	1
	G5019	YELLOW CLIP	RS	424 210	1
	51005	HEATSHRINK	RS	399 748	2x30 mm
	65025	15 mm x 21 mm D.S. P.C.B.			2
	45011	NUMERAL SET	I.P.S.		1 SET
		BLACK WIRE 7/0.2 mm			300 mm
NOTES.					

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DATE	3-4-81	ZICON
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CHECKED		G32 CABLE ASSY
APPROVED		(CLIP)
DATE		DRAWING NUMBER
		40025
		SHEET
		2 OF 2

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy
	60028	26 WAY SOCKET	3M	3429 1303	1
	50006	26 WAY FLAT CABLE	3M		250 mm
	G5019	YELLOW CLIP	RS	424 210	1
	G5018	BLUE CLIP	RS	424 197	1
	G5022	GREEN CLIP	RS	424 204	1
	G5011	RED CLIP	RS	424 175	16
	60033	CROC. CLIP	RS	423 021	1
	65025	CROC. CLIP COVER	RS	423 368	1
	45011	NUMERAL SET	I.P.S.		1 SET
NOTES.					

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DATE	3-4-81	ZICON
DRAWN	G.C.M.	TITLE
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APPROVED		
DATE		DRAWING NUMBER
		40026
		SHEET
		2 OF 2

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy
	40015 REV B	MAIN BOARD ASSY	ZICON	40015 REV B	1
	40016 REV B	FRONT PANEL PCB ASSY	"	40016 REV B	1
	40017	REAR PANEL ASSY	"	40017	1
	40018	MAINS SWITCH ASSY	"	40018	1
	40019	INC/DEC SWITCH ASSY	"	40019	1
	40020	ARM/ABORT SWITCH ASSY	"	40020	1
	40021	THUMBWHEELS SWITCH ASSY	"	40021	1
	45005	FRONT PANEL OVERLAY	I.P.S.	45005	1
	51001	HIS BLACK SLEEVE	R.S.	399-580	3
	51002	RIBBON CABLE CLIP	R.S.	544-134	2
	62005	M3 X 12 SCREW P.H.			1
	62006	M3 NUT			1
	62007	M3 WASHER			1
	62008	M3 SH/PROOF WASHER			1
	62019	No. 4 X 1/4" SELF-TAP SCREW	JEE	SNPT 44	5
	65015	FRONT PANEL	S.P.C.	65015	1
	65021	INSTRUMENT CASE KIT	PRACTEC	CH325	1

NOTES.

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ISS	E.C.O.	DATE	CHKD

DATE	16/9/80	TITLE	MODEL 632 INSTRUMENT ASSY.
DRAWN	I.M.	CHECKED	
APPROVED		DATE	
		DRAWING NUMBER	40027
		SHEET	1 OF 1

DESIGNATOR	PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy
J13	60013	10 WAY HOUSING	MOLEX	6471-10	1
	60017	CRIMP TERMINAL	MOLEX	2759	10
	65011	SPRING CLIP (RED)	RS	424 175	8
	65019	" " (YELLOW)	"	424 210	1
	65012	" " (BLACK)	"	424 181	1
	45011	NUMERAL SET	I.P.S.		1 SET
	50007	BLACK WIRE	R.S.	357 184	200 MM
	50008	YELLOW WIRE	R.S.	357 255	200 MM
	50009	RED WIRE	R.S.	357 227	8 X 200 MM

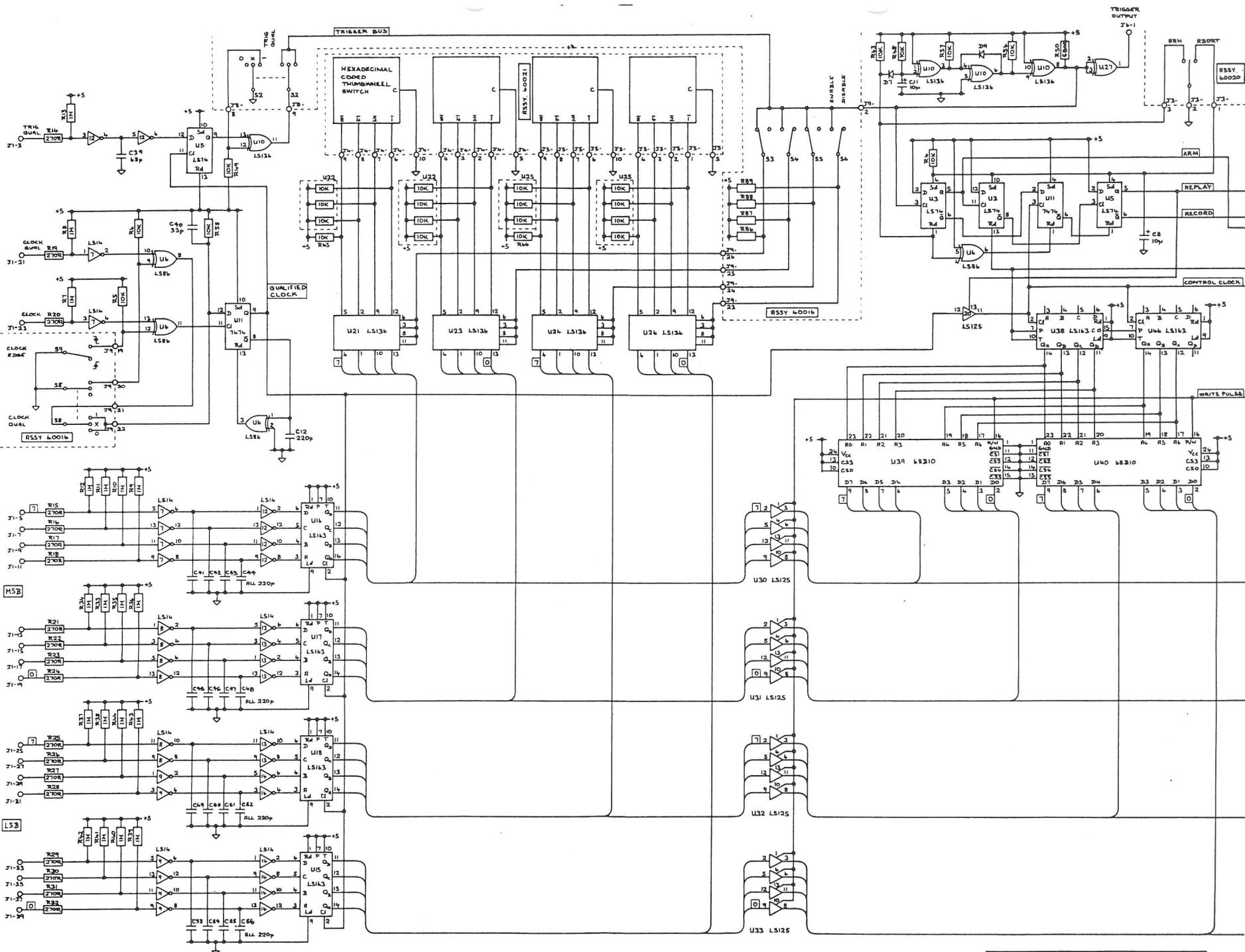
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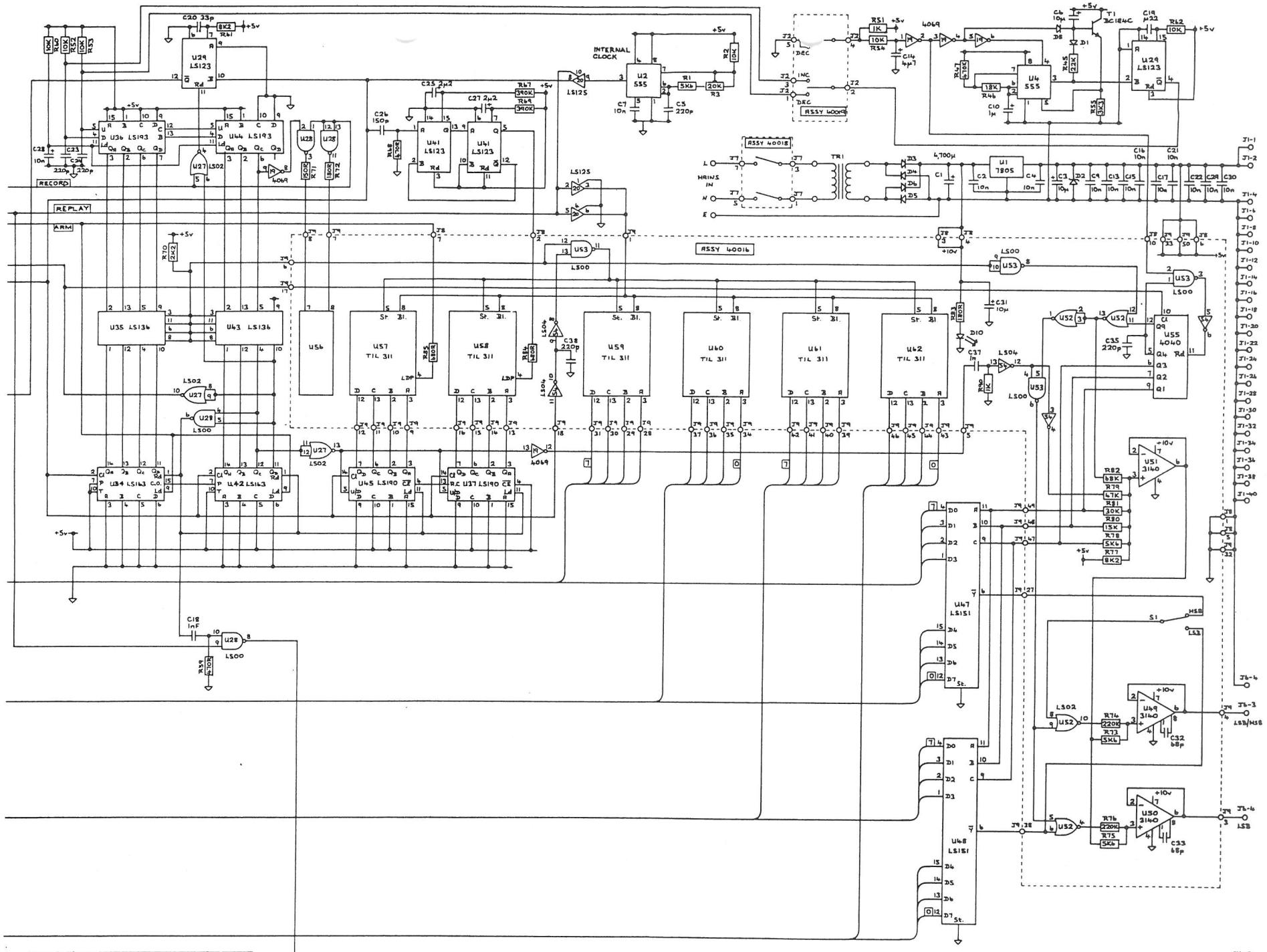
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DATE	15-8-81	TITLE	ZICON
DRAWN	G.C.M.	CHECKED	
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		DRAWING NUMBER	40028
		SHEET	2 OF 2

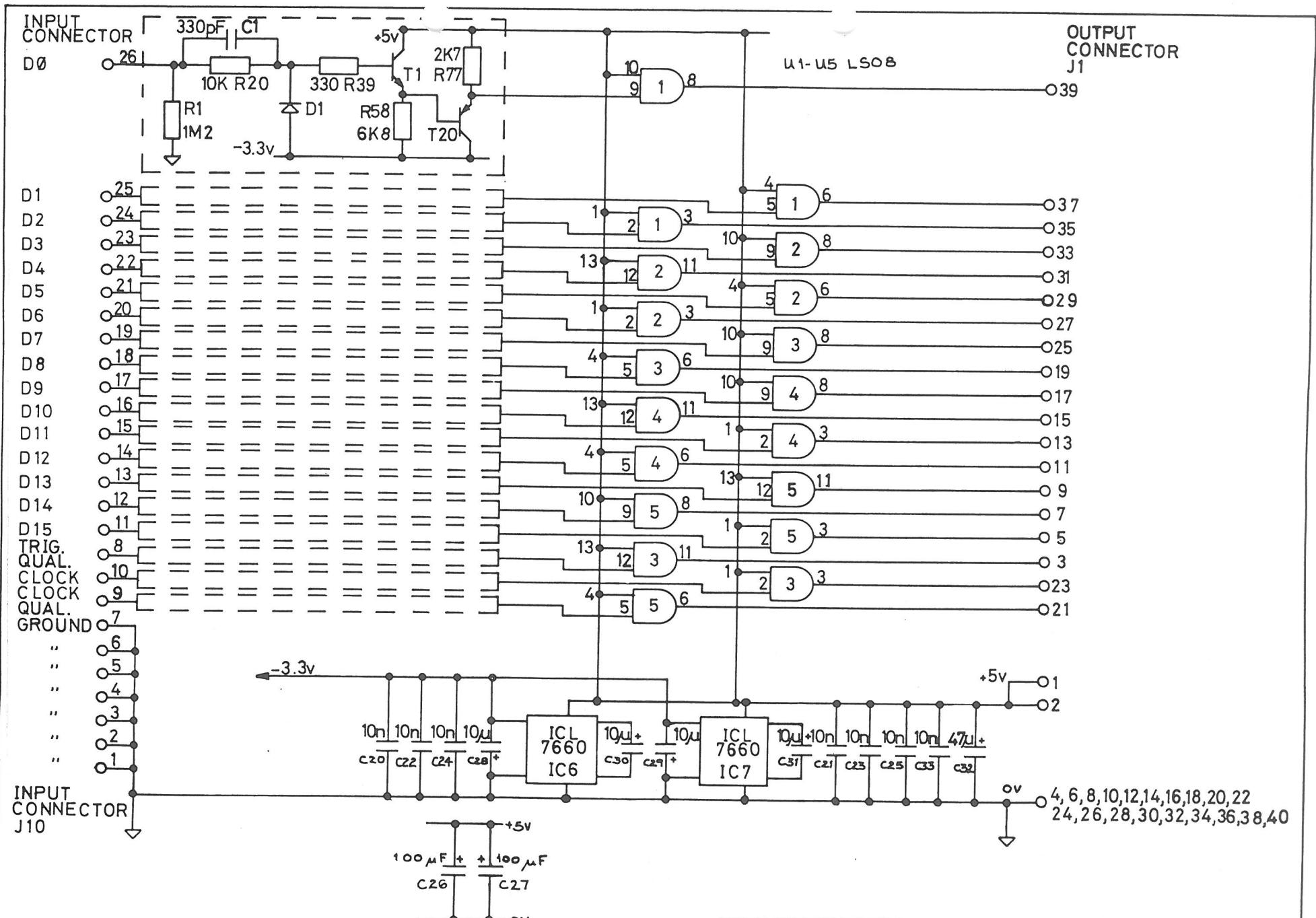
APPENDIX 2



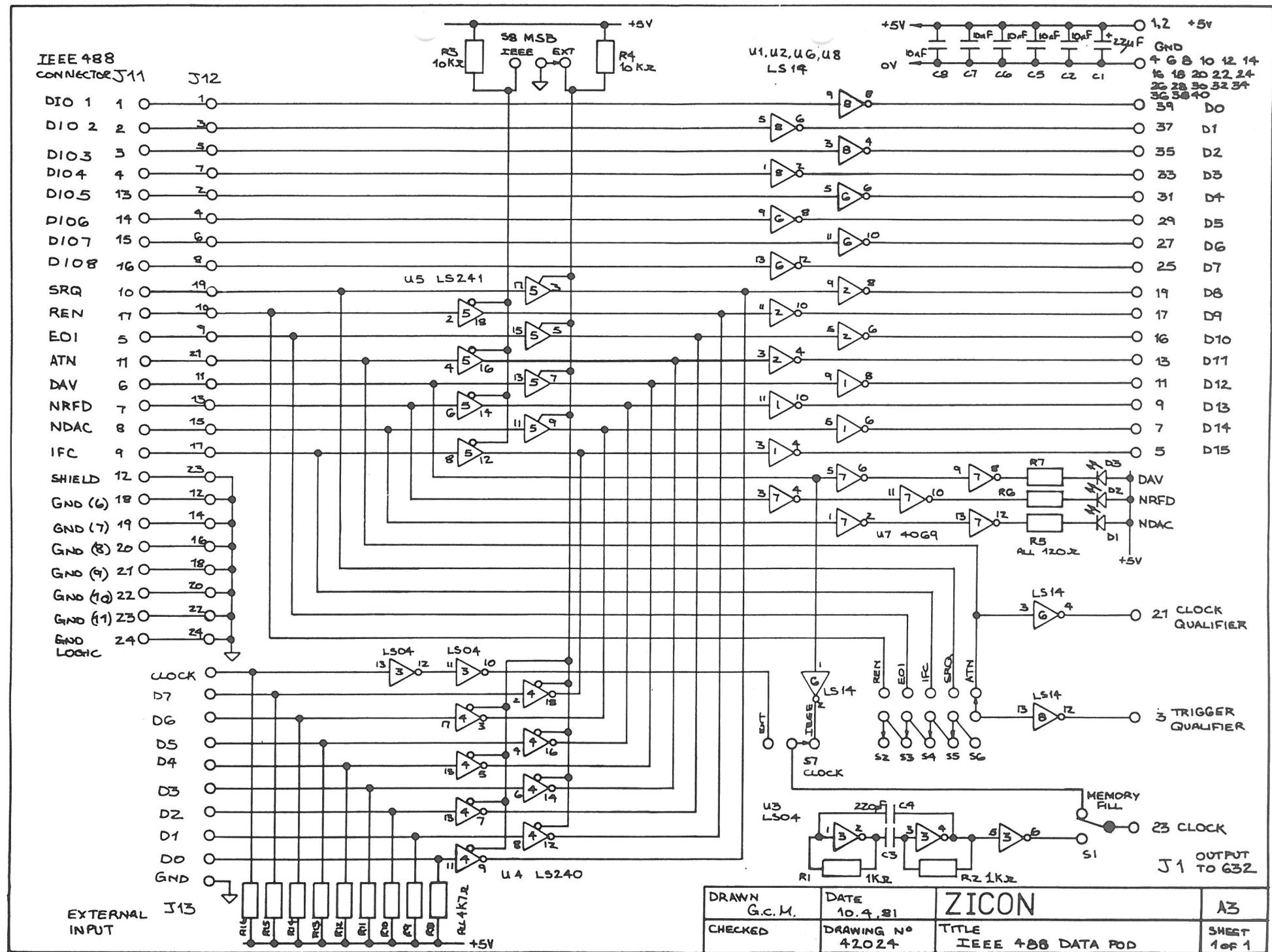


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3b-5
DISPLAY
TRIGGER



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DRAWN G.C.M.	DATE 10.4.81	ZICON	A3
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