# SERIES 54XXA SCALAR MEASUREMENT SYSTEMS 

MAINTENANCE MANUAL

## WARRANTY

The WILTRON product(s) listed on the title page is (are) warranted against defects in materials and workmanship for one year from the date of shipment, except for YIG-tuned oscillators, which are warranted for two years.

WILTRON's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to WILTRON for warranty repairs. Obligation is limited to the original purchaser. WILTRON is not liable for consequential damages.

## LIMITATION OF WARRANTY

The foregoing warranty does not apply to WILTRON connectors that have failed due to normal wear. Also, the warranty does not apply to defects resulting from improper or inadequate maintenance by the Buyer, unauthorized modification or misuse, or operation outside of the environmental specifications of the product. No other warranty is expressed or implied, and the remedies provided herein are the Buyer's sole and exclusive remedies.

## MANUAL CHANGES

## MANUAL:

Title: Series 54XXA Scalar Measurement Systems Maintenance Manual
Part Number: 10410-00123
Rev. Ltr/Date: A / N ovember 1992

## CHANGE PACKET

Part Number: 10900-00106

## INSTRUCTIONS

1. Make the manual changes listed below. These changes are listed in numerical order by page number.
2. The replacement pages provided in this change package are for technical changes and errata to the manual. The black bar or bars in the replacement page margins show the area in which the changes were made.

## CHANGE 1, February 1993:

## 1. Page 2-4:

Replace with enclosed pages 2-3 and 2-4, Changed: February 1993.
2. Pages 2-5 and 2-6:

Replace with enclosed fold-out pages 2-5 and 2-6, Changed: February 1993.

## 3. Pages 6-24 and 6-25:

Replace with enclosed pages 6-23 through 6-26, Changed: February 1993.

## 4. Pages A-5 and A-6:

Replace with enclosed appendix pages A-5 and A-6, Changed: February 1993.

## TABLE OF CONTENTS

## Chapter 1 - General Service Information

This section provides a general description of series 54XXA Scalar Measurement Systems, system serial numbers, and frequency ranges. It explains the level of maintenance covered in this manual and provides preventative maintenance procedures. It also contains static-sensitive component handling precautions and a list of recommended test equipment.

## Chapter 2 - Replaceable Parts

This Chapter lists all replaceable subassemblies and components for all 54XXA models. It explains the WILTRON exchange assembly program and provides parts ordering information.

## Chapter 3 - Troubleshooting

This chapter provides information for troubleshooting 54XXA Scalar Measurement Systems. The troubleshooting information and fault location tables contained in this chapter support fault isolation down to a replaceable subassembly.

## Chapter 4 - Functional Overview

This chapter provides descriptions of the functional operation of the major assemblies contained in 54XXA series Scalar Measurement Systems. The operation of all major circuit blocks is described so that the reader may better understand the function of each major assembly as part of the overall operation of the 54XXA.

## Chapter 5 - Removal and Replacement Procedures

This chapter describes how to gain access to the major 54XXA assemblies and parts for troubleshooting or replacement.

## Chapter 6 - Adjustments

This chapter provides adjustment procedures for all models of series 54XXA Scalar Measurement Systems. These procedures are used after replacement or repair of one or more critical subassemblies, or as indicated by the Performance Verification Procedures (which are contained in Section V of the Series 54XXA Scalar Measurement Systems Operation Manual).

## Appendix A - RF Detector Diode Replacement Procedures

This appendix contains rf detector diode replacement procedures for 5400-71XXX and 560-7XXX series RF Detectors.

## Table of Contents (Continued)

## Appendix B - Fabrication of RF Detector Simulator

This appendix contains information for fabricating the T1492 RF Detector Simulator test aid. This test aid is used in the calibration procedures contained in Chapter 6.

## Appendix C - Fabrication of Dummy Thermistor Test Aids

This appendix contains information for fabricating the T38300 Dummy Down Converter Thermistor and the T38301 Dummy Directional Coupler Thermistor test aids. These test aids are used in the Temperature Compensation Adjustment Procedure for series 54XXA Scalar Measurement Systems contained in Chapter 6.

# Chapter 1 General Service Information 

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Figure 1-1. M odel 5417A Scalar Measurement System with Detector and SWR Autotester (and Test Device)

## Chapter 1 General Service Information

1-1 scope of the manual
This manual provides general service and preventative maintenance information, replaceable parts information, circuit descriptions, troubleshooting procedures, and adjustment procedures for WI LTRON series 54XXA Scalar Measurement Systems (SMS's). Throughout this manual, these systems are referred to as "54XXA".

## 1-2 introduction

## 1-3 identification number

## 1-4 description of 54xia SYSTEM

All WILTRON instruments are assigned a six-digit ID number, such as "101001." This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with WILTRON Customer Service about this instrument.
This chapter of the manual provides a general description of series 54XXA Scalar Measurement Systems, system serial numbers, frequency ranges, and related manuals. Also included is information about the level of maintenance covered in this manual, preventative maintenance procedures, and static-sensitive component handling precautions. A list of recommended test equipment is also provided.

Series 54XXA systems are microprocessor controlled scalar measurement systems. These systems are used to make scalar (magnitude) transmission, reflection, and absolute power measurements. A typical model is shown in Figure 1-1 (facing page). All measurement functions are selectable by using the front panel keys and controls in conjunction with the display screen menus. Refer to the 54XXA Scalar Measurement Systems Operation Manual for information about operation of these systems. Refer also to that manual for information about system options, SWR Autotesters, detectors, and other accessories used with series 54XXA Systems.

Table 1-1. 54XXA M odel Frequency Ranges

| Model | Frequency Range (GHz) |  |  |
| :---: | :---: | :---: | :---: |
| 5407 A | 0.001 | to | 1.0 |
| 5409 A | 0.001 | to | 2.0 |
| 5411 A | 0.001 | to | 3.0 |
| 5417 A | 0.01 | to | 8.6 |
| 5419 A | 2.0 | to | 8.6 |
| 5428 A | 8.0 | to | 12.4 |
| 5431 A | 10.0 | to | 16.0 |
| 5430 A | 12.4 | to | 20.0 |
| 5436 A | 17.0 | to | 26.5 |
| 5437 A | 2.0 | to | 20.0 |
| 5447 A | 0.01 | to | 20.0 |

1-5 LEVEL OF MAINTENANCE

The measurement frequency range of the 54XXA is determined by:
$\square$ The range of the internal signal source of the particular model.
$\square$ The external SWR Autotester and/or detector used with the 54XXA.

The table at left lists the frequency ranges of all 54XXA models. For information about the frequency ranges and characteristics of WILTRON SWR Autotesters and RF detectors normally used with series 54XXA models, refer to the 54XXA Scalar M easurement Systems Operation Manual.

Option 3 to the 54XXA provides remote operation using the IEEE-488 General Purpose Interface Bus (GPIB). This option allows all 54XXA front panel control functions (except POWER on/off) to be controlled remotely from an external computer/controller using GPIB commands. Refer to the 54XXA Scalar Measurement Systems Operation Manual for information about other options and accessories available for 54XXA models.

Maintenance and troubleshooting of the 54XXA consists of:
$\square$ Troubleshooting the 54XXA to a replaceable subassembly
$\square$ Repair by replacing the failed subassembly
$\square$ Adjustments
$\square$ Preventive maintenance

Troubleshooting and Repair

Most faults involving the 54XXA are field repairable by replacing the subassembly that is at fault. The procedures contained in this manual provide troubleshooting to this level. Refer to Chapter 3, Troubleshooting.

This manual also contains procedures for replacing defective detector diodes for Series 560-7XXX RF Detectors and for 5400-71B 75 RF Detectors. These procedures are contained in Appendix A.

Replaceable Subassemblies and Parts

Adjustments Procedures for adjustment of the 54XXA after repair or replacement of one or more subassemblies is described in Chapter 6, Adjustments.

## 1-7 preventive maintenance

Preventive Maintenance

The 54XXA Scalar Measurement Systems Operation Manual (1041000118) describes the front panel operation for all 54XXA models. It also contains general information, specifications, and Performance Verification procedures for all models.

Operation of the 54XXA remotely via the IEEE-488 General Purpose Interface Bus (GPIB) is described in the 54XXA Series Scalar Measurement Systems GPIB User's Guide (10410-00119). This user's guide is located at the rear of the 54XXA Scalar Measurement Systems Operation Manual.

The 54XXA must always receive adequate ventilation. Check and clean the rear panel fan filter periodically. Clean this filter more frequently in dusty environments. Proceed as follows:
Step 1 Remove the four capnuts holding the filter in place (Figure 1-2).

Step 2 Remove the filter.
Step 3 Clean the filter by flushing with compressed air.
Step 4 Replace the filter by reversing the previous steps.
Step 5 Ensure that the cap nuts are securely tightened.


Figure 1-2. Fan Filter Removal/ Replacement

1-8
STATIC SENSITIVE COMPONENT HANDLING PRECAUTIONS

1-9
RECOMMENDED TEST EQUIPMENT

The 54XXA contains components that can be damaged by static electricity. Figure 1-3 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

## NOTE

Use of a grounded wrist strap when removing and/or replacing subassemblies or parts is strongly recommended.

The recommended test equipment for the adjustment and troubleshooting procedures presented in this manual are listed in Table 1-2.


1. Do not touch exposed contacts on any static sensitive component.

2. Wear a static-discharge wristband when working with static sensitive components.

3. Handle PCBs only by their edges. Do not handle by the edge connectors.

4. Do not slide static sensitive component across any surface.

5. Label all static sensitive devices.

6. Lift \& handle solid state devices by their bodies - never by their leads.

7. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

8. Keep component leads shorted together whenever possible.

9. Transport and store PCBs and other static sensitive devices in staticshielded containers.
10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-3. Static SensitiveComponent Handling Procedures

| $54 X X A M M$ | $1-7$ |
| :--- | :--- |

Table 1-2. Recommended Test Equipment

| INSTRUMENT | CRITICAL SPECIFICATION | RECOMMENDED MANUFACTURER/MODEL | USE\# |
| :---: | :---: | :---: | :---: |
| Adaptor Cable | Connection to 54XXA Channel Inputs | WILTRON Model 560-10BX | P, A |
| Detector Simulator | Simulates WILTRON RF Detectors | WILTRON T1492 (see Appendix B) | A |
| Computer/Controller | Personal computer, equipped with National PCIIA GPIB interface card | Any IBM compatible (or WILTRON Model 85, or HP Model 200) | P, T |
| RF Detector | 1. $50 \Omega$ input, 1.0 to $3000 \mathrm{MHz}^{*}$ <br> 2. $75 \Omega$ input, 1.0 to $3000 \mathrm{MHz}^{* *}$ <br> 3. 0.010 to 18.5 GHz <br> 4. 0.010 to $26.5 \mathrm{GHz} \ddagger$ | WILTRON Model 5400-71N50 WILTRON Model 5400-71N75 WILTRON Model 560-7N50 WILTRON Model 560-7K50 | P, A |
| Impedance Adapter | Converts from $50 \Omega$ to $75 \Omega$ | WILTRON Model 12N75B | P, A, T |
| Digital Multimeter | Resolution: 4-1/2 digits (to 20V ) DC Accuracy: $0.002 \%+2$ counts DC Input Impedance: $10 \mathrm{M} \Omega$ AC Accuracy: $0.07 \%+100 \mathrm{cts}(\leq 20 \mathrm{kHz})$ AC Input Impedance: $1 \mathrm{M} \Omega$ | John Fluke Mfg Co. Inc., <br> Model 8840A, with <br> Option 8840A-09, True RMS AC | A, T |
| Frequency Counter | Frequency: 0.1 to 26.5 GHz Input Impedance: $50 \Omega$ | EIP Microwave, Inc., Model 578A | P, A |
| Modulation Meter | Bandwidth: 15 kHz <br> Accuracy: $\pm 3 \%$ of FSD at 1 kHz | Marconi Instruments Inc., Model 2304 | P, A |
| Oscilloscope | Bandwidth: DC to 100 MHz <br> Sensitivity: 2 mV <br> Horiz. Sensitivity: $50 \mathrm{~ns} /$ division | Tektronix, Inc. Model 2445 | A, T |
| Power Meter, with: <br> Power Sensor* $50 \Omega$ input Power Sensor** $75 \Omega$ input Power Sensor <br> Power Sensor\# <br> Atten, Calibration | Power Range: +10 to -55 dBm <br> Other: 50 MHz Calibrated Output <br> Frequency Range: 1.0 MHz to 2.0 GHz <br> Power Range: -30 to +20 dBm <br> Frequency Range: 1.0 MHz to 5.5 GHz <br> Power Range: -30 to +20 dBm <br> Frequency Range: 0.10 to 18.0 GHz <br> Power Range: -30 to +20 dBm <br> Power Range: -70 to -20 dBm <br> Frequency Range: 0.05 to 26.5 GHz <br> Power Range: -30 to +20 dBm <br> Power Range: -70 to -20 dBm <br> Atten: 30 dB , used with MA4702A/04A | Anritsu Corp., Model ML4803A <br> Anritsu Corp., Model MA4601A Anritsu Corp., Model MA4603A with J0365 Conversion Connector <br> Anritsu Corp., Model MA4701A Anritsu Corp., Model MA4702A <br> Anritsu Corp., Model MA4703A <br> Anritsu Corp., Model MA4704A <br> Anritsu Corp., Model MP47A | P, T |
| Printer | Parallel Interface operation | WILTRON, Model 2225C Ink Jet Printer, or equivalent | P, T |
| Spectrum Analyzer | Frequency Range: 0.01 to 26.5 GHz Power Range: +10 dB to -60 dBm | Anritsu Corp., Model MS2802 | P, T |
| Step Attenuator | Attenuation Range: $60 \mathrm{~dB}, 10 \mathrm{~dB} /$ step 0.000 to 18.0 GHz <br> 0.000 to 26.5 GHz | Hewlett-Packard, Model 8495B Hewlett-Packard, Model 8495D | P, A |
| Voltage Standard | Range: 0 mV to -1.462 V Accuracy: $0.002 \%$ of set value. | John Fluke Mfg Co. Inc., Model 335D | P, A, T |
| * Required for models 5407A, 5409A, and 5411A with $50 \Omega$ output. <br> ** Required for models 5407A, 5409A, and 5411A with $75 \Omega$ output, only. <br> \# Required for model 5436A, only. |  | \# Use Code: <br> A Adjustment <br> P Performance verification procedures <br> T Troubleshooting |  |

# Chapter 2 Replaceable Parts 

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## Chapter 2 <br> Replaceable Parts

## 2-1 introduction

## 2-2 exchange ASSEMBLY PROGRAM

## 2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

## 2-4 <br> PARTS ORDERING INFORMATION

This chapter provides replaceable parts information for all 54XXA models. The location of the major replaceable assemblies is shown in Figures 2-1 and 2-2 (pages 2-7 and 2-8).

WILTRON maintains a module exchange program for selected subassemblies of all 54XXA models. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, WILTRON will ship the exchange subassembly to you, typically within 24 hours. You then have 30 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call WILTRON Customer Service direct (paragraph 2-4).

Table 2-2 (page 2-5) lists the major replaceable subassemblies and parts for the 54XXA that are presently covered by the WILTRON exchange assembly program. Table 2-3 and Table 2-4 (page 2-6) list model-dependent and common replaceable parts for the 54XXA that are not presently on the exchange assembly program.

All parts listed in Tables 2-2 through 2-4 may be ordered from your local WILTRON service center (Table 2-1). Or, they may be ordered directly from the factory at the address shown below.

WILTRON Company
ATTN: Customer Service
490 J arvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408)-778-2000
TWX: 285227 WILTRON MH
FAX: (408)-778-0239

Table 2-1. WILTRON Service Centers

| UNITED STATES | CHINA | JAPAN |
| :---: | :---: | :---: |
| WILTRON COMPANY | WILTRON BEIJING SERVICE | ANRITSU CORPORATION |
| 490 Jarvis Drive | CENTER | 1800 Onna Atsugi-shi |
| Morgan Hill, CA 95037-2809 | 416 W Beijing Fourtune Bldg | Kanagawa-Prf. 243 Japan |
| Telephone: (408) 778-2000 | 5 Dong San Huan Bei Lu | Telephone: 0462-23-1111 |
| Telex: 285227 WILTRON MH | Chao Yang Qu, Beijing, China | FAX: 0462-25-8379 |
| FAX: (408) 778-0239 | Telephone: (861) 501-7559 |  |
| ANRITSU WILTRON SALES | FAX: (861) 501-7558 | KOREA |
| COMPANY |  | WILTRON CORPORATION |
| 685 Jarvis Drive |  | 1201 Sinsong Bldg. 12F, |
| Morgan Hill, CA 95037-2809 | FRANCE | 25-4 Yeoeuido-Dong |
| Telephone: (408) 776-8300 | WILTRON S.A | Youngdeungpo-ku, Seoul |
| FAX: (408) 776-1744 | 9 Avenue du Quebec | Telephone: (02) 785-6407 |
|  | Zone de Courtaboeuf | FAX: (02) 784-6409 |
| ANRITSU WILTRON SALES | 91951 Les Ulis Cedex |  |
| COMPANY | Telephone: (01) 64-46-65-46 | SWEDEN |
| 15 Thornton Road | FAX: (01) 64-46-10-65 |  |
| Oakland, NJ 07436 |  | WILTRON AB |
| Telephone: (201) 337-1111 | INDIA | Box 247 |
| FAX: 201-337-1033 | INDIA | S-127 25 Skarholmen |
|  | ACCUTROL SYSTEMS PRIVATE | Telephone: (08) 7405840 |
| AUSTRALIA | LIMITED | Telex: (854) 8135089 |
| AUSTRALIA | Nirmal, 15th Floor | FAX: (08) 7109960 |
| WILTRON PTY. LTD.. | Narimen Point |  |
| 1/410 Church Street | Bombay 400021 | TAIWAN |
| North Parramatta | Telephone: 011-91-22-202-2220 | WILTRON CO., LTD. |
| NSW 2151 Australia | : 011-91-22-204-7187 | 8F, No. 96, Section 3 |
| Telephone: (02) 6308166 <br> Fax: (02) 6836997 | FAX: 011-91-22-202-9403 | Chien Kuo N. Road |
| BRAZIL | ISRAEL | Taipei, Taiwan, R.O.C. <br> Telephone: (02) 515-6050 |
|  | TECH-CENT, LTD | FAX: (02) 505-5519 |
| ANRITSU ELECTRONICA S.A. | 7A, Pinhas Rosen Street |  |
| Av. Passos, 91-Sobrelojas | Tel-Aviv 69356 | UNITED KINGDOM |
| 203/205-Centro | Telephone: (03) 481958 |  |
| 20.051 Rio de Janeiro-RJ Telephone: (011) 2853091 | FAX: (03) 481958 | Capability Green |
| Telex: 1133532 ANBR BR |  | Luton, Bedfordshire |
| Fax: (011) 2886940 | ITALY | LU1 3LU, England |
|  | WILTRON Sp.A | Telephone: (0582) 418853 |
| CANADA | Roma Office | Telex: (851) 826750 |
|  | Via E. Vittorini, 129 | FAX: (011) 582-31303 |
| WILTRON INSTRUMENTS LTD. | 00144 Roma EUR |  |
| 215 Stafford Road, Unit 102 | Telephone: (06) 5005171 | WEST GERMANY |
| Nepean, Ontario K2H 9C1 <br> Telephone: (613) 726-8800 | FAX: (06) 5005273 | WILTRON GmbH |
| FAX: (613) 820-9525 |  | Rudolf Diesel Str 17 |
|  |  | 8031 Gilching |
|  |  | Telephone: (08105) 8055 |
|  |  | Telex: (841) 528523 |
|  |  | FAX: (08105) 1700 |


| Reference Designator | $\begin{aligned} & \text { 54XXA } \\ & \text { Option } \end{aligned}$ | Assembly/Part | 5407A | 5409A | 5411A | 5417A | 5419A | 5428A | 5430A | 5431A | 5436A | 5437A | 5447A |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 |  | Front Panel PCB | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 | D35051-3 |
| A2 |  | Front Panel Interface PCB | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 | D35052-3 |
| A3 |  | Signal Channel PCB (std) | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 | D35345-3 |
|  | Option 5 | Signal Channel PCB (w/R input) | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 | D35053-3 |
| A5 |  | YIG Driver/Signal Channel Intf. PCB | D35358-10 | D35358-10 | D35358-10 | D35358-4 | D35358-4 | D35358-5 | D35358-6 | D35358-7 | D35358-8 | D35358-9 | D35358-9 |
| A6 |  | ALC/Frequency Instruction PCB | ND37738-1 | ND37738-2 | ND37738-3 | ND37738-4 | ND37738-4 | ND37738-4 | ND37738-4 | ND37738-4 | ND37738-4 | ND37738-4 | ND37738-4 |
| A7 |  | Central Processor/GPIB PCB w/o GPIB | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 | D35357-3 |
|  | Option 3 | Central Processor/GPIB PCB w GPIB | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 | D35357-4 |
| A8 |  | Graphics Processor PCB | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 | D35066-3 |
| A10 |  | Menu PCB Assembly | C35060-3 | C35060-3 | C35060-3 | C35060-3 | C35060-3 | C35060-3 | C35060-3 | С35060-3 | C35060-3 | C35060-3 | С35060-3 |
| A11 |  | 500 MHz Sample/Marker Assembly |  |  |  | C35329 | C35329 | C35329 | C35329 | C35329 | C35329 | C35398 | C35398 |
| A12/A13 |  | $500 \mathrm{MHz} \mathrm{VCO} / \mathrm{PA}$ Assembly |  |  |  | C35192 | C35192 | C35192 | C35192 | C35192 | C35192 | C35396 | C35396 |
| A14 |  | 25 MHz Marker Assembly |  |  |  | C35194-11 | C35194-11 | C35194-7 | C35194-7 | C35194-7 | C35194-7 | C35397 | C35397 |
| A17 |  | RF Deck Distribution Panel Assembly (PCB) |  |  |  | C35287-3 | C35287-3 | C35287-3 | C35287-3 | C35287-3 | C35287-3 |  |  |
| A18 |  | Switched Filter Driver Assembly (PCB) |  |  |  | C35286-3 | C35286-3 |  |  |  |  |  |  |
| A19 |  | Multiband Controller Assembly |  |  |  |  |  |  |  |  |  | D35430-3 | D35430-3 |
|  |  | Power Supply Assembly * | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 | D35370 |
|  |  | CRT Monitor Assembly | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 | D35047 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Option 2 | Step Attenuator Assembly, $70 \mathrm{~dB}, 3 \mathrm{GHz}$ | D24335 | D24335 | D24335 |  |  |  |  |  |  |  |  |
|  | Option 2A | Step Attenuator Assembly, $70 \mathrm{~dB}, 20 \mathrm{GHz}$ |  |  |  | 4412K | 4412K | 4412 K | 4412K | 4412K |  | 4412 K | 4412K |
|  | Option 2B | Step Attenuator Assembly, $70 \mathrm{~dB}, 26.5 \mathrm{GHz}$ |  |  |  |  |  |  |  |  | 4512K |  |  |
|  |  | Output Coupler |  |  |  | D21450 | D21450 | D21450 | D21450 | D21450 | D21452 | D21450 | D21450 |
|  |  | Down Converter | D25472 | D25472 | D25472 | D25471 |  |  |  |  |  |  | D25471 |
|  |  | Modulator Assembly |  |  |  | D22870 | D22870 | D22880 | D22900 | D22890 | D22910 |  |  |
|  |  | Switched Filter Assembly |  |  |  | ND39316 | ND39316 |  |  |  |  | D22040 | D22040 |
|  |  | 3 GHz Marker Assembly | D25432 | D25432 | D25432 | D25432 |  |  |  |  |  |  | D25432 |
|  |  | 2 GHz Marker Assembly |  |  |  | C30954-1 |  |  |  |  |  |  |  |
|  |  | YIG Oscillator | C22550 | C22550 | C22550 | C24436** | C24436** | C11282 | C14770-1 | C22560 | C29963 | C21620 | C21620 |

* For instruments with serial numbers 103014 and below, use Power Supply Assembly ND37737.
** For Models 5417 A and 5419 A with 8.4 GHz upper band-edge, use YIG Oscillator C22570.

| Assembly/Part |  | $\begin{gathered} \hline \text { 5407A } \\ \hline \text { B35283 } \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { 5409A } \\ \hline \text { B35283 } \end{array}$ | $\begin{gathered} \hline \text { 5411A } \\ \hline \text { B35283 } \end{gathered}$ | $\begin{array}{r} 5417 \mathrm{~A} \\ \hline \text { C18650-1 } \end{array}$ | $\begin{array}{r} \text { 5419A } \\ \hline \text { C18650-1 } \end{array}$ | $\begin{array}{r} 5428 A \\ \hline \text { C18650-1 } \end{array}$ | 5430A <br> C18650-1 | $\begin{array}{r} \text { 5431A } \\ \hline \text { C18650-1 } \end{array}$ | 5436A | $\begin{array}{r} \text { 5437A } \\ \hline \text { C18650-1 } \end{array}$ | $\begin{array}{r} \text { 5447A } \\ \hline \text { C18650-1 } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RF Output Connector, | $50 \Omega$, Type N |  |  |  |  |  |  |  |  |  |  |  |
| RF Output Connector, | $50 \Omega$, Type K |  |  |  |  |  |  |  |  | C18640-1 |  |  |
| RF Output Conector, | $75 \Omega$, Type N * | B35284 | B35284 | B35284 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| Front Panel Overlay |  | D35026-10 | D35026-11 | D35026-12 | D35026-13 | D35026-14 | D35026-15 | D35026-16 | D35026-17 | D35026-18 | D35026-22 | D35026-20 |
|  |  |  |  |  | D35026-24\# | D35026-26\# |  |  |  |  |  |  |
| Front Panel Overlay (for units w/Option $5^{* * \text { ) }}$ |  | D35026-1 | D35026-2 | D35026-3 | D35026-4 | D35026-5 | D35026-6 | D35026-7 | D35026-8 | D35026-9 | D35026-21 | D35026-19 |
|  |  |  |  |  | D35026-23\# | D35026-25\# |  |  |  |  |  |  |

* 54XXA Option 4 (5407A, 5409A and 5411A, only)
** Third front panel input
\# For units with 8.6 GHz upper band edge.
Table 2-4. Common 54XXA Replaceable Subassemblies and Parts

| Assembly/Part | Part <br> Number | Assembly/Part | Part <br> Number |
| :--- | :--- | :--- | :--- |
| Cover, Top | D30125 | Fuse, 4A, 3AG Slow Blow (115 Vac Operation) | $631-16$ |
| Cover, Bottom | D30126 | Fuse, 2A, Time Lag, 20 mm (230 Vac Operation) | $631-67$ |
| Cover, Side | D30127 | Fuse Holder, 3AG Type | $533-221$ |
| Cover, Side (modified, with holes) | C30051 | Fuse Holder, 5 5 20 mm Type | $533-240$ |
|  |  |  |  |
| Connector, Front Panel Input | $557-152$ | Knob, Data Entry | $710-62$ |
|  |  |  |  |
| Fan Assembly, Rear Panel | C35215 | Line Module Assembly, Rear Panel | B35375 |
| Fan Filter | $783-377$ |  | C13654 |
| Finger Guard, Fan | $790-251$ | Tilt Bail |  |
| Dome Nut, (for Finger Guard) | $900-579$ |  |  |
|  |  |  |  |
| Foot, Rear | D13656 |  |  |
| Foot, Bottom | D13655 |  |  |



Figure 2-1. $54 X X A$ Major Assemblies Location Diagram (Top View)


Figure 2-2. 54XXA Major Assemblies Location Diagram (Bottom View)

# Chapter 3 Troubleshooting 

## Table of Contents

3-1 INTRODUCTION ..... 3-3
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Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

## WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

## CAUTION

Many assemblies in the 54XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies.
Always observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-3.

# Chapter 3 Troubleshooting 

## 3-1 introduction

## 3-2 recommended test EQUIPMENT

3-3 power-up and self TEST DIAGNOSTICS

This chapter provides information for troubleshooting 54XXA Scalar M easurement Systems. The troubleshooting operations presented in this chapter support fault isolation down to a replaceable subassembly. (Remove and replace procedures for major 54XXA assemblies are contained in Chapter 5.)

The recommended test equipment for the troubleshooting operations presented in this chapter is listed in Chapter 1, Table 1-2 (page 1-8).

The 54XXA firmware includes internal diagnostics that are initiated during power-up of the unit, or when the SELF TEST key is pressed. These diagnostics also check for fault conditions during normal operation. Any fault or error conditions found are reported as described below. Tables 3-1 and 3-2 (pages 3-5 and 3-6) list all possible error messages. F or each specific error message, the table provides either a possible cause of the fault, or a reference to another troubleshooting table that contains more detailed troubleshooting operations. There are three primary types of error messages that are reported by the diagnostics:
$\square$ Power-up and Self Test Errors
$\square$ Calibration Errors
$\square$ Normal Operation Error and Warning Messages

## Power-up and Self Test Errors

Serious system malfunctions detected during powerup or Self Test will be flagged by a bold FAILED TESTS CRT display. Specific fault messages will also be reported; for example: A7 GPIB Interface fail. These "self test" fault conditions are also indicated by means of one or more flashing front panel LED indi cators. A specific LED flashes steadily after completion of the self test for each fault detected. Table $3-1$ shows which error message and LED indicator correspond to each major fault condition. Note that the flashing LED indicator provides exactly the same information as the CRT failure message; should the CRT fail, this technique can be used as a troubleshooting aid. The faults listed in Table 3-1 generally indicate malfunctions in the major PCB assemblies of the 54XXA.

## Calibration Errors

After self test, and prior to starting normal operation, the 54XXA performs an internal frequency lock calibration. These calibrations are also performed periodically during normal operation. If a frequency calibration test fails, one or more "calibration error" messages will be displayed along with the FAILED TESTS display (example: fails het band $\mathbf{5 0 0} \mathbf{~ m i s s}$ ); refer to Tables 3-2a and 3-2b. Calibration error messages generally indicate RF deck related problems. During normal operation, a failed calibration is indicated by a failure code displayed in the lower right corner of the screen display (described below). These error codes are listed in Table 3-3 al ong with suggested remedial action.

When an abnormal condition is detected during normal operation, an error or warning messages is displayed in the message box located in the lower right corner of the screen display, as described below. If more than one fault is detected, the highest priority error message will be displayed. Error messages take precedence over warning messages.
Error Messages - These messages report malfunctions that occur either during self test or during normal operation. They can be identified by the presence of a failure code; example: $\mathbf{5 0 0} \mathbf{~ M H z}$ markers 201. Table 3-3 lists these codes and suggested remedies.
Warning Messages - These messages report procedural errors; example: NO CAL DATA. They do not report fault conditions or malfunctions, but they do indicate that an invalid operation has been attempted. A Warning message can be distinguished from an error message by the absence of an error code following the message. Refer to the 54XXA Operation Manual, Appendix A, Table A-3, for descriptions of warning messages and remedies.

3-4
MALFUNCTIONS NOT DISPLAYING ERROR MESSAGES

3-5 $\begin{aligned} & \text { troubleshooting } \\ & \text { tables }\end{aligned}$

Some major system malfunctions may not cause an error message or error code to be displayed. These include problems with the RF deck, CRT monitor, and power supply. Troubleshooting procedures for these problems are provided in Tables 3-8 through 3-22, which begin on page 3-14.

Tables 3-4 through 3-23 that begin on page 3-9 provide procedures for isol ating malfunctions to a replaceable subassembly. In cases where any of several subassemblies are suspect, subassembly replacement is indicated. The recommended replacement order is for the most-likely subassemblies to be replaced first.

Table 3-1. Error Messages and Front Pane LED Indicators for Power-Up/ Self Test Errors

| Condition/Fault | Associated Front Panel LED | Recommended Action |
| :--- | :--- | :--- |
| CPU ASM test running | HARDCOPY PRINTER | PRINTER LED normally flashes during Self Test. |
| A6 PERSONALITY fail | HARDCOPY PLOTTER | Replace A6 PCB *. |
| A7 EPROM U32 check sum fail | CURSOR ON/OFF | Replace A7 PCB *. |
| A7 EPROM U31 check sum fail | CURSOR RELATIVE | Replace A7 PCB *. |
| A7 EPROM U30 check sum fail | DISPLAY, CHAN 1 | Replace A7 PCB *. |
| A7 PROGRAM RAM fail | DISPLAY, CHAN 2 | Replace A7 PCB * |
| A8 LOAD GSP fail | AVERAGING, CHANNEL 1 | Replace A8 PCB * |
| A8 PIPE INTERFACE fail | AVERAGING, CHANNEL 2 | Replace A8 PCB *. |
| A7 NON VOLATILE RAM fail | SMOOTHING, CHAN'S 1 \& 2 | Replace A7 PCB *. |
| A7 INTERRUPT CONTROLLER fail | LEVELING, INTERNAL | Replace A7 PCB *. |
| A7 TIMESLICE GENERATOR fail | LEVELING, EXTERNAL | Replace A7 PCB *. |
| A7 GPIB Interface fail | UNLEVELED | Replace A7 PCB *. |
| A2 KEYBOARD INTERFACE fail | REMOTE | Replace A2 PCB. Refer to PCB removal <br> procedures, paragraph 5-6.. <br> A3 SIGNAL CHANNEL PRESENT <br> or A5 SIGNAL CHANNEL ADC fail CALIBRATION UNCAL |
| Self Test completed | Replace A3 PCB, then Replace A5 PCB, as <br> necessary. Refer to PCB removal procedures, <br> paragraphs 5-3 and 5-4. |  |

* Refer to PCB removal procedures, paragraph 5-3.

Tables 3-2a \& 3-2b. Displayed Error Message Headings and MessageText for Calibration Redated Faults/Errors

| $3-2 a$ERROR MESSAGE HEADINGS* |  | 3-2bERROR MESSAGE TEXT* |  |
| :---: | :---: | :---: | :---: |
| Heading | Category/Type | Message | Meaning |
| GENERAL | Major errors | no 500 | 500 MHz markers cannot be found during GENERAL test |
| START- <br> MAIN | Calibration of START DAC (using main coil) | 500 miss | 500 MHz marker missing during START-MAIN DAC or WIDTH-MAIN DAC calibrations |
| ERROR | Calibration of ERROR DAC (using FM coil) | 1st wrong | For START-MAIN DAC or WIDTH-MAIN DAC calibrations: Cannot find two markers with correct spacing in first group of three at top of frequency range. <br> For HET BAND calibration: Offset between main band 500 MHz markers and HET band 25 MHz markers is out of specification. |
| WIDTHMAIN | Calibration of WIDTH DAC (using main coil) | 500 size | 500 MHz markers not large enough during STARTMAIN DAC or WIDTH-MAIN DAC calibrations |
| WIDTH-FM | Calibration of WIDTH DAC (using FM coil) | spacing | Cannot find two markers with correct spacing in group of three during ERROR, WIDTH-FM, or HET BAND calibrations (using FM coil). |
| HET BAND | Verification of Downconverter and 25 MHz Marker Box operation | Error Codes 210 to 212 | This series of error codes will be displayed after a Frequency Calibration if an error occurs (Refer to paragraph 3-3 and Table 3-3.). |
|  |  | Error Codes 213 and above | This series of error codes will be displayed only during fault diagnosis in the Engineering Mode of operation. To put 54XXA in this mode, refer to paragraph 6-4, step 3 , on page 6-7. Then press DATA ENTRY keys " 4 and " 1 " in sequence to turn on Calibration Error Codes. To return to normal mode, press SELF TEST key. Refer Table 3-3 for explanations of the error codes. |

* These headings and messages are displayed on the CRT Monitor. When 54XXA reverts to normal screen display, the corresponding error codes will be displayed in the lower right corner of the screen display. The error codes are described in Table 3-3.

Table 3-3. Error Codes for Calibration Redated Faults/ Errors (1 of 2)

| Calibration Error Code | Error Description | Refer to Table: |
| :---: | :---: | :---: |
| 201 | General, no 500 MHz or 75 MHz markers | 3-4 |
| 202 | START DAC main band, 500 MHz or 75 MHz marker(s) missing; or, top or bottom frequency(s) not correctly set | 3-4 |
| 203 | START DAC main band, 1st MHz markers (top) wrong | 3-5 |
| 204 | START DAC main band, 500 MHz or 75 MHz marker size error | 3-5 |
| 205 | ERROR DAC, 25 MHz marker spacing wrong | 3-6 |
| 206 | WIDTH DAC main band, 500 MHz or 75 MHz marker(s) missing | 3-4 |
| 207 | WIDTH DAC main band, 1 st MHz markers (top) wrong | 3-5 |
| 208 | WIDTH DAC main band, 500 MHz or 75 MHz marker size error | 3-5 |
| 209 | WIDTH DAC fm, 25 MHz marker spacing wrong | 3-6 |
| 210 | HET band, 500 MHz or 75 MHz marker missing | 3-4 |
| 211 | HET band, 25 MHz and 500 MHz marker spacing wrong | 3-6 |
| 212 | HET band, 25 MHz marker spacing wrong | 3-6 |
| 213 | Start lb, START DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 214 | Start lb, 25 MHz slow lock fail | 3-6 |
| 215 | Stop lb, WIDTH DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 216 | Stop lb, 25 MHz slow lock fail | 3-6 |
| 217 | Start mb, START DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 218 | Start mb, 25 MHz slow lock fail | 3-6 |
| 219 | Stop mb, WIDTH DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 220 | Stop mb, 25 MHz slow lock fail | 3-6 |
| 221 | Start hb, START DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 222 | Start hb, 25 MHz slow lock fail | 3-6 |
| 223 | Stop hb, WIDTH DAC, 500 MHz or 75 MHz marker missing | 3-4 |
| 224 | Stop hb, 25 MHz slow lock fail | 3-6 |
| 225 | lb chan1 error, multiple slow lock fail | 3-7 |
| 226 | lb chan2 error, multiple slow lock fail | 3-7 |
| 227 | mb chan1 error, multiple slow lock fail | 3-7 |


| $54 X X A M M$ | $3-7$ |
| :--- | :---: |

## CALIBRATION RELATED

ERROR CODES
TROUBLESHOOTING

Table 3-3. Error Codes for Calibration Related Faults/ Errors (2 of 2)

| Calibration Error Code | Error Description | Refer to Table: |
| :---: | :---: | :---: |
| 228 | mb chan2 error, multiple slow lock fail | 3-7 |
| 229 | hb chan1 error, multiple slow lock fail | 3-7 |
| 230 | hb chan2 error, multiple slow lock fail | 3-7 |
| 231 | lb chan1 error, 25 MHz slow lock fail | 3-6 |
| 232 | lb chan2 error, 25 MHz slow lock fail | 3-6 |
| 233 | mb chan1 error, 25 MHz slow lock fail | 3-6 |
| 234 | mb chan2 error, 25 MHz slow lock fail | 3-6 |
| 235 | hb chan1 error, 25 MHz slow lock fail | 3-6 |
| 236 | hb chan2 error, 25 MHz slow lock fail | 3-6 |
| 237 | lb mb chan1 error, 25 MHz fast lock fail | 3-6 |
| 238 | lb mb chan2 error, 25 MHz fast lock fail | 3-6 |
| 239 | mb chan1 error, 25 MHz fast lock fail | 3-6 |
| 240 | mb chan2 error, 25 MHz fast lock fail | 3-6 |
| 241 | hb chan1 error, 25 MHz fast lock fail | 3-6 |
| 242 | hb chan2 error, 25 MHz fast lock fail | 3-6 |
| 243 | lb chan1 error, 25 MHz ref fast lock fail | 3-6 |
| 244 | lb chan2 error, 25 MHz ref fast lock fail | 3-6 |
| 245 | mb chan1 error, 25 MHz ref fast lock fail | 3-6 |
| 246 | mb chan2 error, 25 MHz ref fast lock fail | 3-6 |
| 247 | hb chan1 error, 25 MHz ref fast lock fail | 3-6 |
| 248 | hb chan2 error, 25 MHz ref fast lock fail | 3-6 |

Table 3-4. Error Messages 201, 202, 206, 210, 213, 215, 217, 219, 221, or 223 (1 of 1)
ERROR MESSAGES 201, 202, 206, 210, 213, 215, 217, 219, 221, or 223
Step 1. Perform Self Test and note all error messages. Then perform marker adjustment procedure Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 2. Check for front panel RF output.
QUESTION: Was RF output present?
YES: Go to next step.
NO: See troubleshooting table on RF deck problems (Table 3-10, or 3-12, or 3-15, as appropriate.

Step 3. Replace the 500 MHz Sample/Marker module, and perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 4. Replace the 500 MHz VCO/PA module, and perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-5. Error Messages 203, 204, 207, or 208 (1 of 1)
ERROR MESSAGES 203, 204, 207, or 208

Step 1. Perform Self Test and note all error messages. Then perform marker adjustment procedure Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 2. Replace the 500 MHz Sample/M arker module, and perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-6. Error Messages 205, 209, 211, 212, 214, 216, 218, 220, 222, 224, or 231 through 248 (1 of 2)
ERROR MESSAGES 205, 209, 211, 212, 214, 216, 218, 220, 222, 224, or 231 through 248
Step 1. Perform Self Test and note all error messages. Then perform marker adjustment procedure Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 2. Determine specified frequency range of unit.
QUESTION: Is unit specified below 2 GHz ?
YES: Go to next step.
NO: Go to step 4.
Step 3. Perform hetrodyne band 25 MHz marker verification - Chapter 6, paragraph 6-7.
QUESTION: Wereany 25 MHz markers missing, or spurious markers present?
YES: Goto step 7.
NO: Go to next step.
Step 4. Replace 25 MHz Marker module. (Refer to Chapter 5, Figures 5-6 through 5-9, as appropriate.) Then perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 5. Replace 500 MHz VCO/PA module. (Refer to Chapter 5, Figures 5-6 through 5-9, as appropriate.) Then perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.

Table 3-6. Error Messages 205, 209, 211, 212, 214, 216, 218, 220, 222, 224, or 231 through 248 (2 of 2 )

Step 6. Replace 500 MHz Marker module. (Refer to Chapter 5, Figures 5-6 through 5-9, as appropriate.) Then perform marker adjustment procedure - Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Call Customer Service.
Step 7. Replace 2 GHz or 3 GHz Marker module, as appropriate for model. (Refer to Chapter 5, Figures 5-6 through 5-9, as appropriate.)

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Go to next step.
Step 8. Replace the Down Converter module and perform ALC adjustment — Chapter 6, paragraph 6-8.
QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-7. Error Messages 225 thru 230 (1 of 1 )

## ERROR MESSAGES 225 thru 230

Step 1. Perform Self Test and note all error messages. Then perform marker adjustment procedure Chapter 6, paragraph 6-6.

QUESTION: Is error message gone?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-8. RF Deck Problems - M odels 5407A, 5409A, or 5411A (1 of 2)

## RF Deck Problems - Models 5407A, 5409A, or 5411A

Step 1. Reset instrument and measure power into the step attenuator, if installed. If no attenuator, go to next step.

QUESTION: Is theRF leve into the attenuator approximatel y equal to the power out of the front pane?

YES: Go to next step.
NO: Go to Table 3-17 (step attenuator problems).
Step 2. Measure the RF output of the YIG oscillator (at YIG).
QUESTION: Is theRF level between -1 dbm and +6 dBm ?
YES: Go to next step.
NO: Go to step 6.
Step 3. Perform YIG driver adjustment - Chapter 6, paragraph 6-4, and ALC adjustment - Chapter 6, paragraph 6-8.

QUESTION: Was adjustment procedure successful?
YES: Problem is cleared.
NO: Go to next step.
Step 4. Measure the supply voltages to the Down Converter module per Table 3-13.
QUESTION: Are the voltages correct?
YES: Replace down Converter module.
NO: Replace A5 PCB.
Step 5. Perform YIG driver adjustment - Chapter 6, paragraph 6-4, and ALC adjustment - Chapter 6, paragraph 6-8.

QUESTION: Was adjustment procedure successful?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-8. RF Deck Problems - M odel s 5407A, 5409A, or 5411A (2 of 2)

Step 6. Measure the signal and bias voltages to the YIG oscillator per Table 3-9.
QUESTION: Are the voltages correct?
YES: Replace YIG oscillator (refer to Chapter 5, paragraph 5-12); then go to step 3.

NO: Replace A5 PCB (refer to Chapter 5, paragraph 5-3); then go to step 3.

Table 3-9. YIG Assembly Control Signal Voltages

| Control Signal | Location | Value* $^{c}$ |
| :--- | :---: | :---: |
| +15 V Bias | YIG Assembly Connector | +15 V |
| -5 V Bias | YIG Assembly Connector | -5 V |
| FM Coil Signal** | A5 PCB, TP1 (ref. TP2) | -10 V to +10V |
| Main Coil Tuning Ramp | A5 PCB, TP5 (ref. TP4) | 0 V to +10 V |

* All values $\pm 0.5 \mathrm{~V}$, unless noted.
** Set WIDTH to $<40 \mathrm{MHz}$.

Table 3-10. RF Deck Problems - Models 5428A, 5430A, 5431A, or 5436A (1 of 2)
RF Deck Problems - Models 5428A, 5430A, 5431A, or 5436A
Step 1. Reset instrument and measure power into the step attenuator, if installed. If no attenuator, go to next step.

QUESTION: Is theRF leve into the attenuator approximatel y equal to the power out of the front pane?

YES: Go to next step.
NO: Go to Table 3-17 (step attenuator problems) on page 3-24.
Step 2. Measure input into the Directional Coupler module.
QUESTION: Is theinput level greater than 10 dBm full band?
YES: Go to troubleshooting Table 3-16 (ALC leveling problems) on page 3-23.
NO: Go to next step.
Step 3. Measure the RF output of the YIG oscillator (at YIG).
QUESTION: Is theRF level greater than 13 dBm ?
YES: Goto step 6.
NO: Go to next step.
Step 4. Measure the signal and bias voltages to the YIG oscillator per Table 3-9.
QUESTION: Are the voltages correct?
YES: Replace YIG oscillator (refer to Chapter 5, paragraph 5-12).
NO: Replace A5 PCB (refer to Chapter 5, paragraph 5-3).
Step 5. Perform YIG driver adjustment - Chapter 6, paragraph 6-4, and ALC adjustment - Chapter 6, paragraph 6-8.

QUESTION: Was adjustment procedure successful?
YES: Problem is cleared.
NO: Go to next step.

Table 3-10. RF Deck Problems - Model s 5428A, 5430A, 5431A, or 5436A (2 of 2)

Step 6. Measure the signal and bias voltages to the Control M odulator module per Table 3-11.
QUESTION: Are the voltages correct?
YES: $\quad$ Replace the Control Modulator module (refer to Chapter 5, paragraph 5-12).
NO: Replace A6 PCB (refer to Chapter 5, paragraph 5-3).
Step 7. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Was adjustment successful?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-11. Control Modulator Signal and Bias Voltages

| Control Signal | Location | Value $^{*}$ |
| :--- | :---: | :---: |
| Mod Control | A6 PCB, TP18 | Approx. +14 V to -4 V (pulse chain) |
| Mod Bias | A6 PCB, TP19 | Approx. +14 V to -14 V (pulse chain) |

* All values $\pm 0.5 \mathrm{~V}$

Table 3-12. RF Deck Problems Be ow 2 GHz - Models 5417A and 5447A (1 of 3)
RF Deck Problems Below 2 GHz - Models 5417A and 5447A
Step 1. Reset instrument.
QUESTION: Is theRF output problem only below 2 GHz ?
YES: Go to next step.
NO: Go to Table 3-15 (RF problems above 2 GHz ) on page 3-21.
Step 2. Measure power into the step attenuator, if installed. If no attenuator, go to next step.
QUESTION: Is theRF leve into the attenuator approximately equal to the power out of the front pane?

YES: Go to next step.
NO: Go to Table 3-17 (step attenuator problems) on page 3-24.
Step 3. Measure the RF power level at the output of the Switched Filter assembly (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).

QUESTION: Is it greater than 11.0 dBm ?
YES: Go to next step.
NO: Go to step 7.
Step 4. Measure the input signal voltages to the Down Converter module per Table 3-13. (Measure at test points on A6 PCB.)

QUESTION: Are the voltages correct?
YES: Go to next step.
NO: Replace A6 PCB (refer to Chapter 5, paragraph 5-3).

Table 3-13. Down Converter ModuleSignal and Bias Voltages

| Control Signal | Location | Value $^{*}$ |
| :--- | :---: | :---: |
| Mod Control | A6 PCB, TP16 | Approx. +14 V to -4 V (pulse chain) |
| Mod Bias | A6 PCB, TP17 | Approx. +14 V to -14 V (pulse chain) |
| $*$ All values $\pm 0.5 \mathrm{~V}$ |  |  |

Table 3-12. RF Deck Problems Be ow 2 GHz - Models 5417A and 5447A (2 of 3)

Step 5. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Is output leveled?
YES: Problem is cleared.
NO: Replace the Down Converter module (refer to Chapter 5, paragraph 5-12).
Step 6. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Is output leveled?
YES: Problem is cleared.
NO: $\quad$ For model 5417A, go to next step. For model 5447A, go to step 8.
Step 7. Measure the logic level signals going to the Switched Filter assembly per Table 3-14. (Measure at the RF Deck Distribution Panel PCB; refer to Chapter 5, Figures 5-7 and 5-9, as appropriate.)

QUE STION: Are the voltages correct?
YES: Go to next step.
NO: Go to step 10.

Table 3-14. Switched Filter Driver Assembly Input Signals

| A17 RF Deck Dist. PnI. PCB, <br> Connector XA18 Pin No. | Signal Voltage <br> Value $^{*}$ |
| :---: | :---: |
| 1 thru 5 | Toggling (0V to $+5 \mathrm{~V})$ |
| 6 | Not used |
| 7 | $+15 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| 8 | $0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| 9 | $-15 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| All values $\pm 0.5 \mathrm{~V}$ |  |

Table 3-12. RF Deck Problems Be ow 2 GHz - Models 5417A and 5447A (3 of 3)

Step 8. Replace the Switched Filter assembly (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).
QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: F or model 5417A, go to next step. F or model 5447A, call Customer Service.
Step 9. Replace the A18 Switched Filter Driver assembly (mounted on the Switched Filter assembly —refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).

QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: Call Customer Service.
Step 10. Replace the A7 Central Processor PCB.
QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: Go to step 8.

Table 3-15. RF Deck Problems Greater Than 2 GHz, Models 5417A, 5419A, 5437A, or 5447A (1of 2)

## RF Deck Problems Greater Than 2 GHz, Models 5417A, 5419A, 5437A, or 5447A

Step 1. Reset instrument and measure power into the step attenuator, if installed. If no attenuator, go to next step.

QUESTION: Is theRF leve into the attenuator approximately equal to the power out of the front pane?

YES: Go to next step.
NO: Go to Table 3-17 (step attenuator problems).
Step 2. Measure the RF power level at the input of the Directional Coupler module (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).

QUESTION: Is the input level greater than 10 dBm full band?
YES: Go to Table 3-16 (ALC leveling problems).
NO: Go to next step.
Step 3. Measure the RF power level at the output of the YIG oscillator (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).

QUESTION: Is the power greater than 13 dBm .
YES: Go to step 5.
NO: Go to next step.
Step 4. Verify YIG oscillator signal and bias voltages per Table 3-9.
QUESTION: Are they correct?
YES: Replace YIG oscillator (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).
NO: Replace the A5 YIG Driver/Signal Interface PCB (refer to Chapter 5, paragraph 5-3).

Table 3-15. RF Deck Problems Greater Than 2 GHz, Models 5417A, 5419A, 5437A, or 5447A (2 of 2)

Step 5. Perform YIG driver adjustment - Chapter 6, paragraph 6-4, and ALC adjustment - Chapter 6, paragraph 6-8.

QUESTION: Was adjustment procedure successful?
YES: Problem is cleared.
NO: For models 5417A and 5419A, go to next step. F or models 5437A and 5447A, go to step 7.

Step 6. Measure the logic level signals going to the Switched Filter assembly per Table 3-14 on page 3-19. (Measure at the RF Deck Distribution Panel PCB; refer to Chapter 5, Figures 5-7 and 5-9, as appropriate.)

QUESTION: Are the vol tages correct?
YES: Go to next step.
NO: Go to step 9.
Step 7. Replace the Switched Filter assembly (refer to Chapter 5, Figures 5-7 and 5-9, as appropriate).
QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: $\quad$ For models 5417A and 5419A, go to next step. F or models 5437A and 5447A, call Customer Service.

Step 8. Replace the A18 Switched Filter Driver assembly (mounted on the Switched Filter assembly -refer to Chapter 5, Figures 5-7 and 5-9, as appropriate)..

QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: Call Customer Service.
Step 9. Replace the A7 Central Processor PCB.
QUESTION: Is there output power across the band?
YES: Problem is cleared.
NO: Go to step 7.

Table 3-16. ALC Leveling Problems (1of 1)

## ALC Leveling Problems

Step 1. Reset instrument.
QUESTION: Is leveling problem below 2 GHz ?
YES: $\quad$ Refer to Table 3-8, or Table 3-12, as appropriate (RF deck problems).
NO: Go to next step.
Step 2. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Is unit leveling?
YES: Problem is cleared.
NO: Replace the Directional Coupler module (or Down Converter module for RF models). (Refer to Chapter 5, Figures 5-6 through 5-9, as appropriate.)

Step 3. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Was adjustment successful?
YES: Problem is cleared.
NO: Replace A6 ALC/F requency Instruction PCB (refer to Chapter 5, paragraph 5-3).
Step 4. Perform ALC adjustment - Chapter 6, paragraph 6-8.
QUESTION: Was adjustment successful?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-17. Step Attenuator Problems (1of 2)

## Step Attenuator Problems

Step 1. Reset instrument. Verify drive signals for each attenuator step per Table 3-18 or 3-19, as appropriate for model.

QUESTION: Aredrivesignals correct?
YES: Replace the step attenuator assembly.
NO: Replace the A7 Central Processor PCB.

Table 3-18. Step Attenuator DriveSignals for RF Band Models 5407A, 5409A, and 5411A

| A4 Motherboard | Attenuator Step* |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Connector J6 Pin No. | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 |
| 1 | Not used |  |  |  |  |  |  |  |
| 2 | H | H | H | H | L | L | L | L |
| 3 \& 4 | Not used |  |  |  |  |  |  |  |
| 5 | H | H | H | H | H | H | L | L |
| 6 | H | H | H | H | H | H | H | H |
| 7 \& 8 | Not used |  |  |  |  |  |  |  |
| 9 | H | L | H | L | H | L | H | L |
| 10 | H | H | L | L | L | L | L | L |
| 11 thru 14 | Not used |  |  |  |  |  |  |  |

* To set 54XXA to desired attenuator step, set RF output level to same value as step; e.g., 0 dBm for step $0,-10 \mathrm{dBm}$ for step $10 \ldots$ etc. $\mathrm{H}=$ approx 24 V
$\mathrm{L}=$ approx OV

Table 3-17. Step Attenuator Problems (2of 2)

Table 3-19. Step Attenuator Drive Signals for MicrowaveBand Modeds 5417A through 5447A

| A4 Motherboard Connector J6 Pin No. | Attenuator Step |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 |
| 1 | Not used |  |  |  |  |  |  |  |
| 2 | H | L | H | L | H | L | H | L |
| 3 | L | L | L | L | H | H | H | H |
| 4 | Not used |  |  |  |  |  |  |  |
| 5 | H | H | L | L | H | H | L | L |
| 6 | H | H | H | H | H | H | H | H |
| 7 \& 8 | Not used |  |  |  |  |  |  |  |
| 9 | H | H | H | H | L | L | L | L |
| 10 | Not used |  |  |  |  |  |  |  |
| 11 | L | L | H | H | L | L | H | H |
| 12 | Not used |  |  |  |  |  |  |  |
| 13 | L | H | L | H | L | H | L | H |

* To set 54XXA to desired attenuator step, set RF output level to same value as step; e.g., 0 dBm for step $0,-10 \mathrm{dBm}$ for step $10 \ldots$ etc. $\mathrm{H}=$ approx 24 V
$\mathrm{L}=$ approx 0 V

Table 3-20. CRT Monitor Problems (lof 2)

## CRT Monitor Problems

Step 1. Switch unit off, then back on.
QUESTION: Is display normal?
YES: Problem is cleared.
NO: Go to next question.
QUESTION: Is thereany display at all?
YES: Go to step 3.
NO: Go to next step.
Step 2. Measure +12 V power supply voltage across pins 10 and 11 of A4J 2. (Refer to Table $3-22$ and associated figure on page 3-28).

QUESTION: Is +12 V present?
YES: Go to next step.
NO: Refer to Table 3-21 (power supply problems) to correct fault condition. Then recheck CRT display per this table, as necessary.

Step 3. Observe CRT monitor display.
QUESTION: Does the display exhibit a single horizontal lineor dot?
YES: Replace the CRT monitor assembly (refer to Chapter 5, paragraph 5-8). Then go to next step.

NO: Go to next step.
Step 4. Observe CRT monitor display.
QUESTION: Is display normal?
YES: Problem is cleared.
NO: Go to next step.

Table 3-20. CRT M onitor Problems (2of 2)

Step 5. Replace the A8 Graphics Processor PCB (refer to Chapter 5, paragraph 5-3).
QUESTION: Is display normal?
YES: Problem is cleared.
NO: Go to next step.

Step 6. Replace the A7 Central Processor PCB (refer to Chapter 5, paragraph 5-3).
QUESTION: Is display normal?
YES: Problem is cleared.
NO: Go to next question.

QUE STION: Was CRT monitor assembly replaced in step 3?
YES: Call Customer Service.
NO: Go to next step.

Step 7. Replace the CRT monitor assembly (refer to Chapter 5, paragraph 5-8).
QUESTION: Is display normal?
YES: Problem is cleared.
NO: Call Customer Service.

Table 3-21. Power Supply Problems (1of 1)

## Power Supply Problems

Step 1. Switch unit off and wait five minutes for capacitors to discharge. Clean the rear panel fan filter, check the fuse and verify the voltage selector setting. Then, turn unit back on.

QUESTION: Is unit operating properly?
YES: Problem is cleared.
NO: Go to next step.
Step 2. Verify power supply voltages per Table 3-22 and associated figure.
QUESTION: Areall voltages correct per table?
YES: Go to troubleshooting table for CRT monitor problems (Table 3-20).
NO: Replace power supply.
Step 3. Verify power supply voltages per Table 3-22 and associated figure.
QUESTION: Areall voltages correct per table?
YES: Problem is cleared.
NO: Call Customer Service.


A9 Power Supply M otherboard Connector Location \& Orientation

Table 3-22. Power supply Voltages

| Nominal <br> Voltage | Measure: <br> A9 J2 Pin No. | Reference: <br> A9 J2 Pin No. | Value |
| :---: | :---: | :---: | :---: |
| +5 V | 2,4 | 1,3 | $+5 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| +12 V | 12,11 | 10,14 | $+12 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| +15 V | 6,7 | 8,16 | $+15 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| -15 V | 9 | ground | $-15 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| -18 V | 15 | ground | $-18 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| +22 V | 13 | ground | $+22 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |
| Nominal <br> Voltage | J3 Pin No. <br> (A9 PCB) | J3 Pin No. <br> (A9 PCB) | Value |

Table 3-23. Measurement Channe Problems (1of 1 )

## Measurement Channel Problems

Step 1. Initiate 54XXA Self Test.
QUESTION: Does Failed Test message for A3 PCB or A5 PCB occur?
YES: If $A 3$ PCB error only, replace $A 3 P C B$.
If A5 error is indicated, replace A5 PCB.
NO: Go to step 3.
Step 2. Perform Signal Channel Adjustment Procedure - Chapter 6, paragraph 6-3.
QUESTION: Is unit operating properly?
YES: Problem is cleared.
NO: Call Customer Service.
Step 3. With a normal measurement mode display on CRT monitor, check for presence of error warning message in lower right hand corner of screen display.

QUESTION: Is therea warning message?
YES: Refer to 54XXA Operation Manual - Appendix A, Table A-3. Take remedial action appropriate for error message and go to next question below.

NO: Go to next step.
QUESTION: Is unit operating properly?
YES: Problem is cleared.
NO: Go to next step.
Step 4. Refer to 54XXA Operation Manual - Section IV, paragraph 4-4, and observe operation of 54XXA while performing an appropriate measurement operation.

QUESTION: Is the unit operating normally?
YES: Problem is cleared.
NO: Call Customer Service.

# Chapter 4 Functional Description 

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## Chapter 4 <br> Functional <br> Description

## 4-1 introduction

## 4-2 overview of 54xxa SERIES SYSTEMS

This chapter provides descriptions of the functional operation of the major assemblies contained in each of the models of the 54XXA series Scalar Measurement Systems. The operation of each of the major circuit blocks is described so that the reader may better understand the function of the major assembly as part of the overall operation of the 54XXA. (The CRT monitor assembly is not covered in this chapter this assembly is replaced as an entire unit.)

Eleven models comprise the 54XXA Scalar Measurement System series. The RF models (Table 4-1) cover a frequency range of 1.0 MHz to 3.0 GHz . The microwave models cover a frequency range of 10 MHz to 26.5 GHz.

Table 4-1. 54XXA M ode Frequency Ranges

| Model Group | Model | Frequency <br> Range (GHz) |  |
| :---: | :---: | :---: | :---: |
|  | 5407A | 0.001 to | to 1.0 |
| RF | 5409A | 0.001 | to 2.0 |
|  | 5411A | 0.001 to | to 3.0 |
|  | 5417A | 0.01 | to 8.6 |
|  | 5419A | 2.0 | to 8.6 |
|  | 5428A | 8.0 | to 12.4 |
| Microwave | 5431A | 10.0 | to 16.0 |
|  | 5430A | 12.4 | to 20.0 |
|  | 5436A | 17.0 | to 26.5 |
|  | 5437A | 2.0 | to 20.0 |
|  | 5447A | 0.01 to | to 20.0 |

The frequency range of measurements that can be made by each model is determined by the signal source (Table 4-1) and by the SWR Autotester and/or RF detector(s) used with the analyzer section of the 54XXA. The frequency ranges and characteristics of WILTRON SWR Autotesters and RF detectors for series 54XXA systems are described fully in the 54XXA Operation Manual.

The CW frequency accuracy of the signal sources of the RF models is $\pm 100 \mathrm{kHz}$ ( $\pm 200 \mathrm{kHz}$ below 10 MHz ). The CW frequency accuracy for the microwave models is $\pm 200 \mathrm{kHz}$. The standard RF power output for the RF models is +12 dBm to +2 dBm , and for the microwave models it is +10 dBm to 0 dBm ( +7 dBm to -3 dBm for model 5436A). Adjustment of the output power can be increased by the addition of an optional internal 70 dB step attenuator, which provides adjustment in 0.1 dB steps.

The analyzer section of the 54XXA is normally equipped with two measurement channels ( $A$ and $B$ ) as standard. The measurement range of each channel is +16 dBm to -63 dBm . An additional channel $(R)$ is available as an option. The $R$ channel is equal in performance to channels $A$ and $B$ and may be used as a reference channel when performing ratio measurements. For a detailed description of the characteristics and specifications for all 54XXA models refer to the 54XXA Operation Manual.

4-3 54XXA MAJOR FUNCTIONAL BLOCKS

The major circuit blocks that comprise a 54XXA system are shown in Figure 4-1. As shown in the figure, the circuitry for each block may be located on multiple printed circuit boards, or assemblies, that are located throughout the 54XXA. Refer to Figure 4-1 while reading the functional descriptions of these circuit blocks on the following pages.

Central Proc- The central processor is the heart of the 54XXA and essor coordinates all of its functions. This controller is an

8 -bit microprocessor that is mounted on the A7 CPU PCB. It directly or indirectly controls all measurement functions, display functions, and any input/ output functions that are being performed by the 54XXA. It is directly linked via a dedicated data and address bus to the A8 Graphics System Processor PCB, the A6 ALC/F requency Instruction PCB, the A5 YIG Driver/Signal Channel Interface PCB, the A3 Signal Channel PCB, and the A1/A2 Front Panel PCB's.

54XXA User Interfaces

The standard operator interfaces to the 54XXA central processor are the front panel control keys and the function menus displayed on the internal CRT monitor. The control keys, indicator LED's, and associated circuitry are located on the A1 and A2 PCB's.

Option 3 to the 54XXA adds interface and control circuitry for the IEEE-488 Interface Bus (GPIB) to the A7 PCB. This option allows the 54XXA internal processor to be controlled remotely by an external computer/controller running a suitable control program. The over 400 device-specific GPIB commands recognized by the 54XXA firmware are described and explained in the 54XXA Series Scalar Measurement Systems GPIB User's Guide.


Figure 4-1. Overall Block Diagram of Typical 54XXA Scalar Network Analyzer

## Graphics Processor Sub-System

The graphics processor circuitry located on the A8 Graphics System Processor PCB generates the various elements that make up the screen display presented on the internal VGA monochrome monitor. Similarly, it produces the screen display signals that drive an external VGA col or monitor. It also formats and controls the output to the Centronics printer interface.

The graphics processor circuitry is controlled by the graphics system processor, which is a dedicated microprocessor located on the A8 PCB. The functions of this controller (and subsystem) are controlled and coordinated indirectly by the (A7) Central Processor using high level commands.

The output frequency and power level of the 54XXA signal source are controlled by the central processor by control latches and DACs located on the A6 ALC/ Frequency Instruction PCB. The ALC level control circuits on this PCB generate analog control signals that are fed to the RF deck. For microwave models, the Control Modulator produces the desired output power level. F or the RF models, the control modulator circuitry contained in the Down Converter performs this function.

A portion of the RF output is detected by an internal RF detector. The detector output signal is used as feedback to the ALC circuits to maintain the desired output level at all output frequencies. Option 6 adds a rear panel External ALC Input connector that allows using an external RF detector for leveling.

The frequency control information is converted to an analog signal on the A6 PCB and fed to the YIG driver circuitry located on the A5 YIG Driver/Signal Channel Interface PCB. These circuits generate the appropriate control signals that cause the YIG tunedoscillator to produce the desired output frequency.

The YIG-tuned oscillator, Control Modulator, Directional Coupler, and other devices that generate and control the signal source RF output signal are located on the RF deck assembly. This assembly is mounted on the right hand side of the 54XXA and can easily be removed as a complete unit for service work. The functioning of the RF deck is explained in detail in later paragraphs.

## Measurement Channel Signal Processing

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A9 Power Supply Assembly
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The low-level analog signals from the external SWR Autotester(s) and/or detectors used with the 54XXA are fed from the front panel input connectors to the A3 Signal Channel PCB. This PCB is positioned behind the input connectors and underneath the RF deck in a screened metal cage.

The standard A3 PCB contains measurement channel circuitry that is multiplexed to provide two measurement channels, $A$ and $B$. This circuitry is basically an analog signal conditioner that amplifies and filters the DC signal voltage(s) from the front panel input(s).

Option 5 adds a third "reference" measurement channel ( $R$ ). The $R$ measurement channel circuitry is totally separate from the main measurement channel, which allows accurate ratio measurement to be made.

The outputs from the main and (optional) R channel circuits are fed to the A5 YIG Driver/Signal Channel Interface PCB. These signals are multi plexed onto the input of a 12 -bit analog-to-digital converter. The resultant digital information is fed to the A7 Central Processor PCB and processed into finished measurement data to be displayed or printed.

The 54XXA power supply assembly produces all of the DC voltages used by the 54XXA printed circuit boards, RF deck components, rear panel fan, and CRT monitor assembly. The operation of the power supply circuitry is explained in detail in later paragraphs.

Motherboard and Rear Panel

The A4 M otherboard Assembly and associated cables provide the data bus interconnections, signal paths, and DC voltage busses that link all of the 54XXA printed circuit boards and other major assemblies.

The rear panel includes connectors for the External VGA M onitor, GPIB/IEEE-488 Instrument Interface, Centronics Parallel Printer Interface, External ALC Input, and Horizontal (Sweep) Output. The cables associated with these connectors connect to the A4 M otherboard, which distributes the various signal paths to the appropriate 54XXA circuitry. The wiring/cable assembly associated with the rear
panel line voltage module connects it directly to the power supply module.

A7 CENTRAL PROCESSOR PCB

The A7 PCB contains the central processor circuits, driver circuits for the (optional) 70 dB attenuator, and for the Switched Filter that is part
of the RF Deck of models 5417A, 5419A, 5437A, and 5447A. The A7 PCB also contains the circuits for the IEEE-488/GPIB Interface Bus if the 54XXA has Option 3 installed. A block diagram of these circuits is shown in Figure 4-2.

## Central Processor Circuits

The 54XXA central processor is implemented using an Intel 8088 microprocessor. In addition to the mi-
croprocessor, the following circuits are used:
$\square$ A clock chip and crystal oscillator that generate and control the clock signal to the microprocessor
$\square$ Three 1 Mbit EPROMS that store operating firmware
$\square$ A 1 Mbit RAM that stores calibration data, trace data, stored set ups, and unit identification information
$\square$ Address latches and buffers that interface the microprocessor to the internal memory
$\square$ Bi-directional data buffers that transfer data to/from the microprocessor and the internal address and data buses. Similar circuits transfer data to/from the external data, address, and interrupt buses that connect to the other PCB's in the 54XXA.
$\square$ Interrupt control and vectoring circuits
$\square$ A backup battery and control circuit that powers the RAM chip during power off conditions

When the 54XXA is powered up, the central processor is reset. It then performs the following initial operations:
$\square$ Runs the instrument self-test routine
$\square$ Reads the instrument model identification and configuration from the A6 PCB
$\square$ Down-loads the display software to the A8 Graphics System Processor PCB
$\square$ Sets up the unit with the last used front panel control configuration
$\square$ Starts normal instrument operation.

## Attenuator Driver Circuit

A control latch and four bi-polar output circuits comprise the drive circuits for the (optional) 70 dB step attenuator located on the RF deck. Each output circuit provides a 24 V reversible drive signal for one of the four stages of the attenuator. These circuits contain protection diodes that absorb the back EMF from the attenuator drive coils. The control latch is controlled by the central microprocessor via the internal data and address buses on the A7 PCB.


Figure 4-2. Block Diagram of A7 Central Processor PCB

| Switched | The Switched Filter Control latch provides the five <br> Filter <br> Control <br> Circuit |
| :--- | :--- |
|  | RF deck (used on models 5417A, 5419A, 5437A, and <br> 5447A). This latch is controlled by the central micro- <br> processor via the internal data and address buses on <br> the A7 PCB. |
| GPIB | Two GPIB data bus transceiver chips and a GPIB <br> circuits |
|  | controller chip comprise the (optional) GPIB inter- <br> face circuits (Figure 4-2). The transceiver chips con- <br> nect to the rear panel GPIB connector via the A4 <br> Motherboard and associated connector cable assem- <br>  <br>  <br>  <br>  <br>  <br> bly. The central microprocessor controls the GPIB <br> controller and passes data to/from it via the internal <br> data, address, and interrupt buses on the A7 PCB. |

## 4-5 <br> A8 GRAPHICS SYSTEM PROCESSOR PCB

The Graphic System Processor (GSP) circuits are located on the A8 PCB (Figure 4-3). These circuits comprise an intelligent subsystem that is loosely controlled by the A7 PCB Central Processor. It produces the video signals for the internal CRT monitor screen display and for the external VGA monitor interface. It also produces the data and control signals for the Centronics printer interface. There are no adjustments on this PCB.
$\begin{array}{ll}\text { Major GSP } & \text { The major circuit blocks that comprise the A8 } \\ \text { Circuits } & \text { Graphic System Processor PCB are: }\end{array}$
$\square$ Graphics controller chip (34010) - this controller interprets the commands from the A7 PCB Central Processor and produces appropriate command signals and data streams that produce the desired CRT monitor display or printer output. The GSP controller communicates with the GSP memory, video output circuits and printer interface circuits via the internal GSP Data Bus (Figure 4-3).
$\square$ Clock Signal Generation - The 40 MHz clock chip produces the INCLK signal that is used by the GSP controller to derive all program related timing signals. The controller divides this signal by eight to produce the LCLK2 signal that clocks data into and out of the GSP memory. The controller also produces other timing and control signals related to this clock.

## A8 GRAPHICS SYSTEM <br> PROCESSOR PCB

The video clock oscillator and associated divider circuits produce the 6 MHz video clock signal, VCLK. This signal is used to establish the rate that the video information is clocked from the GSP memory to the video output circuits.

## NOTE

For troubleshooting, all programrelated cycles should be observed synchronized to LCLK 2 (test point 2). All video cycles should be observed synchronized to VCLK (test point 3).
$\square$ Data interface circuits - these circuits interface the GSP processor to the data and address bus lines from the A7 central processor. The graphics processing control program is downloaded through this interface.


Figure 4-3. Block Diagram of A8 Graphics System Processor PCB
$\square$ Data "Pipe" - two latches form a data pipe that allows direct communication from the A7 central processor to/from the GSP processor via the GSP Data Bus (Figure 4-3).
$\square$ Video/Program Memory - four 256K x 4 Video Dynamic RAMs (VRAMs) comprise the memory for the GSP subsystem. This memory is used to store the GSP control program and the video data that will produce the CRT monitor screen display output.
$\square$ Video Output Circuits - Two shift registers, a video clock oscillator chip, a video mixer chip and a video amplifier/buffer circuit comprise the video output circuits. These circuits shift the video data out of the GSP memory and convert it into the Red, Green, and Blue signals for the VGA Monitor Interface and the mono-video signal for the internal CRT monitor.
$\square$ Centronics Printer Interface - A data buffer/ latch, a printer interface controller chip and a portion of a data latch comprise the interface circuitry for the Centronics printer interface. This circuitry provides the formatted data, data strobe, and control signals for the printer interface. It also receives and stores the status signals from the printer.

The GSP controller receives the graphics processing program down-loaded to it from the A7 Central Processor at power-up. It stores the GSP control program in the high memory locations of the GSP Video/ Program Memory and starts it on command from the central processor. (Low memory locations are used for video data.) The control program is run continuously until the 54XXA is powered-down.

The GSP control program controls all aspects of the operation of the GSP subsystem, which include:
$\square$ Timing of communication operations from/to the central processor
$\square$ Setting up the CRT scanning
$\square$ Generating and maintaining the graphic elements of the CRT display
$\square$ Formatting and control ling the data output to the Centronics printer interface

A preliminary step performed by the program is the setup of timing information for the video output signals. This operation places certain control codes into the A8 PCB internal registers. (At execution time, the contents of these registers are processed in the same manner as memory location data.) These codes control internal clock dividers that generate the required Horizontal and Vertical Synchronization signals for the output video signal. The Video blanking signal is also generated in this manner. The timing of these signals is compatible the VGA Standard, so that standard VGA monitors may be used with the 54XXA (rear panel EXTERNAL MONITOR interface connector).

The GSP control program causes the GSP controller to wait for instructions and data that are sent to it from the central processor via the pipe interface (Figure 4-3). The commands used by the central processor to control the GSP are high level commands such as draw line and write text The GSP controller translates these commands into primitive instructions which it can directly execute. It then performs the necessary sub-tasks to produce the desired results.

F or example, the command draw line performs the following operations: It generates primitive commands that instruct the GSP controller to produce a series of memory fetch cycles from the video data stored in the low memory locations of the GSP memory. After each fetch, it modifies the video data and returns it to memory. This process alters the contents of video memory so that when the memory contents are displayed on the CRT monitor, the desired line appears. The GSP controller performs these graphic memory fetch cycles interleaved with control program fetches from the high memory locations of the GSP memory.

The GSP control program does not control the overall content of the CRT monitor display - it produces graphic elements and puts them into video memory as instructed by the central processor. The central processor controls the content and placement of the graphic elements that make up the display. After the video information for a complete screen display has been built up in memory (as explained above), it is shifted out to the video output circuits.

| Printer <br> Interface Operation | The GSP processor sends formatted printer output data and control signals to the printer interface circuits via the GSP data bus. The printer interface controller chip provides the data strobe that clocks the output data from the GSP bus into the data buffer/ latch (Figure 4-3). It also provides the LSTB (strobe) and PRINTER RESET signals to the printer. Along with associated data latch circuits, it receives the printer status signals and sends them to the GSP controller via the GSP bus. |
| :---: | :---: |
| Video Output Circuit Operation | The 24 MHz signal from the video clock oscillator is divided down and gated by divider circuits and the video mixer chip to produce the video dot-rate clock signal, VCLK. This signal and other clock signals from it are used to transfer the video data out of the GSP memory and shift it into the video mixer chip. This chip converts the video data signals into a combination of Red, Green, and Blue signals that are output to the External VGA M onitor interface. These signals are mixed to produce a composite monochrome signal that is fed to the input of the video buffer amplifier. This amplifier boosts the signal to the 3 to 5 V level required to drive the internal CRT monitor. |
| Internal CRT Monitor | The video and synchronization signals from the A8 Graphics System Processor PCB and the required DC power are fed to the CRT monitor by a cable assembly that connects to the A4 Motherboard PCB. The monitor is not field repairable and should be replaced with an exchange unit if defective. |

## NOTE

The adjustment potentiometers for these units are set at the factory and should require no further adjustment. Any adjustment of these potentiometers or of the CRT geometry magnets should not be attempted.

4-6
A6 ALC/FREQUENCY INSTRUCTION PCB

The circuitry contained on the A6 ALC/F requency Instruction PCB (Figure 4-4) generates control signals that perform the following functions:
$\square$ Sets the RF power output level of the 54XXA internal source to the value instructed by the A7 Central Processor.
$\square$ Maintains the RF output power level flat throughout the selected operating frequency range.
$\square$ Sets the frequency of the internal source to the value instructed by the A7 Central Processor.

- Maintains the RF output frequency at the selected values.

In addition, the A6 PCB contains circuits that allow the A7 Central Processor to read the 25 MHz and 500 MHz marker signals that are generated on the RF Deck. (This information is used to create frequency correction data that is fed back to the A6 PCB.) It al so contains a Unit Identification Circuit that is read by the A7 Central Processor at power-up to determine model type and configuration.


Figure 4-4. Overall Block Diagram of A6 ALC/ Frequency Instruction PCB

## ALC Circuit Operation

## ALC Circuit Groups

The ALC circuits control the RF power output level and flatness of the internal source. These circuits receive instructions and data from the A7 Central Processor PCB and convert them into a voltage that represents the desired output level. This voltage is converted into control currents that drive the PIN attenuator circuits located in the control modulator on the RF deck. These circuits attenuate the signal from the YIG-tuned oscillator to the desired level.

## NOTE

The RF output level is controlled by the internal control modulator circuits located in the down converter in models 5407A, 5409A, and 5411A.

The source output is maintained at the desired level by the servo action of the ALC control circuits, which use the output signals from detectors located in the down converter and directional coupler as negative feedback. Option 6 to the 54XXA provides a rear panel external ALC input connector for use with a suitable external RF detector. This feature allows the RF output to be leveled at points in the external test path instead of internal to the 54XXA.

The circuit groups listed below comprise the ALC circuitry located on the A6 PCB. These circuits are described in following paragraphs. See block diagrams in Figure 4-4 and Figure 4-5 (on page 4-19).
$\square$ Power Level Set
$\square$ Control Modulator driver circuits
$\square$ Down converter modulator driver circuits
$\square$ Internal Leveling
$\square$ External Leveling
$\square$ Quiet Data Bus
The RF power level information from the A7 Central Processor PCB is transferred to the power control DAC and to the temperature compensation circuit DAC by the quiet data bus on the A6 PCB (Figure 4-5). The input to the power control DAC is an frequency sweep voltage derived from the main coil and $F M$ coil drive signals. The input to the temperature compensation circuit DAC is either the feedback voltage from the down converter thermistor or the directional coupler thermistor (as selected by the A7 Central Processor).

## Control Modulator Driver Circuits

Down
Converter
Modulator
Driver
Circuits

YIG PIN
Switch

## Driver

Circuit

The output voltages from the two DAC's are summed with the feedback voltage from the internal (or external) ALC detectors to produce the ALC LEVEL control signal. This signal represents the desired RF output level and is the input to the Control Modulator and Down Converter modulator driver circuits.

The Control Modulator controls the RF output power level above 2.0 GHz (see note above). There are two circuits located on the A6 PCB that drive the control modulator (Figure 4-5). The Mod Bias Circuit drives the control modulator PIN switches that switch the RF power on and off. The state of this circuit is switched by commands from the A7 Central Processor PCB.

The second circuit, Mod Control, drives the control modulator PIN switches that control the RF power output level. This circuit is activated by commands from the A7 Central Processor PCB and controlled by the output of the power level set circuits. Potentiometer R133 in this circuit controls the circuit bandwidth. It is adjusted during circuit alignment to assure that no oscillation of the driver circuit occurs.

The down converter controls the RF output power level in models 5407A, 5409A, and 5411A. (The down converter also performs this function in models 5417A and 5447A for output frequencies below 2.0 GHz ). The two A6 PCB driver circuits that control the down converter PIN modulators are similar in operation to those described above for the Control Modulator (Figure 4-5). These circuits are selected by commands from the A7 Central Processor PCB as appropriate for the model and output frequency selected. Potentiometer R112 in the M od Control driver circuit controls the circuit bandwidth. It is adjusted during circuit alignment to assure that no oscillation of the driver circuit occurs.

The YIG-tuned oscillators used in M odels 5407A, 5409A, and 5411A contain a PIN switch circuit that attenuates the RF signal on and off. The YIG PIN Control driver circuit for this function is located on the A6 PCB (Figure 4-5). The state of this circuit is switched by commands from the A7 Central Processor PCB.

## Internal Leveling Circuits

The source RF output is leveled by a closed feedback loop. For microwave band models 5417A through 5447A, the ALC feedback signal is produced by a directional detector located on the RF deck. F or models 5407A, 5409A, and 5411A, (and for models 5417A and 5447A at output frequencies below 2.0 GHz ), the feedback signal is produced by a detector located in the down converter.

The internal ALC feedback signals are conditioned by two separate amplifier chains, one for above 2.0 GHz and one for below 2.0 GHz . The outputs of these circuits are switched to the ALC summing point amplifier by commands from the A7 Central Processor PCB, as appropriate for the model and output frequency selected.

The overall output RF power of the source is controlled by adjusting the amount of feedback supplied to the ALC loop by these amplifier chains. During circuit alignment, potentiometer R62 is used to adjust the upper power level output in the $>2.0 \mathrm{GHz}$ amplifier chain. The low power output is adjusted by R196. Potentiometer R56 is the high power output adjustment and potentiometer R190 is the low power output adjustment in the $<2.0 \mathrm{GHz}$ amplifier chain.

## External Leveling Circuits

The signal voltage from the (optional) rear panel EXTERNAL ALC INPUT connector is fed to signal conditioning circuits that include an absolute value circuit. The absolute value circuit ensures that a signal with the correct polarity is fed to the input of the ALC Scaling DAC.

To allow external RF detectors with different voltage outputs to be used, a method of calibrating the external ALC input signal is required. This operation is controlled by commands from the A7 Central Processor PCB, as follows:
$\square$ The external detector feedback signal from the scaling DAC is compared with the feedback voltage generated by the internal ALC detector.
$\square$ The central processor causes the External ALC Scaling DAC to adjust the amplitude of the external detector signal until it is equal to the internal detector voltage.
$\square$ The resultant external ALC signal is then switched to the ALC summing point amplifier.

## "Quiet" Data Bus Circuits

This bus is used to transfer data between the A6 PCB data latch circuits and the Frequency Instruction DAC's and Power Level Control DAC's (Figure 4-4). The quiet data bus is buffered from the A7 Central Processor Data Bus to insulate these circuits from noise on the main bus.


Figure 4-5. Block Diagram of ALC Power Control Circuits

## Frequency Instruction Circuits Operation

## Frequency Instruction Circuit Groups

RAMP DAC Circuits

The frequency instruction circuits located on the A6 PCB control the frequency of the 54XXA RF output signal. These circuits receive instructions and data from the A7 Central Processor PCB and convert them into control signals for the YIG-tuned oscillator main coil and FM coil drive circuits that are located on the A5 YIG Driver/ Channel Interface PCB (Figure 4-7 on page 4-23).

The two main output signals from the frequency instruction circuits are Main Coil Sweep and FM Coil Sweep. E ach is a composite signal that is normally comprised of variable DC and ramp elements. (The ramp element is not present for CW operation.) These circuits also produce a sweep ramp signal that is fed to the rear panel HORIZONTAL OUTPUT connector and a frequency compensation signal that is fed to the ALC control circuits.

The four circuit groups that comprise the frequency control circuits are: RAMP DAC, WIDTH DAC, CENTER DAC, and ERROR DAC. Each circuit group contains a 12-bit DAC and associated operational amplifiers and control circuits (Figure 4-7). Each of these circuits receive data from the A7 Central Processor PCB via the A6 PCB quiet data bus (Figure 44). The control signals for these circuits are produced by data latches on the A6 PCB that are controlled by the Central Processor data bus.

The A7 Central Processor sequentially programs the RAMP DAC, thereby producing a ramp output signal containing 4000 steps. This ramp signal is fed to the WIDTH DAC and is further modified to produce either the Main Coil Sweep signal or the FM Coil Sweep signal. The ramp signal is also buffered and fed to the rear panel HORIZONTAL OUTPUT connector.

The signal produced by the RAMP DAC always has the same voltage range (number of steps) when the 54XXA is sweeping, regardless of the selected sweep width. The A7 Central Processor may halt the update of the DAC at any time (e.g., when dealing with interrupts, etc.). This will produce steps of varying duration, which will produce a ramp with a shape that is irregular rather than smooth and continuous. However, this does not effect the displayed sweep in any way.

## WIDTH DAC Circuits

## CENTER DAC Circuits

The input to the WIDTH DAC is the ramp signal output by the RAMP DAC. The WIDTH DAC output is a ramp signal with a magnitude that is scaled by the data it receives from the A7 Central Processor. Thus the ramp signal is scaled, under control of the central processor, to produce a sweep signal that will tune the YIG oscillator over the required range.

## For example:

To produce a sweep over half the maximum range of the 54XXA, the A7 Central Processor programs the WIDTH DAC to output a ramp with an amplitude that is half of the DACs' maximum range. The input to the WIDTH DAC is a 0 V to - 10 V ramp; therefore, the output signal will be a 0 V to +10 V ramp.

F or sweep widths greater than 40 MHz , the drive signal is applied to the main coil of the YIG-tuned oscillator. F or sweep widths of 40 MHz or less, the drive signal is applied to the FM coil of the YIG-tuned oscillator. This signal switching is performed by analog switches that transfer the WIDTH DAC output signal to either the Main Coil Sweep or FM Coil Sweep signal output circuits (Figure 4-7). These switch circuits are controlled by commands from the A7 Central Processor.

A proportion of the WIDTH DAC output signal is fed to the 25 MHz marker generator circuits located on the RF deck. This signal ensures that the marker width remains constant throughout the full frequency range of the unit.

The output of the CENTER DAC circuit is a DC voltage in the range of 0 to +10 V that is controlled by the A7 Central Processor. This signal is summed with the WIDTH DAC ramp signal at the input to the Main Coil Sweep circuit, thereby controlling the DC component of the composite Main Coil Sweep signal. This allows the A7 Central Processor to set the center frequency of the sweep range to the desired value.

ERROR DAC The output of the ERROR DAC circuits is a DC voltCircuits
age that is used as a frequency source lock error correction signal. The A7 Central Processor sets the magnitude and polarity of this signal using error information obtained by processing the 500 MHz and 25 MHz marker read signals from the A6 PCB.

The output of the ERROR DAC circuit is a DC voltage in the range of -10 to +10 V . This signal is fed through a summing resistor to the input of the FM Coil Sweep signal output circuit, thereby controlling the DC component of the composite FM Coil Sweep signal. The DC signal component causes the YIG FM coil to produce a frequency offset that cancels the frequency error. For sweep widths of 40 MHz or less, the WIDTH DAC ramp signal is summed with the error signal at the input of the FM Coil Sweep signal output circuit.

## 500MHz and 25 MHz Markers Read Circuits

The 500 MHz and 25 MHz marker signals that are generated by the marker modules on the RF deck are read by the encoder circuits located on the A6 PCB. The outputs of these circuits are stored in a data buffer latch that is read by the A7 Central Processor. This information is used by the Central Processor to generate the frequency source lock error correction data that is feed back to the ERROR DAC.

This circuit consists of an 8 position jumper block (J 3), a bank of 8 pull-up resistors, and an 8 -bit latch, as shown in Figure 4-6. An open jumper in any position will be sensed by the associated latch input as a logic one and a closed jumper will be sensed as a logic zero. The jumpers are configured at the factory to identify the unit model type and configuration. The outputs of the data latch are read by the A7 Central Processor at power-up.


Figure 4-6. Unit Type Identification Circuit


Figure 4-7. Block Diagram of A6 PCB Frequency Instruction Circuits

A5 YIG DRIVER/ SIGNAL CHANNEL INTERFACE PCB

There are two YIG-tuned oscillator coil driver circuits located on the A5 PCB: the Main Coil Driver and the FM Coil Driver. These circuits receive the YIG Main Coil and FM Coil control signals from the A6 ALC/F requency Instruction PCB and convert them into the drive currents for the YIG tuning coils.

The circuits that interface with and control the A3 Signal Channel PCB are also located on the A5 PCB. These circuits receive commands from the A7 Central Processor PCB and generate appropriate control signals to the A3 Signal Channel PCB. They receive the multiplexed measurement signal from the A3 Signal Channel PCB, digitize it, and send the resultant data to the A7 Central Processor via the central processor data bus. They also process the status signals from the A3 PCB and send appropriate status signals back to the to the Central Processor. These circuits are described in later paragraphs in this chapter.

YIG Driver Operation

The YIG-tuned oscillator requires current drive to its coils to create the magnetic fields that cause oscilIation. The operating frequency of the YIG is controlled by adjusting the magnitude of the currents sent to these coils. The main coil of the YIG provides the main magnetic field and requires a drive current with a single polarity. The YIG can be swept over its entire frequency range by varying the magnitude of the main coil current in an appropriate manner.

The FM coil has a more limited frequency range and a higher sensitivity. It can be driven in either direction so that its magnetic field either augments or diminishes the main coil field. By this means fine control of the YIG output frequency is achieved.

The Main Coil Control and FM Coil Control signals from the A6 ALC/F requency Instruction PCB are voltages. The YIG Driver circuits on the A5 PCB provide the necessary voltage to current conversion (and power amplification) to drive the YIG coils. Both coil driver circuits are designed to drive floating loads.

## Main Coil Driver Circuit

Figure 4-8 is a block diagram showing the YIG Main Coil driver and FM Coil driver circuits. The input to the main coil driver circuit is the Main Coil Control signal from the A6 PCB. This signal is a voltage in the range of 0 to -10 V . The resultant output is a drive current that flows in one direction only.

When the 54XXA is in the CW mode, or sweeping using the FM coil, the bandwidth of the Main coil driver is reduced by switching a low-pass filter into the driver circuit. This results in reduced noise and residual FM on the RF output.


Figure 4-8. Block Diagram of YIG Driver Circuits

When the 54XXA is sweeping using the FM coil, the rapidly changing field causes a voltage to be induced in the main coil. This effect (and the action of the low-pass filter) causes a frequency shift to occur. To counteract this, a linearization transformer is used to couple some of the FM coil drive signal into the main coil driver circuit. This signal causes a field in the main coil that cancels out the frequency shift error.

Potentiometer R42 provides adjustment of the YIG oscillator lower frequency limit, and potentiometer R56 provides adjustment of the total sweep range. These potentiometers are adjusted during circuit alignment of the unit.

To match the characteristics of the various YIG driver assemblies used in different 54XXA models, the values of various coil driver components are different. This is reflected in the different part numbers of the A5 PCB's used (see Chapter 2).

The Main coil sensitivity of YIG-tuned oscillators varies somewhat from band to band but is of the order of 20 to 30 MHz per mA. The Main coil driver therefore must supply over 1.2A when driving a high frequency YIG-tuned oscillator.

FM Coil Driver Circuit

The input to the FM coil driver circuit is the FM Coil Control signal from the A6 PCB. This signal is a voltage in the range of +10 to -10 V . The resultant output is a drive current that flows in either direction, depending upon the input signal.

The FM coil sensitivity of YIG-tuned oscillators is in the range of 300 to 450 kHz per mA . The maximum frequency range covered is normally $\pm 60 \mathrm{MHz}$. Therefore, the FM coil driver is required to supply up to $\pm 200 \mathrm{~mA}$ maximum.

## Signal Channel Interface Circuits

Figure $4-9$ is a block diagram of the signal channel interface circuits located on the A5 PCB. The major circuit blocks that comprise these circuits are:
$\square$ Sample-and-Hold
$\square$ Analog-to-Digital Converter
$\square$ Detector Recognition
$\square$ Address Decode
$\square$ Quiet Data Bus

## Sampleand-

 Hold CircuitsThere are two separate sample and hold circuits, one for the A/B channel measurement signal and one for
the $R$ channel measurement signal. Both circuits are identical. The ANALOG A/B input signal from the A3 Signal Channel PCB contains time multiplexed signals for the $A$ and $B$ channels (if both are active). This includes the measurement signals, Log Conformity signals, and Temperature (detector thermistor) signals. (These signals are multiplexed by circuits on the A3 PCB under control of the A7 Central Processor.) Similarly, the ANALOG R input signal contains the multiplexed signals for Channel R. This signal is active only if the 54XXA is equipped with Option 5, and the R Channel is selected as active.

Both input signals are fed to the A5 PCB inputs via a shielded cable. Differential amplifiers are used in the inputs of these circuits to ensure good common mode noise rejection. The outputs of the sample and hold circuits are fed to the input of the Anal og-toDigital Converter (ADC). The ADC circuit converts only positive polarity signals (negative polarity signals are ignored). Therefore, the sample and hold circuits are designed to add a 100 mV positive offset to the measurement signal. The A7 Central Processor automatically subtracts this offset when processing the measurement signal data.

Analog-toDigital Converter Circuit

The output of each sample and hold circuit is fed to the input of the Analog-to-Digital Converter circuit via an analog switch. These switches are controlled by the A7 Central Processor and programmed so that only one switch is active at any given time. The 12 bit output of the ADC is stored by two data latches and then transferred to the A7 Central Processor in two 8-bit bytes.

| Detector Rec- <br> ognition Cir- <br> cuits | The A, B, and R Detector Sensed signals from the <br> A3 Signal Channel PCB are buffered and then <br> stored in a data latch that outputs to the quiet data <br> bus. This allows the A7 Central Processor to deter- <br> mine if a particular channel input has a RF detector <br> or Autotester connected. The three detector sensed <br> signals are also OR'd to produce a status signal that <br> is read by the A7 Central Processor before reading <br> the output of the ADC. If this status signal if false <br> (no input connected) an error interrupt occurs. |
| :--- | :--- |
| Address De- | The address decode circuits located on the A5 PCB <br> produce control signals and data strobes that control <br> the various circuit functions on the A3 Signal Chan- |
| code And |  |
| Data Latch |  |
| Circuits | nel PCB and locally on the A5 PCB. These circuits <br> decode the instrument address lines and I/O select <br> lines from the A7 Central Processor bus to produce <br> the control signals and data strobes. The timing of <br> these signals is controlled by the A7 Central Proces- <br> sor. |
| Quiet Data | The A3 Signal Channel and A5 Signal Channel Inter- <br> face communicate via a quiet data bus. This bus is |
| Bus Circuits |  |
| also used to transfer data between circuits on the A5 |  |



Figure 4-9. Block Diagram of Signal Channe InterfaceCircuits

A3 SIGNAL CHANNEL PCB

The standard A3 Signal Channel PCB has two measurement signal inputs, $A$ and $B$. The signals from these inputs are multiplexed together by an input switching circuit and then fed to an amplifier chain (Figure $4-13$ on page 4-35). The resultant A/B measurement signal is filtered and then fed to the output multiplexer circuits. These circuits multiplex the measurement signal with the Log Conformity and Temperature Sense signals from the A and B input connectors. The resultant output signal is then fed to the A5 YIG Driver/Signal Channel Interface PCB where it is digitized and the data sent to the A7 Central Processor.

If the 54XXA is equipped with Option 5 , the A3 will also include a third measurement signal input ( R ). The signal channel circuits associated with this input are identical to those for the A/B channel, except they do not include an input switching circuit.

Channel Input Circuits

The Detector/Auto Tester output signals from the front panel input connectors are fed to the Channel A, B, and (optional) R input circuits on the A3 PCB. These signals are typically low level DC signals that contain low-frequency AC components. The A and B input circuit includes two low-pass filter networks and a switching network comprised of FET switches. The output of this circuit is a time multiplexed signal that represents the measurement signals for Channels A and B. The R input circuit contains only a low-pass filter network.

Input Amplifier Circuits

An instrumentation amplifier and associated gain control and auto-zero circuits comprise the I nput Am- plifier circuit block (Figure 4-10). The gain of this amplifier is set to either $x 1, \times 10$, or $\times 100$, by the action of the gain control circuit, which is controlled by signals from the A5 YIG Driver/Signal Interface PCB. Potentiometers R199 and R201 are the x10 and x 100 gain adjustments, respectively. They are adjusted during circuit alignment.

## Variable Gain Amplifier Circuits

The variable gain amplifier block consists of four operational amplifiers that provide an overall programmable gain of one to ten thousand. The gain control circuit associated with these amplifiers is also controlled by signals from the A5 PCB. Potentiometer R118 is the overall gain adjustment for these circuits. The variable gain amplifier block combined with the input amplifier circuit comprise an amplifier chain that has an overall programmable gain of one to one million, programmable in factors of ten (x1, x10, x100...).

Auto-Zero Circuits

When the amplifier chain is operated at high gain settings, the errors due to overall amplifier DC offset and wide band noise from the internal RF source must be eliminated. An autozero circuit is used to perform this function. This circuit consists of a Zener diode DC voltage source, a DAC integrated circuit, and associated operational amplifiers. The output of this circuit is fed to a separate input on the instrumentation amplifier. Identical circuits are used for the Channel $A / B$ and Channel $R$ amplifier chains.

The autozero nulling procedure is performed under control of the A7 Central Processor at the end of each frequency sweep, as follows:
$\square$ The amplifier chain is set to maximum gain and the DC offset is measured (by the A5 PCB).
$\square$ The autozero circuit is programmed to produce a voltage that will cancel out the offset error.
$\square$ The resultant compensation voltage value is used for subsequent measurements during the next sweep.


Figure 4-10. Block Diagram of Signal Channe Input Switching and Amplifier Chain Circuits

## Smoothing Circuits

The output signal from the amplifier chain contains appreciable high frequency noise when processing low level input signals. To reduce this noise, five levels of filtering can be applied by the A3 PCB smoothing circuit. This circuit consists of a programmable RC filter network shown in Figure 4-11.

Resistor R148 is permanently connected in the signal path of this circuit. When Smoothing Level 1 (minimum) is selected, a capacitor is connected from the output end of R148 to ground. A separate capacitor is used for Channel A measurements (C38) and another for Channel B (C39). These capacitors are connected by anal og switches that are controlled by the A7 Central Processor.

The other four levels of smoothing are achieved by switching resistor R155, 154, 153, or 152 in parallel with R148. The output of the smoothing circuit is fed to the input of the output multiplexer circuits ( Fig ure $4-13$ on page 4-35). The Channel $R$ smoothing circuit contains only one filter capacitor.


Figure 4-11. Signal Channel Smoothing Circuit

Log Conformity Circuits

WILTRON RF Detectors and Autotesters have a built-in resistance that is set at the factory to match the log characteristic of the detector diode used. The Log Conformity Sense circuits (Figure 4-12) convert this resistance value into a voltage value. Variable resistor R108 is used to calibrate the Input A log conformity circuit with a "standard detector" connected to the front panel INPUT A connector. Variable resistor R109 performs the same function for the I nput B log conformity sense circuit.

The outputs from the $A$ and $B$ log conformity sense circuits are read by the ADC circuit on the A5 YIG Driver/Signal Channel PCB (via the output multiplexer circuits). The resultant log conformity data is read by the Central Processor and used by it when processing measurement data.


Figure 4-12. Block Diagram of Log Conformity and Temperature Compensation Circuits

The output from each log conformity sense circuit is also fed to an associated comparator circuit. The output of the comparator is used as a status signal that indicates that a RF detector or Autotester is connected to the associated input. These signals are fed to the A5 PCB and are included along with other status bits read by the Central Processor. The log conformity and detector connect sense circuits for Input R are identical to those for Inputs A and B.

| Temperature | Also contained in the RF detector/Autotester is a |
| :--- | :--- |
| Sense | thermistor, which is used to sense the working tem- |
| perature of the detector diode (Figure 4-12). The re |  |
| circuits | sistance value of the thermistor is converted to a <br> voltage and read in the same manner as for the log <br> conformity resistor. The resultant temperature sens- <br> ing data is read by the Central Processor and used <br> by it when processing measurement data. The tem- <br> perature sensing circuits for Inputs A, B and R are <br> identical. |

## Output Multiplexer Circuits

## Control Latch Circuits

The output multiplexer circuit for Channels A and B consists of five solid state relay switches and an operational amplifier. This circuit switches the five signal lines listed below onto a single signal path (ANALOG A/B) that is fed to the inputs of the sam-ple-and-hold circuits on the A5 PCB. The five signal lines multiplexed are:
$\square A / B$ measurement signal
$\square$ A Log Conformity Value
$\square$ A Temperature Sense Value
$\square$ B Log Conformity Value
$\square$ B Temperature Sense Value
The quiet data bus lines, control signals, and data strobes from the A5 YIG Driver/Signal Channel PCB are fed to five control latches on the A3 PCB. The outputs of these latches form the control lines and data strobes that control all the circuit functions on the A 3 PCB .


Figure 4-13. Overall Block Diagram of A3 PCB Signal Channe Circuits

The Front Panel Assembly circuitry is contained on three printed circuit boards: the A1 Front Panel PCB, the A2 Front Panel Interface PCB, and the A10 Menu PCB Assembly (Figure 4-14). These circuits form a subsystem that performs the following functions:
$\square$ Detects Control Key closures
$\square$ Generates Interrupt for key closure

- Identifies Control Key that was pressed
$\square$ Detects Data Entry Knob rotation
$\square$ Generates Interrupts for Data Entry Knob CW and CCW rotation
$\square$ Receives and stores drive data for front panel LED indicators
$\square$ Drives front panel LED indicators
The A1 Front Panel PCB is mounted on the rear surface of the front panel and contains the control key switches and indicator LED's for the main portion of the front panel. In all, 42 switches and 16 LED's. The switches are of single pole, membrane construction. The contacts of each switch are formed by two interleaved, gold plated PCB traces directly underneath the switch membrane. Depressing the control key cap flexes the membrane and forces it into contact with the PCB traces, thus closing the switch. The operation of the switch interface circuits is described in a following paragraph.


Figure 4-14. Front Pane Assembly Overall Block Diagram

The A10 Menu PCB contains the six control key switches and one LED indicator that are located on the lower portion of the front panel. (The POWER switch is a separate assembly.) These switches are membrane type switches identical to those on the A1 PCB.

The A2 Front Panel Interface Board provides the interface between the A7 Central Processor and the A1 and A10 front panel PCBs. The main circuit blocks on this PCB are:
$\square$ Keyboard interface
$\square$ LED indicator data latches and driver circuits

- Data Entry Knob interface
$\square$ Address decode and control circuits
Keyboard The switches on the A1 PCB are connected into a Interface two-dimensional matrix consisting of eight X-lines Circuits and eight Y-lines (Figure 4-15). Each switch point forms a unique $X / Y$ coordinate (i.e., address); however, only 48 of the 64 possible X-Y combinations are used for switch positions. Closing any switch connects one of the $Y$-lines to one of the $X$-lines. Three of the $X$-lines and two of the $Y$-lines of the matrix are also routed to the six control key switches located on the A10 Menu Board.


Figure 4-15. Control Key Matrix and Decode Circuits Block Diagram

The switch controller/decoder circuit on the A2 PCB sequentially pulses the eight $X$-lines and also monitors each of the eight Y -lines for the presence of pulses. A pulse detected on a $Y$-line signifies a switch closure, which causes the controller/decoder circuit to send a Control Key Interrupt signal to the A7 Central Processor. The unique switch address determined by the X -line/ Y -line combination is output from the controller/decoder circuit as a data byte onto the Central Processor Data Bus. Upon receiving the interrupt, the Central Processor reads the address byte to determine which key was pressed.

```
LED Indicator Latch Circuits
```

The 16 LED indicators located on the A1 and A10 PCB's are controlled by latches on the A2 PCB (Figure 4-16). The Central Processor causes an individual LED indicator to be lit by writing a logic one into the latch bit associated with the selected LED. A control strobe from the control decode circuit clocks the data into the data latches. Each latch output line contains a current limiting resistor for the associated LED.

The Data Entry K nob is fixed to the shaft of a small DC motor that is used as a generator. When the knob is rotated, the motor produces a DC voltage which is proportional to the speed of rotation. The polarity of the voltage indicates the direction of rotation of the knob. The output of the motor is connected to the Data K nob I nterface Circuits (Figure 4-16). The input portion of these circuits consists of two comparator circuits: one circuit that produces a pulse train for clockwise knob rotation, and a second circuit that produces a pulse train for counterclockwise knob rotation.

Data Entry Knob Interface

The pulse rate of the CW and CCW pulse trains is determined by the rate of knob rotation. These signals are fed to the Knob Interrupt Circuits, which produce the CW and CCW Interrupt signals that are sensed by the A7 Central Processor.

CPU The Address Decode Circuits located on the A2 PCB

## Interface

 Circuitsdecode the address lines of the Central Processor Data Bus to produce strobe signals that control the interface circuits located on the A2 PCB. These signals clock data from the data bus into the Keyboard Interface Circuit and the LED Indicator data/driver latches. They also control the clocking of interrupt signals and keyboard address data onto the data bus.


Figure 4-16. LED Indicator and Data Entry Knob Interface Circuits Block Diagram

A9 \& A16 POWER SUPPLY PCB's

The 54XXA power supply circuits consist of a half-bridge line rectifier coupled to a high efficiency DC/DC switching type power converter. These circuits produce the following output voltages:
$\square+5 \mathrm{~V}$ High Current Supply
$\square+12 \mathrm{~V}$ High Current regulated supply
$\square+12 \mathrm{~V}$ Low Current regulated supply
$\square+15 \mathrm{~V}$ regulated supply
$\square-15 \mathrm{~V}$ regulated supply
$\square-18 \mathrm{~V}$ regulated supply
$\square+22 \mathrm{~V}$ regulated supply
The power supply circuits are located on the A9 Power Supply M otherboard PCB, the A16 Power Supply Converter PCB, the rear panel assembly, and the front panel (Figure 4-17). In addition to the output voltages listed above, a +12 V Start-Up Power Supply is also included on the A9 PCB. This power supply is used internally on the A9 PCB.

## WARNING

Hazardous voltages are present throughout the switching power supply and at the front and rear panels. When performing maintenance, use extreme care to avoid electrical shock.

## Front and Rear Panel Components

## Power

Supply Motherboard PCB Circuits

The POWER ON/OFF switch is located on the front panel and connects to the A9 Power Supply Motherboard PCB. The line voltage selector module is located on the rear panel. It provides primary circuit switching for $115 \mathrm{~V} / 230$ Vac line operation and contains the fuses for operation at these voltages. The rear panel fan operates on 12 Vdc power, which it obtains from the A9 Power Supply Motherboard PCB.

The major circuits located on the A9 Power Supply Motherboard PCB are:
$\square$ Start-up Power Supply, transformer and regulator
$\square$ Line Circuit Rectifier/Doubler circuit
$\square$ Soft Start Control circuit
$\square$ Pulse Width Modulator and Control Amplifier circuits
$\square$ Over Current Sense, Over Voltage Sense and Shut Down Timer circuits
$\square+12 \mathrm{~V},+15 \mathrm{~V},-15 \mathrm{~V},-18 \mathrm{~V}$, and +22 V regulator circuits

## Power Supply Converter PCB Circuits <br> Power <br> Supply Circuits Operation

The major circuits located on the A16 Power Supply Converter PCB are:
$\square$ Switching Transistors
$\square$ Over-Current Sense
$\square$ Output Voltage Transformer
$\square$ Output Rectifiers
The switches contained within the line voltage selector module configure the primary windings of the Start Up Power Supply transformer for 115 Vac or 230 Vac operation, as selected.

The line voltage selector module switches also configure the line rectifier circuit as either a full wave voltage doubler ( 115 Volt line operation) or a full wave bridge rectifier ( 230 Volt line operation). The output voltages from the rectifier circuit in either mode will be +165 Vdc and -165 Vdc , which are fed to the DC isolator switching transistors on the A16 Power Supply Converter board.

The switching transistors alternatively switch +165 Vdc and -165 Vdc to the primary windings of the output transformer at a 55 kHz rate. The driving signals for these transistors are supplied by the Pulse Width Modulator (PWM) circuit on the A9 PCB. The drive signals are two pulse trains with a variable duty cycle that is determined by the output from the Control Amplifier circuit during normal operation. During power up (or fault recovery) operation, these signals are controlled by the Soft Start Control circuit. During a fault condition, they are controlled by the Shut Down Timer circuit.

The four secondary windings of the Output Voltage Transformer produce reduced voltages that are fed to rectifier and filter circuits also located on the A16 Power Supply Converter PCB. These circuits contain inductors that function as integrators. The output of the +5 V rectifier/filter is fed to the A9 PCB where it is sensed by the Control Amplifier. The action of the Control Amplifier and PWM circuits cause the +5 V output (and other power supply outputs) to be regulated to their correct values.

The outputs produced by the other three windings and associated rectifier/filter circuits are: +14 V , $+18 \mathrm{~V},-18 \mathrm{~V},-21 \mathrm{~V}$, and +25 V . These voltages are feed to the final regulator circuits on the A9 PCB.

The main input to the Control Amplifier is the +5 V output sense line. Any change in the +5 V output cause the control amplifier to force the PWM to change the duty cycle of the drive signals so that the +5 V power supply output is regulated back to +5 V .

At power up, the +12 V output of the Start-up Power supply is used to charge a capacitor. The voltage across the capacitor is sensed by the PWM circuit, which causes it to set the drive signal duty cycle for a minimum output from the +5 V supply. As the capacitor charges, the drive signal duty cycle increases, causing the +5 V output (and other power supply outputs) to gradually reach full operating value.

The Over-Current Sense circuit monitors the currents through the switching transistors, and the Over-Voltage Sense circuit monitors the output of the +5 V supply. The outputs of these circuits are inputs to the Shut Down Timer circuit. When activated by either of these inputs, the Shut Down Timer circuit generates a shut down signal to the PWM, which causes the switching transistors to turn off. The shut down signal has a duration of approximately one half second. When the Shut Down Timer circuit resets, the power supply soft starts, as described above. If the condition causing the shut down is still present, the circuit will generate another pulse and shut down the power supply again. This mode of operation will repeat until either the over voltage/current condition is removed or the line power is removed.

The final regulator circuits on the A9 PCB produce the +12 V HC (high current), +12 V LC (low current), $+15 \mathrm{~V},-15 \mathrm{~V},-18 \mathrm{~V}$, and +22 V power supply outputs. These regulator circuits are driven by the outputs from the A16 PCB as follows:
$\square$ The +12 V HC and 12V LC are driven by the +14 V supply.
$\square$ The +15 V regulator is driven by the +18 V supply.
$\square$ The -15 V regulator is driven by the -18 V supply.
$\square$ The -18 V regulator is driven by the -21 V supply.
$\square$ The +22 V regulator is driven by the +25 V supply.


Figure 4-17. Block Diagram of 54XXA

## 4-11 a4 моtherboard PCB

The M otherboard PCB provides interconnection between all the PCBs and assemblies in the 54XXA. The motherboard connects directly to the following:
$\square$ A5 YIG Driver/Signal Channel Interface PCB

- A6 ALC/Frequency Instruction PCB
$\square$ A7 Central Processor/GPIB PCB
$\square$ A8 Graphics System Processor PCB
The motherboard distributes the various power supply voltages throughout the 54XXA. It connects to the A1/A2 and A3 PCB's, power supply PCB, RF Deck, and rear panel connectors via various cables. Table 4-2 lists the cable connectors on the A4 Motherboard and denotes their cable destination.

Table 4-2. A4 M otherboard PCB CableConnectors

| Connector | Cable Destination |
| :---: | :--- |
| J1 | A3 Signal Channel PCB (ribbon cable) |
| J2 | A2 Front Panel Interface PCB (ribbon cable) |
| J3 | YIG Oscillator Assembly |
| J4 | Downconverter |
| J5 | Control Modulator |
| J6 | 70 dB Step Attenuator* |
| J7 | Directional Coupler |
| J8 | Distribution PCB |
| J9 | Horizontal Output connector (rear panel) |
| J10 | Centronics Printer output (rear panel) |
| J13 | GPIB Interface connector (rear panel)* |
| J14 | (not used) |
| J15 | A9 Power Supply motherboard |
| J16 | Internal CRT monitor |
| J17 | A3 Signal Channel PCB Output Cable |
| J20 | External Monitor connector (rear panel) |
| * Optional |  |

4-12 rf deck assembly

The RF deck assembly contains the components that generate CW and swept frequency RF signals and route these signals to the front panel RF OUTPUT connector. The RF decks used in the 54XXA series are designed around a single YIG-tuned oscillator configuration. In these units, the YIG frequency is controlled by the frequency instruction and YIG driver circuitry located on the A6 and A5 PCB's. In addition to the components used to generate and route the RF signals, each RF deck assembly also contains components that produce the markers used by the central processor to control the accuracy of the output frequency.

RF Deck Con- There are six different configurations of the RF deck figurations assembly. One configuration covers the RF models (5407A thru 5411A); the other five configurations cover the Microwave Band models (5417A thru 5447A). The frequency range of these eleven models is 1.0 MHz to 26.5 GHz .

The block diagram of the RF Deck for Models 5417A and 5419A is shown in Figure 4-18 on page 4-51. This diagram, includes all of the RF components found on a typical RF deck assembly for 54XXA series microwave band models. Refer to this block diagram during the descriptions of common RF components and frequency control circuits presented below.

## Common RF Deck Components

Many RF components are common to all RF deck assembly configurations. These common components are described in Table 4-3. Refer to this table as necessary while reading the descriptions of 54XXA RF decks in the following paragraphs. RF components that are peculiar to a specific RF deck configuration are described as part of the description for that particular RF deck.

## Table 4-3. Common RF Deck Component Descriptions

## YIG-tuned Oscillator

Each RF deck assembly contains a single YIG-tuned oscillator. The YIG-tuned oscillator generates high-power RF output signals that have low broadband noise and low spurious content.

The YIG-tuned oscillator is driven by the FM and Main tuning coil currents from the A5 YIG Driver PCB. During CW mode, the main tuning coil current tunes the oscillator to within a few megahertz of the final output frequency. The frequency control circuitry then fine adjusts the FM tuning coil current to make the output frequency exact.

In the sweep mode, with sweep widths greater than 40 MHz , the main tuning coil current tunes the oscillator through the swept frequency range. For sweep widths of 40 MHz or less, the FM tuning coil current tunes the oscillator throughout the swept frequency range.

## Control Modulator

Each RF deck assembly contains a control modulator (Figure 4-18). In some configurations the control modulator is located inside another component such as the Down Converter (models 5407A, 5409A, and 5411A), It may also be located in the Switched Filter Assembly (models 5437A and 5447A).

The control modulator contains PIN switches that control the output power of the YIG-tuned oscillator. The modulator bias input drives the PIN switches that switch the RF power on and off; the modulator control input drives the PIN switches that control the output RF power level. A portion of the RF input to the modulator is picked off for use by the frequency source-lock circuitry.

## Filters

The filters provide bandpass filtering of the RF signals to reduce harmonic emissions.

## Directional Detector

Each RF deck assembly contains a directional detector that transfers the RF output signal to the RF OUTPUT connector. It also couples a portion of the RF output signal to an integral RF detector. The detected output is used as the "internal" ALC sense signal that is input to the power leveling circuits located on the A6 ALC/Frequency Instruction PCB.

The directional detector assembly also includes a thermistor that senses the detector's temperature that is also connected to the A6 PCB power leveling circuits. In models 5407A, 5409A, and 5411A, the directional detector is located inside the Down Converter.

## Step Attenuator

The optional step attenuators provide up to 70 dB attenuation of the RF output in 10 dB steps. The step attenuator control and driver circuits are located on the A7 Central Processor PCB. There are three versions of these attenuators, which are model dependant. Refer to the 54XXA Scalar Measurement Systems Operation Manual for further details.

## Frequency Control and Source-Lock

The A7 Central Processor controls the output frequency of the YIG-tuned Oscillator through the frequency instruction circuits located on the A6 ALC/ Frequency Instruction PCB. These circuits convert the digital instructions from the central processor into analog control signals for the YIG main coil and FM coil driver circuits located on the A5 YIG Driver/ Channel Interface PCB. The main coil and FM coil driver circuits convert the control signals into currents that drive the coils of the YIG-tuned oscillator to produce an output RF signal. The output RF signal from the YIG-tuned oscillator goes to the Control Modulator. In the control modulator, a portion of the RF signal is picked off and routed to the Sampler as an input to the frequency source-locking circuitry.

The frequency accuracy of the 54XXA series is based upon an internal 10 MHz crystal oscillator ( 75 MHz crystal oscillator for models 5407A, 5409A, and $5411 \mathrm{~A})$. The output of this 10 MHz reference oscillator, located in the Divider Module, is used to phaselock the 500 MHz VCO located in the 500 MHz VCO/Power Amplifier Module. The output of the 500 MHz VCO goes via a power amplifier to a step recovery diode (SRD).

The SRD produces a 500 MHz comb signal throughout the full range of the 54XXA, 10 MHz to 26.5 GHz . The 500 MHz comb signal then goes to the Sampler where it is used to switch the sampling diodes. (The sampler is physically part of the 500 MHz Marker Module.) The other input to the sampler is the RF signal picked off in the control modulator. The sampling diodes sample the RF input signal at the 500 MHz comb signal rate. The RF signal output of the sampler goes to the 500 MHz Marker Module where it is amplified and filtered to produce 500 MHz markers. The 500 MHz markers then go to a data buffer on the A6 PCB to be read by the central processor.

The 500 MHz VCO/Power Amplifier module (Figure 4-18) also produces a 25 MHz output using the divider circuitry in the Divider module. This 25 MHz signal goes to the 25 MHz Marker Module. There it is amplified and applied to a SRD producing a 25 MHz comb signal. The 25 MHz comb signal goes to the sampler where it turns on the sampling diodes that sample the DC to 250 MHz IF signal input which was generated in the 500 MHz Marker module. The resultant output is 25 MHz markers that cover the frequency range of 2.0 to 26.5 GHz . The 25 MHz markers also go to a data buffer on the A6 PCB to be read by the central processor.

The central processor processes the 500 MHz and 25 MHz marker read signals from the A6 PCB. If the marker read signals indicate that the frequency is not source-locked, the central processor generates error correction instructions which it sends to the A6 PCB. In the A6 PCB, the frequency error correction circuitry outputs a voltage to the A 5 PCB that is the frequency source-lock error correction signal. In the A5 PCB, this signal produces a current to drive the FM coil to offset the frequency error and source-lock the YIG-tuned oscillator.

The RF decks of models 5417A and 5447A RF have a 10 MHz to 2 GHz Down Converter installed. A portion of the down-converted RF signal is picked off and routed to an additional 25 MHz M arker Generator. This marker generator produces 25 MHz markers that cover the frequency range of 10 MHz to 2.0 GHz . The central processor uses these 25 MHz markers to achieve frequency source-lock in exactly the same manner as described in the preceding paragraphs.

The RF models 5407A, 5409A, and 5411A use 75 MHz and 25 MHz markers to achieve frequency source-lock. A description of the $75 \mathrm{MHz} / 25 \mathrm{MHz}$ Marker Generator is included as a part of the functional description of the RF deck assembly.

## RF Decks for Models 5417A/ 5419A

The RF decks of microwave band models 5417A ( 10 MHz to 8.6 GHz ) and 5419A ( 2.0 to 8.6 GHz ) are very similar. However, model 5417A contains two additional components, a Down Converter and a 25 MHz Marker Generator. These additional components enable the 5417A to generate RF outputs in the frequency range of 10 MHz to 2.0 GHz . (This band of frequencies is referred to as the "hetrodyne band;" M odel 5447A also operates in this band.) Refer to Figure 4-18 during the following functional description.

The output RF signal from the YIG-tuned oscillator goes to the Control Modulator. In the control modulator, a portion of the RF signal is picked off for input to the frequency source-lock circuitry (previously described). There are two inputs to the control modulator that control the RF output power level - the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/F requency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output. The RF output signal from the control modulator is sent to the Switched Filter.

In the 5417A, the control modulator has an additional RF output for the Down Converter. When the unit is generating RF signals in the frequency range of 10 MHz to 2.0 GHz , a 6.31 to 8.3 GHz signal is sent to the down converter where it is mixed with a 6.3 GHz signal from the down converter's internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the Switched Filter.

A portion of the down-converted RF signal is picked off and sent as an input to the 25 MHz Marker Generator. In the marker generator, it goes to the input sampler where it is sampled by the sampling diodes at a 25 MHz comb signal rate. The resultant output is 25 MHz markers that are used by the central processor to achieve frequency source-lock.


A portion of the RF output signal from the down converter is detected (by the directional detector), and sent to the ALC circuitry on the A6 PCB. This is the feedback signal for the internal ALC function.

The directional detector also contains a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A 6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF output-vs-temperature characteristic.

The Switched Filter provides rejection of the harmonics generated by the 2.0 to 8.6 GHz YIG-tuned oscillator. In model 5417A, it also multiplexes between the 10 MHz to 2.0 GHz and the 2.0 GHz to 8.6 GHz signals from the down converter during full band sweeps. Drive current for the switched filter is provided by the A18 Switch Filter Driver PCB that is mounted on top of the switched filter assembly. The 2.0 to 8.6 GHz RF signal from the control modulator has three filtering paths; the 3.5 GHz filter path, the 6 GHz filter path, and the 8 GHz filter path. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the signal is multiplexed through to the switched filter output.

The RF signal output from the switched filter is sent to the Directional Detector and transferred to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. In the ALC circuitry, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

## RF Decks for Models 5428A, 5430A, 5431A, and 5436A

The RF decks of models 5428A ( 8 to 12.4 GHz ), 5430A ( 12.4 to 20 GHz ), 5431 A ( 10 to 16 GHz ), and 5436 A ( 17 to 26.5 GHz ) have an identical configuration. Refer to Figure 4-19 during the following functional description.

The output signal from the YIG-tuned oscillator goes to the Control M odulator. In the control modulator, a portion of the RF signal is picked off for input to the frequency source-lock circuitry, which was previously described in the general description (page 4-46).

There are two inputs to the control modulator that control the RF output power level - the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/F requency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output.

The output from the control modulator is sent to the Directional Detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and sent as a feedback signal to the ALC circuitry located on the A6 PCB. This signal is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output to the desired level.

The directional detector also contains a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF -output-vs-temperature characteristic.


Figure 4-19. Block Diagram of RF Decks for Modeds 5428A


The RF decks of microwave band models 5437A (2.0 to 20 GHz ) and 5447A ( 10 MHz to 20 GHz ) are very similar. However, model 5447A contains two additional components, a Down Converter and a 25 MHz Marker Generator. These additional components enable the 5447A to generate RF signals in the frequency range of 10 MHz to 2.0 GHz . Refer to Figure 4-20. during the following functional description.

The output signal from the YIG-tuned Oscillator goes to the Switched Filter Assembly. As shown in Figure 4-20, the switched filter assembly contains a control modulator and a switched filter. After amplification, a portion of the RF signal is sent to the frequency source-lock circuitry (previously described).

There are two inputs to the control modulator section that control the RF output power level - the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/ Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output signal.

The output signal from the control modulator section is sent to the switched filter, which contains a coupler to provide a signal for the Down Converter. Whenever the model 5447A is generating RF signals in the frequency range of 10 MHz to 2.0 GHz , a 6.31 to 8.3 GHz RF signal is coupled out of the switched filter, through an 8 GHz filter path, and routed to the down converter. In the down converter, this signal is mixed with a 6.3 GHz signal from the down converter's internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the switched filter. A portion of the down-converted signal is picked off and is input to the $75 \mathrm{MHz} / 25 \mathrm{MHz}$ Marker Generator.

Inside the marker generator, the output from the local 75 MHz crystal oscillator is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step recovery diode produces a 75 MHz comb signal that drives the sampling diodes. These diodes sample the RF signal from the down converter (above). The output of the sampler is amplified and filtered to produce 75 MHz markers (the 75 MHz markers are not used in this application). In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a DC to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers.

The 25 MHz markers are used by the central processor to achieve source-lock. A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature as an input to the A6 PCB.

The switched filter provides rejection of the harmonics that are generated by the 2.0 to 20 GHz YIGtuned oscillator. In model 5447A, it also multiplexes between the 10 MHz to 2.0 GHz and 2.0 GHz to 20.0 GHz signals from the down converter during full band sweeps. The 2.0 to 20 GHz RF signal from the control modulator has four filtering paths and one through path. The four filtering paths are:
$\square 3.3 \mathrm{GHz}$ path
$\square 5.5 \mathrm{GHz}$ path
$\square 8.6 \mathrm{GHz}$ path

- 13.5 GHz path

Signals above 13.5 GHz are routed via the through path to the switched filter output. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the RF signal is multiplexed through to the switched filter output.


The RF signal output from the switched filter is sent to the Directional Detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. In these circuits, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF-output-vs-temperature characteristic.

## RF Decks for Models 5407A, 5409A, and 5411A

The RF decks of the models 5407A ( 1.0 MHz to 1.0 GHz ), 5409A ( 1.0 MHz to 2.0 GHz ), and 5411A ( 1.0 MHz to 3.0 GHz ) contain identical components. Refer to Figure 4-21 during the following functional description.

The RF output signal from the YIG-tuned Oscillator goes to the Down Converter through an Isolator. The isolator prevents the reflection of RF energy back into the YIG-tuned oscillator. In the down converter, the 10 to 13 GHz RF signal from the YIG-tuned oscillator is mixed with a 10 GHz signal from the down converter's internal oscillator. The resulting 1.0 MHz to 3.0 GHz RF signal goes to the control modulator.

The control modulator is used to control the RF output power level of the unit. The modulator control output signal from the A6 ALC/F requency Instruction PCB drives the modulator PIN switches that control the power level of the output signal. From the control modulator, the RF signal goes through a Low-Pass Filter, is amplified, and then routed to the RF OUTPUT connector.

A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. On the A6 PCB, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry that drives the control modulator PIN switches to adjust the RF power output level.

The directional detector in the down converter also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 ALC circuits and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF output-vs-temperature characteristic.


Within the down converter, a portion of the downconverted RF signal is picked off for input to the 75 MHz/25 MHz Marker Generator. Inside the marker generator, the 75 MHz crystal oscillator output is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step-recovery diode produces a 75 MHz comb signal. This comb signal turns on the sampling diodes that sample the RF signal from the down converter. The output of the sampler is amplified and filtered to produce 75 MHz markers.

In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a DC to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers. The 25 MHz and 75 MHz markers go to a data buffer on the A6 PCB to be read by the central processor.

The central processor processes the 75 MHz and 25 MHz marker read signals from the A6 PCB. If the marker-read signals indicate that the frequency is not source-locked, the A7 central processor generates error correction instructions that are sent to the A6 PCB frequency error correction circuitry. These circuits output a frequency source-lock error correction signal that is sent to A5 YIG Driver/Channel Interface PCB. The output from the A5 YIG driver circuit is a current that causes the FM coil to offset the frequency error, thus producing source-lock of the YIG-tuned oscillator.

# Chapter 5 <br> Removal and Replacement Procedures 

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# Chapter 5 <br> Removal and Replacement Procedures 

## 5-1 introduction

The disassembly procedures presented in this chapter describe how to gain access to the major 54XXA assemblies and parts for troubleshooting or replacement.

## WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

## CAUTION

Many assemblies in the 54XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. Always observe the static-sensitive component handling precautions described in Figure 5-1.

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some 54XXA assemblies and parts require removal of all covers. The following procedures describe this process.

Preliminary Disconnect the power cord from the unit.
Procedure Step 1 Using a Pozidriv ${ }^{\circledR}$ screwdriver, remove the two feet from the top corners at the rear of the instrument.

Step 2 Carefully slide the top cover out along the grooves in the chassis.

Step 3 Lift the top cover off and set it aside.
Step 4 Place the instrument on its side.
Step 5 Using a Pozidriv screwdriver, remove the two feet from the bottom corners at the rear of the instrument.

Step 6 Carefully slide the bottom cover out along the grooves in the chassis.

Step 7 Lift the bottom cover off and set it aside.
Step 8 Place the instrument on its right side and slide the left side cover out, towards the back of the instrument. Set the cover aside.

Step 9 Place the instrument on its left side and slide the right side cover out, towards the back of the instrument. Set the cover aside.

Step 10 To replace the covers, reverse the procedure used to remove them. Note that the side cover with ventilation holes mounts on the right side of the 54XXA (side opposite the fan).


1. Do not touch exposed contacts on any static sensitive component.

2. Wear a static-discharge wristband when working with static sensitive components.

3. Handle PCBs only by their edges. Do not handle by the edge connectors.

4. Do not slide static sensitive component across any surface.

5. Label all static sensitive devices.

6. Lift \& handle solid state devices by their bodies - never by their leads.

7. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

8. Keep component leads shorted together whenever possible.

9. Transport and store PCBs and other static sensitive devices in staticshielded containers.
10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 5-1. Static Sensitive Component Handling Procedures

## 5-3 <br> REMOVING AND REPLACING THE A5, A6, A7 AND A8 PCB's

This paragraph provides instructions for removing and replacing the A5, A6, A7 and A8 PCB's, which are located underneath the cover of the card cage.

## Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 5-2.

## Procedure Step 1 Remove the four screws and associated

 washers that retain the card cage cover and set aside.Step 2 Remove card cage cover and set aside.
Step 3 Lift up on edge tabs of selected PCB(s) and lift out of card cage. (Note that locations of A5, A6, A7 and A8 PCB's are shown on top of card cage cover.)

Step 4 To replace PCB(s), reverse the removal process.

This paragraph provides instructions for removing and replacing the A3 Signal Channel PCB, which is located immediately behind the front panel input connectors. Use this procedure also for gaining access to the INPUT A, INPUT B, and (optional) INPUT C connectors for replacement.

Preliminary
Disconnect the power cord from the unit and remove the instrument covers as described in paragraph 5-2.

## Procedure

Step 1 Place 54XXA on its right side on a padded surface. Disconnect the output cable from A3 PCB at connector J 16 of the A4 M otherboard. (It will be necessary to first remove the A5 PCB from the card cage.)

Step 2 Gently place 54XXA upside down. Disconnect the white grounding wire from the A3 PCB and dress away from the PCB (see figure).

Step 3 Disconnect the ribbon cable at the rear of the A3 PCB.

Step 4 Remove the five screws and associated washers that fasten the A3 PCB and the associated output cable to the 54XXA
main deck (Figure 5-2). Set screws and washers aside.

Step 5 Remove the two nuts that fasten the input connector bracket to the front panel (see figure), and set aside.

Step 6 Gently lift the rear edge of the A3 PCB and pull toward the rear of the 54XXA to remove.

Step 7 To replace the A3 PCB and front panel input connectors, reverse the removal process.


Figure 5-2. Removing the A3 Signal Channel PCB and Front Pane Input Connectors

| $54 X X A M M$ | $5-7$ |
| :--- | ---: |

# 5-5 <br> REMOVING AND REPLACING THE FRONT PANEL ASSEMBLY 

This paragraph provides instructions for removing and replacing the front panel assembly of the 54XXA.

Preliminary: Disconnect the power cord from the unit and remove all four instrument covers as described in paragraph 5-2.

## Procedure:

Step 1 Place 54XXA upside down on a padded
surface.

Step 2 Remove the two nuts that fasten the front panel input connector bracket, which is part of the A3 Signal Channel PCB. Refer to step 5 of paragraph 5-4 and to Figure 5-2.

Step 3 Turn 54XXA right side up.
Step 4 Disconnect the ribbon cable at connector J 1 of the A2 PCB.

Step 5 Disconnect the multi-wire cable at connector J 3 of the A2 PCB.

Step 6 Use a 3/32 inch right-angle hex wrench to remove the three hex head screws that are located al ong the top of the chassis frame at the front of the unit. (The heads of these screws are located at the rear edge of the chassis frame and fasten to the front panel.) Repeat for the two hex head screws located al ong the right front edge of the chassis and for the four screws along the bottom edge.

Step 7 Gently pull front panel assembly forward until it is clear of the RF output connector and lay flat.

Step 8 To replace the front panel assembly, reverse the removal process.

This paragraph provides instructions for removing and replacing the A1 Front Panel PCB and A2 Front Panel Interface PCB. These PCB's are located immediately behind the front panel on the left side of the unit.

Preliminary: Remove the front panel assembly of the unit (paragraph 5-5).

Procedure: Step 1 If not done previously, disconnect the cables at connectors J 1 and J 3 of the A2 PCB.

Step 2 Using a 0.050 in . hex wrench, loosen the two Data Entry knob hex screws. Remove knob and set aside.

Step 3 Lay the front panel assembly face down on a padded surface.

Step 4 Remove the six screws that fasten the A1 and A2 PCB's to the front panel. Carefully lift both PCB's from the front panel, and set the front panel aside.

Step 5 Disconnect the cable from the spinwheel generator at connector J 2 of the A1 Front Panel PCB.

Step 6 Disconnect the A2 PCB from the A1 PCB and carefully lift the A2 PCB until it is clear of the spinwheel generator.

Step 7 To replace the A1 and A2 PCB's, reverse the removal process.

This paragraph provides instructions for removing and replacing the D35370 Power Supply Assembly, which consists of the A9 Power Supply Motherboard PCB and the A16 Power Supply Converter PCB. The power supply assembly is removed/replaced as a complete unit.

Preliminary: Disconnect the power cord from the unit and remove all four instrument covers as described in paragraph 5-2.

## Procedure: <br> Step 1 Place 54XXA on its left side on a padded

surface.

Step 2 Remove the two screws that fasten the POWER ON/OFF switch mounting bracket to the chassis (Figure 5-3, top).

Step 3 Similarly, remove the two screws that fasten the power supply assembly bottom bracket to the chassis center rail.

Step 4 Turn 54XXA right side up.
Step 5 Disconnect the cable from the Line Voltage Selector M odule at connector J 1 of the Power Supply M otherboard.

Step 6 Similarly, disconnect the fan cable at connector J 3.

Step 7 Disconnect the cable at connector J 2 (at the front edge of the Power Supply M otherboard).

Step 8 Remove the five screws that fasten the power supply assembly to the chassis side rail (Figure 5-3, bottom).

Step 9 Lift the power supply assembly up and forward to remove from unit.

Step 10 To replace the power supply assembly, re verse the removal process.


Figure 5-3. Removing the Power Supply Assembly

## 5-8 <br> REMOVING AND REPLACING THE CRT MONITOR ASSEMBLY

This paragraph provides instructions for removing and replacing the CRT M onitor Assembly, which consists of the CRT monitor unit and mounting bracket. The CRT M onitor Assembly is removed/ replaced as a complete unit.

Preliminary: Disconnect the power cord from the unit and remove all four instrument covers as described in paragraph 5-2.

## Procedure:

Step 1 54XXA on its left side on a padded surface.

Step 2 Remove the four screws that fasten the CRT monitor assembly to its mounting bracket (Figure 5-4).

Step 3 While supporting the CRT monitor assembly, turn the 54XXA right side up.

Step 4 Disconnect the CRT monitor assembly cable at connector J 15 of the A4 M otherboard PCB.

Step 5 M ove the assembly to the rear and lift from unit.

Step 6 To replace the CRT monitor assembly, reverse the removal process.


Figure 5-4. CRT Monitor Assembly Removal (Bottom)

## 5-9 <br> REMOVING AND REPLACING THE REAR PANEL

This paragraph provides instructions for removing and replacing the 54XXA rear panel. This procedure is used to provide access to the HORIZONTAL OUTPUT and (optional) EXTERNAL ALC INPUT connectors and to the cooling fan for replacement.

NOTE
It is not necessary to remove the rear panel to replace the Line Voltage Selector Module, or the EXTERNAL MONITOR, GPIB/IEEE-488 INTERFACE, or PARALLEL PRINTER INTERFACE connectors.

Preliminary: Disconnect the power cord from the unit and remove all four instrument covers as described in paragraph 5-2.

Procedure: Step 1 Place 54XXA right side up on a padded surface.

Step 2 Remove the three screws al ong the lower edge of the rear panel plate.

Step 3 Similarly, remove the three screws along the upper edge of the rear panel plate and lay panel flat.

Step 4 To replace the rear panel, reverse the removal process.

5-10
REMOVING AND REPLACING THE FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the rear panel cooling fan assembly.

Preliminary: Disconnect the power cord from the unit and remove the rear panel as described in paragraph 5-9.

Procedure: Step 1 Disconnect the fan power cable at connector J 3 of the A9 P ower Supply Motherboard PCB.

Step 2 With the rear panel laying flat, use a $5 / 16$ inch open-end wrench to remove the four nuts that fasten the fan to the rear panel.

Step 3 Lift the defective fan assembly from the rear panel and discard.

Step 4 To replace the fan assembly, reverse the removal process.

## NOTE

The fan filter should be cleaned at this time, if necessary.

## 5-11 <br> REMOVING AND REPLACING THE RF DECK ASSEMBLY

This paragraph provides instructions for removing and replacing the RF deck assembly, which is located on the left side of the chassis. Use this procedure for gaining access to the RF deck components for removal and replacement.

## NOTE

Normally, it is not necessary to remove the RF Deck from M odels 5407A, 5409A, and 5411A. Almost all troubleshooting and repair operations can be performed with the RF Deck in place.

Preliminary: Disconnect the power cord from the unit and Remove the top, bottom, and left side covers of the unit (paragraph 5-2).

Procedure: Step 1 Disconnect all cable connections between the RF deck to the A4 Motherboard.

Step 2 Using a Phillips screwdriver, remove the five screws and associated washers that secure the RF deck to the unit chassis (Figure 5-5). Set the screws and washers aside.

Step 3 Slide the RF deck toward the rear of the chassis until the RF OUTPUT connector clears the front panel (see figure).

Step 4 Lift the RF deck up and out of the chassis using care to avoid snagging any of the RF deck cables.

Step 5 To replace the RF deck, reverse the removal process.

## 5-12 rfdeck COMPONENT location DIAGRAMS

There are six different configurations of the RF deck assembly. One configuration covers the RF models (5407A thru 5411A); the other five configurations cover the Microwave Band models (5417A thru 5447A). Figures 5-6 through 5-11 show the component locations for these RF Decks; the table below lists the figure(s) appropriate for each model.

| Model | Internal Side Parts <br> Location | External Side Parts <br> Location | Page <br> No |
| :--- | :---: | :---: | :---: | :---: |
| 5407A, 5409A, <br> 5411A | N/A | Figure 5-6 | $5-18$ |
| 5417A, 5419A | Figure 5-7a | Figure 5-7b | $5-19$ |
| 5428A, 5430A, <br> 5431A, 5436A | Figure 5-8a | Figure 5-8b | $5-21$ |
| 5437A, 5447A | Figure 5-9a | Figure 5-9b | $5-23$ |

Figure 5-5. RF Deck Removal/ Replacement


Figure 5-6. Models 5407A, 5409A, and 5411A RF Deck Parts Location


Figure 5-7a. Models 5417A and5419A: RF Deck Parts Location (Internal SideDetail)


Figure 5-7b. Models 5417A and 5419A: RF Deck Parts Location (External SideDetail)


Figure 5-8a. Models 5428A, 5430A, 5431A, and 5436A: RF Deck Parts Location (Internal SideDetail)


Figure 5-8b. Models 5428A, 5430A, 5431A, and 5436A RF Deck Parts Location
(External Side Detail)


Figure 5-9a. Modes 5437A and 5447A: RF Deck Parts Location (Internal SideDetail)

## Chapter 6 Adjustments

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## Chapter 6 Adjustments

## 6-1 introduction

## 6-2 recommendedtest EQUIPMENT

This chapter provides adjustment procedures for all models of series 54XXA Scalar Measurement Systems. The organization of these procedures is shown in the table of contents on page 6-1.

NOTE
Throughout these procedures, the terms "adjustment potentiometer", " potentiometer", and "adjustment variable resistor" are used interchangeably.

The recommended test equipment for each adjustment procedure is listed at the beginning of the procedure. This test equipment is also listed in Table 1-2 (in Chapter I - General Service Information). If the recommended equipment is not available other test equipment with suitable characteristics may be substituted.

## NOTE

Allow the 54XXA and all test equipment to warm up at least 30 minutes prior to performing any of the adjustments.

Use this procedure to make all necessary adjustments to the A3 Signal Channel PCB. This procedure is in two parts: The Log Conformity Adjustment (next page), and the Signal Channel Sensitivity Adjustment (page 6-5). All potentiometers ( Rx ) referred to in this procedure are located on the A3 PCB.

Required Test Equipment:
$\square$ Detector Simulator — WILTRON T1492, or equivalent; refer to Appendix B.
$\square$ DC Voltage Standard — J ohn Fluke M odel 335D, or equivalent
$\square$ Adaptor Cable - WILTRON 560-10BX

Perform this procedure as follows:
Step 1 Connect detector simulator T1492 to INPUT A and turn the 54XXA on. (If not done previously, allow 30 minutes warm up before continuing with the adjustment procedure.)
Step 2 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 3 Set channel 1 to measure power from signal channel INPUT A (or INPUT B, as appropriate). Turn channel 2 measurement off.

Step 4 Press the CALIBRATION key and select DC CAL MENU.
Step 5 Press the ENTER key. The 54XXA will display the log conformity ( $\mathbf{L}$ ) and temperature thermistor ( $\mathbf{T}$ ) values in the menu area of the 54XXA display.
Step 6 With the detector simulator connected to signal channel INPUT A, observe that the displayed $\mathbf{T}$ value is $0.00 \pm 0.10$.

Step 7 Adjust variable resistor A3R108 to obtain a displayed $\mathbf{L}$ value of $0.00 \pm 0.01$.

Step 8 Connect the detector simulator to INPUT B, and set the 54XXA as in steps $\mathbf{3}$ thru 5 above. Observe that the displayed $\mathbf{T}$ value is $0.00 \pm 0.10$.
Step 9 Adjust variable resistor R109 to obtain a displayed L value of $0.00 \pm 0.01$.
Step 10 Connect the detector simulator to INPUT R (if present). Observe that the displayed $T$ value is $0.00 \pm 0.10$.

Step 11 Adjust variable resistor R110 to obtain a displayed L value of $0.00 \pm 0.01$.


Perform this procedure as follows:
Step 1 Connect the equipment as shown in Figure 6-1.
Step 2 Press the SYSTEM MENU key. Select reset and press the SELECT key.
Step 3 Select Restore Default Setup and press the SELECT key.
Step 4 Set channel 1 to measure power on signal channel INPUT A (or INPUT B, or INPUT R, as appropriate). Turn measurement channel 2 off.

Step 5 Set the DC Voltage Standard for zero volts output. (Verify that it is connected to the correct input channel connector using a 560-10BX adaptor cable.)
Step 6 Press the CALIBRATION key and select DC CAL MENU.
Step 7 The 54XXA should now display a noise floor at approximately -63 dBm . Allow the 54XXA to sweep for 5 seconds.

Step 8 Using the menu up/down keys, select ON from the DC CAL MENU. The 54XXA will now display DC CAL in the top right hand corner of the screen display.


Figure 6-1. Equipment Setup for Signal Channe Sensitivity Adjustment

Step 9 Set the DC Voltage Standard for - 0.6208 volts output. Press the 54XXA CURSOR key to obtain a readout in the menu area of the 54XXA display.
Step 10 Adjust A3R118 to obtain a cursor readout of $+9.00 \mathrm{dBm} \pm 0.01 \mathrm{dBm}$.
Step 11 Set the DC Voltage Standard for -1.462 volts output. Observe that the 54XXA cursor readout is $+16.00 \mathrm{dBm}+0.25 /-0.10$ dBm.

Step 12 Set the DC Voltage Standard for - 1.313 millivolts output. Observe that the cursor readout is $-26.00 \mathrm{dBm} \pm 0.34 \mathrm{dBm}$.

Step 13 Connect the DC Voltage Standard to INPUT B and repeat steps 2 thru 12.
Step 14 Connect the DC Voltage Standard to INPUT R (if present) and repeat steps 2 thru 12. Use variable resistor R117 to adjust the R channel gain, as necessary.

## NOTE

Variable resistor R118 adjusts the gain for both channel A and channel B. If there is a difference of more than $\pm 0.02 \mathrm{dBm}$ between the channel A and channel B cursor readouts at +9.00 dBm , recheck the Log Conformity Adjustment on page 6-4.

## 6-4 <br> YIG DRIVER ADJUSTMENT PROCEDURE

Table 6-1. J umper A5J 2 Position, by Mode

| 54XXA Model | J2 Pin <br> Position |
| :--- | :---: |
| 5407A thru 5419A, <br> and 5430A | $1 \& 2$ |
| 5431A and 5436A | $3 \& 4$ |
| 5428A, 5436A, and <br> 5447A | $5 \& 6$ |

Use this procedure to make adjustments to the A5 YIG Driver/Signal Channel Interface PCB. All variable resistors ( Rx ) and jumpers referred to in this procedure are located on the A5 PCB.

Procedure Step 1 Confirm that jumper J 2 is positioned per table at left.
Step 2 Connect the input of the microwave counter to the RF OUTPUT connector of the 54XXA (Figure 6-2). Select the correct band input on the counter for the frequency to be measured.
Step 3 Set the 54XXA for the Service Mode of operation, as follows: Press the SELF TEST key; when the HOLD LED flashes during the self test, quickly press the FREQUENCY, MARKERS, and LEVELING keys in sequence. The 54XXA will now display the main service mode menu.
If any key is pressed in error when in the "frequency dac control" section of the service mode, press the SELF TEST key and re-enter the service mode. This will ensure that the START, ERROR, WIDTH, and RAMP DAC settings are preset correctly for this adjustment. (It is possible to change the settings for these DAC's while in this section of the service mode.)

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Figure 6-2. Equipment Setup for YIG Driver Adjustment Procedure

| $54 X X A M M$ | $6-7$ |
| :--- | ---: |

Table 6-2. START DAC Minimum Adjustment Frequencies

| 54XXA Model | START DAC <br> Calibration <br> Freq (GHz) |
| :--- | :---: |
|  <br> 5411A | 0.069 * |
| 5417A \& 5419A | 1.800 |
| 5428A | 7.800 |
| 5430A | 12.200 |
| 5431A | 9.800 |
| 5436A | 16.800 |
| 5437A \& 5447A | 1.800 |
| * This frequency is on other side of |  |
| "zero-beat" due to offset below band |  |
| edge. |  |
|  |  |

Step 4 Press the 54XXA DATA ENTRY "1" key to select "frequency dac control" sequence.

Step 5 Press the DATA ENTRY "1" key twice. This sets the START DAC to minimum frequency. The highlighted video block should now display "start dac" set to "min".

## NOTE

> Earlier A5 PCB versions (those without daughter-boards) have different designations for the adjustment potentiometers. For these units, use the potentiometer designations shown in parentheses in this procedure.

Step 6 For models 5417A through 5447A: Adjust R4 (R42) on the A5 PCB for a counter reading that is $200 \mathrm{MHz} \pm 10$ MHz below the band start frequency of the unit (Table 6-2).

Step 7 F or models 5407A, 5409A, and 5411A: Adjust R4 (R42) for a counter reading 70 $\mathrm{MHz} \pm 2 \mathrm{MHz}$ bel ow the band start frequency, as explained in Table 6-2.
A clockwise adjustment of R4 (R42) must increase the reading on the frequency counter. If this is not the case, the frequency adjustment is on the wrong side of the "zero-beat" and requires readjustment.

Step 8 F or all models except the 5436A: Press the DATA ENTRY " 1 " and " 3 " keys in sequence. This sets the START DAC to maximum frequency. The highlighted video block should now display the "start dac" set to "max.

| ADJUSTMENTS | YIG DRIVER |
| :--- | ---: |

Table 6-3. START DAC Maximum Adjustment Frequencies

| 54XXA Model | START DAC <br> Calibration <br> Freq (GHz) |
| :--- | :---: |
| 5407 A | 1.070 |
| 5409 A | 2.070 |
| 5411 A | 3.070 |
| $5417 \mathrm{~A} \& 5419 \mathrm{~A}$ | $8.800^{*}$ |
| 5428 A | 12.600 |
| 5431 A | 16.200 |
| $5430 \mathrm{~A}, 5437 \mathrm{~A} \&$ | 20.200 |
| 5447 A | 26.400 |
| 5436 A |  |

* 8.600 GHz for units with 8.4 GHz HBEF . (To check, reset unit and note displayed STOP frequency.)

Step 9 F or model 5436A: Press the DATA ENTRY "1" and " 5 " keys simultaneously. The highlighted video block should now display the "start dac" set to "top."

Step 10 F or models 5417A through 5447A: Adjust R2 (R56) on the A5 PCB for a counter reading that is $200 \mathrm{MHz} \pm 10$ MHz above the band stop frequency of the unit. (These values are listed in Table 6-3.)

Step 11 F or models 5407A, 5409A, and 5411A: Adjust R2 (R56) for a counter reading that is $70 \mathrm{MHz} \pm 2 \mathrm{MHz}$ above the band stop frequency of the unit (Table 6-3).

Step 12 Repeat steps 5 thru 10 until no further adjustment is required.

Step 13 Press the SELF TEST key to return to normal instrument operation.

## ADJUSTMENTS

## 6-5 <br> ALC PRE-ADJUSTMENT PROCEDURES FOR MICROWAVE BAND MODELS

These procedures ensure that the RF output power of models 5417A through 5447A is approximately correct so that the 500 MHz and 25 MHz markers can be calibrated. Perform these procedures only if the ALC PCB or RF Deck components have been changed. If not re quired, go to paragraph 6-7.

NOTE
For models 5407A, 5409A, and 5411A, go to paragraph 6-6, RF Band ALC Pre-Adjustment Procedures for RF Band Models, which is located on page 6-16.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. All variable resistors ( Rx ) and test points (TPx) referred to in this procedure are on the A6 ALC/ Frequency Instruction PCB.

## NOTE

If the A6 PCB was changed, verify the jumper configuration is correct per Table 6-11 (page 6-27).

Required Equivalent equipment may be used - refer to paraTest Equipment
graph 6-2 and to Table 1-2 (in Chapter I - General Service Information):
$\square$ Power Meter, with suitable matching power sensor (Figure 6-3)

- Digital Voltmeter, with 4-1/2 digits resolution (Table 1-2)
$\square$ Oscilloscope, dual channel with two X10 probes (Table 1-2)
$\square$ WILTRON RF Detector - to match 54XXA model (Table 1-2)
MITROWAVE BAND
ADJUSTMENTS PRE-ADJUSTMENT PROCEDURE


## Reference <br> Voltage Adjustment

## Procedure

For units equipped with D35429-3A A6 PCB's, use the variable resistor designations shown in parenthesis in the following procedure.

Step 1 Set DVM for DC, 1V range (not autorange). Connect common lead to TP25; connect other lead to TP14.

Step 2 Adjust variable resistor A6R65 for a DVM reading of $1.0000 \mathrm{~V} \pm 0.5 \mathrm{mV}$.

Step 3 Connect common lead of DVM to TP25; connect other lead to TP31. Set voltmeter to autorange. (If the ALC PCB is equipped with a daughter-board, TP31 is the only test point on the daughterboard.)

Step 4 Adjust variable resistor R216 (R183) for a DVM reading of $-4.1 \mathrm{~V} \pm 0.05 \mathrm{~V}$. (If the ALC PCB is equipped with a daughterboard, R216 is located on the daughterboard.)

Step 5 Disconnect DVM. Go on to the the Power Output Adjustment on next page.

Power
Output Adjustment

Proceed as follows:
Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.
Step 2 Put the 54XXA in CW mode by setting measurement Channels 1 and 2 off.

Step 3 Press the FREQUENCY key and select CENTER/ WIDTH mode; Set WIDTH to 0 GHz , and set CENTER frequency at the (microwave) low band edge frequency for the model being calibrated, as follows:

M odels 5417A and 5447: 2.0 GHz
All other models: Lower frequency indicated on front panel.

Step 4 For all models except 5436A: Connect a MA4701A power sensor to the Anritsu ML4803A power meter (Figure 6-3). F or model 5436A, use a MA4703A power sensor. Perform a calibration as instructed in the power meter operation and service manual.

Step 5 Verify that the power meter Cal Factor is set correctly for the test frequency.


Figure 6-3. Equipment Setup for ALC PreAdjustment Procedure

Step 6 Connect the power meter sensor to the 54XXA RF OUTPUT connector (Figure 6-3). Press the 54XXA RF ON/OFF key to OFF. Zero the power meter, and then press RF ON/OFF key to ON.
Step 7 Adjust variable resistor R62 to give a power meter reading equal to the 54XXA reset power level $\pm 0.5 \mathrm{dBm}$. These levels are listed in Table 6-4.
Step 8 Reduce the 54XXA RF output power by 10dB.

Step 9 Adjust variable resistor R196 to give a power meter reading equal to the 54XXA set power $\pm 0.5 \mathrm{dBm}$.
Step 10 Adjustments R62 and R196 are interactive. Therefore, set RF output power to reset level (Table 6-4) and repeat steps 7 through 9 until both power meter readings are within $\pm 0.5 \mathrm{dBm}$ of 54 XXA indicated RF output power.
Step 11 Disconnect the power meter from the 54XXA RF OUTPUT connector. Go on to the ALC Operating Point Adjustment on next page.

Table 6-4. 54XXA Reset Power Leved Values

| 54XXA Model | Without <br> Attenuator | With <br> Attenuator |
| :--- | :---: | :---: |
| $5407 \mathrm{~A}, 5411 \mathrm{~A}, 5411 \mathrm{~A}$ <br> with $50 \Omega$ output | +12 dBm | +10 dBm |
| $5407 \mathrm{~A}, 5411 \mathrm{~A}, 5411 \mathrm{~A}$ <br> with $75 \Omega$ output | +10 dBm | +8 dBm |
| 5436 A | +7 dBm | +4 dBm |
| All other models | +10 dBm | +7 dBm |

ALC Operat- Proceed as follows: ing Point Adjustment

Step 1 Press the SYSTEM MENU key. Select RESET and press SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.
Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation).
F or models 5417A and 5447A, set START frequency to 2.0 GHz .
RF Power Output: 2 dB abovereset power level (see Table 6-4)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points: 401
Graticule: ON

Step 3 Set Oscilloscope as follows:
Horizontal Sweep: X-Y mode
Channel A vertical sensitivity: 1V/div
Channel B vertical sensitivity:
$0.5 \mathrm{~V} / \mathrm{div}$ (with X10 probe)
CH A input: DC
CH B input: DC
Display: CH A and CH B On

Step 4 Connect a suitable detector from the 54XXA RF OUTPUT connector to INPUT A. Press the channel 1 AUTOSCALE key (on).

Step 5 Connect oscilloscope CH A input to the 54XXA rear panel HORIZONTAL OUTPUT connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen.

## ADJUSTMENTS

Step 6 Connect CH B probe to A6TP28; connect the probe ground dip to the 54XXA chassis. The oscilloscope will display a waveform with a negative dc component.
Step 7 For models 5417A through 5436A: Adjust A6R133 to move the oscilloscope trace more positive until the trace oscillates and/or the 54XXA UNLEVELED LED lights. Now adjust R133 back two turns (trace more negative).

Step 8 For models 5437A and 5447A: Adjust R31 on the multi-band controller to move the oscilloscope trace more positive until the trace oscillates and/or the 54XXA UNLEVELED LED lights. Now adjust R31 back two turns (trace more negative).

This completes the microwave band pre-adjustment procedure. For all models except 5417A and 5447A, proceed to the 500 MHz and 25 MHz Marker Adjustment, paragraph 6-7, on page 6-20.

## 6-6

ALC PRE-ADJUSTMENT PROCEDURES FOR RF BAND MODELS

These procedures ensure that the RF output power of models 5407A, 5409A, and 5411A is approximately correct so that the 75 MHz and 25 MHz markers can be calibrated. Use this procedure al so for the RF (heterodyne) band of models 5417A and 5447A. Perform these proce dures only if the ALC PCB or RF Deck components have been changed. If not required, go to paragraph 6-7 on page 6-20.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. All variable resistors ( Rx ) and test points (TPx) referred to in this procedure are on the A6 ALC/Frequency Instruction PCB.

## NOTE

If the A6 PCB was changed, verify the jumper configuration is correct per Table 6-13 (page 6-31).
Required $\quad$ Refer to paragraph 6-5.
Test Equip-
ment

Reference Voltage Adjustment

Procedure

For models 5417A and 5447A go to the Power Output Adjustment Procedure on the next page. F or units equipped with D35429-3A A6 PCB's, use the variable resistor designations shown in parenthesis in the following procedure.

Step 1 Set DVM for DC, 1V range (not autorange). Connect common lead to TP25; connect other lead to TP 14.

Step 2 Adjust variable resistor A6R65 for a DVM reading of $1.0000 \mathrm{~V} \pm 0.5 \mathrm{mV}$.

Step 3 Connect common lead of DVM to TP25; connect other lead to TP31. Set voltmeter to autorange. (If the ALC PCB is equipped with a daughter-board, TP31 is the only test point on the daughterboard.)

Step 4 Adjust variable resistor R216 (R183) for a DVM reading of $-4.1 \mathrm{~V} \pm 0.05 \mathrm{~V}$. (If the ALC PCB is equipped with a daughterboard, R216 will be on the daughterboard.)

Step 5 Disconnect DVM.

## Power Output Adjustment

Proceed as follows:
Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 2 Put the 54XXA in CW mode by setting measurement Channels 1 and 2 off.

Step 3 Press the FREQUENCY key and select CENTER/ WIDTH mode; Set WIDTH to 0 MHz and CENTER to 50 MHz .

Step 4 F or models 5407A, 5409A, and 5411A equipped with $50 \Omega$ RF outputs: connect a MA4601A power sensor to the Anritsu ML4803A power meter.

Step 5 F or units equipped with $75 \Omega$ RF outputs: connect a MA4603A power sensor along with a J 0365 Conversion Connector to the Anritsu ML4803A power meter (see Figure 6-3 on page 6-12).
Step 6 F or models 5417A and 5447A: Use the MA4701A power sensor (as in the microwave band adjustment procedure, above).

Step 7 Perform a calibration as instructed in the power meter operation and service manual.

Step 8 N ote that the power meter Cal Factor is set correctly for the test frequency.

Step 9 Connect the power meter sensor to the 54XXA RF OUTPUT connector.

Step 10 Press the 54XXA RF ON/OFF key to OFF. Zero the power meter, and then press RF ON/OFF key to ON.
Step 11 Adjust variable resistor R56 to obtain a power meter reading equal to the 54XXA reset power level $\pm 0.5 \mathrm{dBm}$. These levels are listed in Table 6-4 (page 6-13).

Step 12 Reduce the 54XXA RF output power by 10 dB .

Step 13 Adjust variable resistor R190 to obtain a power meter reading equal to the 54XXA set power level $\pm 0.5 \mathrm{dBm}$.

Step 14 Adjustments R56 and R190 are interactive. Therefore, set RF output power to reset level (Table 6-4) and repeat steps 8 through $\mathbf{1 0}$ until both power meter readings are within $\pm 0.5 \mathrm{dBm}$ of 54XXA indicated RF output power.
Step 15 Disconnect the power meter from the 54XXA.

ALC Operating Point Adjustment

Proceed as follows:
Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation).
For models 5417A and 5447A, set for 10 MHz to 2.0 GHz .
RF Power Output: 2 dB abovereset power level; see Table 6-4 (page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points : 401
Graticule: ON

Step 3 Set Oscilloscope as follows:
Horizontal Sweep: X-Y mode
Channel A vertical sensitivity: 1V/div
Channel B vertical sensitivity:
$0.5 \mathrm{~V} / \mathrm{div}$ (with X10 probe)
CH A input: DC
CH B input: DC
Display: CH A and CH B On

[^0]500 MHz AND 25 MHz MARKER ADJUSTMENT

Use this procedure to make adjustments to the 500 MHz and 25 MHz marker assemblies (on the RF Deck) and to the A6 ALC/F requency Instruction PCB. Perform this procedure only if:
$\square$ The unit is a model 5417A through 5447A. (F or models 5407A, 5409A, and 5411A, go to paragraph 6-10 on page 6-31).
$\square$ The unit displays frequency errors.
$\square$ One or more RF Deck components have been replaced.
Measurement The procedures presented below use a special Technique

500 MHz
Marker
Adjustment

54XXA operating mode that displays the 500 MHz and 25 MHz markers on the internal monitor. The marker waveforms are presented on a screen display with the horizontal axis graduated in frequency units. (These units are meaningless and are used only to quantize the waveform width.)

During this procedure if the 54XXA does not display the marker(s) as described it is probably due to a failure to frequency lock with the current marker adjustment settings. To overcome this problem, adjust the 500 MHz and 25 MHz marker sensitivity variable resistors until markers are displayed and then press the SELF TEST key. The 54XXA will perform a major frequency calibration and produce an accurate display.

Proceed as follows:
Step 1 Disconnect any detectors connected to the signal channel inputs.
Step 2 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press SELECT.

Step 3 Set channel 1 to measure power from signal channel INPUT A . Turn channel 2 measurement off.
Step 4 Set the 54XXA for the Service Mode of operation, as follows: Press the SELF TEST key; when the HOLD LED flashes during the self test, quickly press the FREQUENCY, MARKERS, and LEVELING keys in sequence. The 54XXA will now display the main service mode menu.
Step 5 Press the DATA ENTRY "2" key to select "diagnostic markers" sequence.

Table 6-5. 500 MHz Markers LBE

| Adjustment Frequenies |  |
| :--- | :---: |
| 54XXA Model | Set <br> Frequency <br> (GHz) |
| 5417A, 5419A, | 2.500 |
| 5437A, and 5447A | 8.500 |
| 5428A | 12.500 |
| 5430 A | 10.500 |
| 5431 A | 17.500 |
| 5436 A |  |

Figure 6-4. Typical Low Band Edge 500 MHz Marker

Step 6 Press the DATA ENTRY "1" key to activate the marker display.

Step 7 Press the SELF TEST key, which will normalize the 54XXA display. The display should be a flat line with wide and narrow pips that represent 500 MHz markers and 25 MHz markers, respectively. (If the 54XXA fails self test, press the SELECT key to obtain a measurement display.)

## NOTE

The 500 M HZ markers are one graticle division in height; the 25 MHz markers are one-half division (Figure 6-4).

Step 8 Press the OUTPUT POWER key (on) and verify that the output power is at the reset power level (Table 6-4 on page 6-13).
Step 9 Press the FREQUENCY key and select CENTER/WIDTH mode; set WIDTH to 50 MHz . Set CENTER frequency to the first full 500 MHz point above the low band edge frequency of the unit (Table 6-5).
Step 10 The 500 MHz marker waveform should be displayed on the 54XXA screen (Figure 6-4). The waveform should have a displayed width between " 12 MHz " and " 26 MHz ." Use the cursor and delta cursor to measure the waveform width, as necessary.
Step 11 If the marker width does not require adjustment, go to step 13. Otherwise, proceed as follows:
F or all models except 5437A and 5447A:
Carefully remove the cover of the 500 MHzIF Amplifier module, which is located on the side of the RF Deck. I dentify the marker sensitivity variable resistor (located above U1) and go to step 12.
F or models 5437A and 5447A: Locate the access hole for the marker sensitivity variable resistor that is located on the side of the 500 MHz IF Amplifier module housing. Proceed with next step.

Table 6-6. 500 MHz Markers HBE Adjustment Frequencies

| 54XXA Model | Set <br> Frequency <br> $(\mathbf{G H z})$ |
| :--- | :---: |
| 5417 A and 5419A | 8.000 |
| 5428 A | 12.000 |
| 5430 A | 19.500 |
| 5431 A | 15.500 |
| 5436 A | 26.000 |
| 5437 A and 5447A | 19.500 |

Table 6-7. Power Set Levels for M arkers Power Sensitivity Check

| 54XXA Model | Without <br> Atten. | With <br> Atten. |
| :--- | :---: | :---: |
| 5417A thru <br> 5431A, 5437 A, <br> and 5447A | 0.0 dBm | -3.0 dBm |
| 5436A | -3.0 dBm | -6.0 dBm |

Step 12 Adjust the marker sensitivity variable resistor for a waveform width between 12 MHz and 26 MHz . (The optimum width for these markers is as wide as possible - up to 26 MHz - without generating spurious markers elsewhere in the band.)
Step 13 For all models, set the center frequency to the first 500 MHz point below the upper band edge frequency of the unit (Table 6-6). The high frequency marker display should resemble that shown in Figure 6-4. (F or models 5417A and 5419A, the waveform width will typically be reduced.)

Step 14 Confirm that the marker displayed has a width of between 12 MHz and 26 MHz . For all models, except 5437A and 5447A: If the width is incorrect, readjust the marker sensitivity as in step 11.
Step 15 For models 5437A and 5447A: If width is incorrect: adjust the marker tracking potentiometer R21 (which is the white potentiometer located below the 500 MHz RF module on the RF deck).

Step 16 Press the OUTPUT POWER key and set the power level as shown in Table 6-7. Repeat steps 9 through 15 until the marker widths are within 12 MHz to 26 MHz .
Step 17 Set the 54XXA to the reset power level (Table 6-4 on page 6-13), and set the CENTER frequency per Table 6-5 (step 9).
Step 18 Observe that the marker width is between 12 MHz and 26 MHz .

Step 19 Set the center frequency to every 500 MHz point throughout the frequency band of the unit $(2.5 \mathrm{GHz}, 3.0 \mathrm{GHz}$, 3.5 GHz , etc, for models 5417A and 5447A). Observe at each point that the marker width is between 12 MHz and 26 MHz .

Table 6-8. 25 MHz Markers LBE Adjustment Frequency

| 54XXA Model | Set <br> Frequency <br> $(\mathrm{GHz})$ |
| :--- | :---: |
| $5417 \mathrm{~A}, 5419 \mathrm{~A}$, <br> 5437A, and 5447A | 2.200 |
| 5428A | 8.200 |
| 5430A | 12.600 |
| 5431A | 10.200 |
| 5436A | 17.200 |

Table 6-9. 25 Mhz Markers HBE Adjustment Frequency

| 54XXA Model | Set <br> Frequency <br> (GHz) |
| :--- | :---: |
| 5417A and 5419A | 8.200 |
| 5428A | 12.200 |
| 5430A | 19.800 |
| 5431A | 15.800 |
| 5436A | 26.300 |
| 5437A and 5447A | 19.800 |

Step 20 Press the OUTPUT POWER key and again set the power as shown in Table 6-7. Repeat steps $\mathbf{1 7}$ through 19.
Step 21 Press the SELF TEST key and confirm that no 500 MHz frequency calibration failures occur during the self test sequence.

25 MHZ
Marker Adjustment

Proceed as follows:
Step 1 Set 54XXA as in steps 1 through 8 of the 500 MHz M arker Adjustment procedure (page 6-15). Refer also to the M easurement Technique paragraph.

Step 2 Press the FREQUENCY key and select CENTER/ WIDTH mode; set WIDTH to 400 MHz . Set CENTER frequency 200 MHz above the low band edge frequency of the unit (Table 6-8).
Step 3 The 25 MHz markers should now be displayed on the channel 1 trace. A marker should be located at each 25 MHz point and there should be no spurious markers in between locations. Use the cursor as necessary to identify each 25 MHz point.

Step 4 If the marker display is correct, go to step5, otherwise, proceed as follows: Carefully remove the six screws that secure the cover of the 25 MHz IF Amplifier module (located on the side of the RF Deck) and remove the cover.
On the IF amplifier PCB, adjust the marker sensitivity variable resistor (located next to U1) for a correct marker display (step 3).

Step 5 Set the center frequency to 200 MHz below the upper band edge frequency (Table 6-9).
Step 6 Verify that the markers displayed are located at each 25 MHz point and there are no spurious markers. If display is correct, proceed to step 8, otherwise perform the next step.

Step 7 On the A6 ALC/F requency Instruction PCB, adjust the frequency compensation variable resistor (R80) as follows: Adjust R80 until markers just begin to appear and note setting. Continue adjustment in same direction until spurious markers appear. Then adjust R80 half way between the two points noted.
If difficulty is experienced when performing steps $\mathbf{2}$ through $\mathbf{7}$, then do as follows:

Remove the VCO/PA Divider Module cover plate.
Set the 54XXA as in step 2. Then adjust C16 in the divider module to improve the 25 MHz marker display. (C16 is the only variable capacitor in the module.)

Step 8 Press the OUTPUT POWER key and set the power level as shown in Table 6-7 (page 6-22). Repeat steps 2 through 7 to verify correct marker display.
Step 9 Again set the center frequency per Table 6-8. Set WIDTH to 0.005 GHz ( 5 MHz ).
Step 10 The 25 MHz marker waveform should be displayed on the 54XXA screen as shown in Figure 6-5. The waveform should have a displayed width between 1.0 MHz and 2.0 MHz. Use the cursor and delta cursor to measure the width of the markers, as necessary.

Step 11 If the marker width is incorrect, readjust the 25 MHz marker sensitivity variable resistor slightly (step 4).

Step 12 Set the center frequency as per Table 6-9. Observe that the displayed marker has a width of between 1.0 MHz and 2.0 MHz . If the marker width is incorrect, readjust the A6R80 frequency compensation variable resistor slightly.
Step 13 Set the 54XXA to the reset power level (Table 6-4 on page 6-13). Repeat steps 9 through 12.
Step 14 Set the center frequency as per Table 6-8. Increase the center frequency in 0.4 GHz steps throughout the frequency range of the unit. At each step, verify that markers are present every 25 MHz and that there are no spurious markers.

Step 15 Again set the power as shown in Table 6-7 (on page 6-22). Repeat step 14.
Step 16 For models 5437A and 5447A: If the A6R80 frequency compensation variable resistor was adjusted when setting up the 25 MHz markers (step 7), repeat steps 9 through 21 of the 500 MHz Marker Adjustment procedure (page 6-16) before proceeding with the next procedure.

| 1: TRANSMSSN (A)       <br> 2: OFF       <br>   $0.1 \mathrm{~dB} /$ DIV OFFSET -59.7 dB    <br>        <br>        <br>        <br>        <br>        <br>        <br>        <br>        <br> CENTER: 4.2500 GHz       |
| :--- |

Figure 6-5. Typical 25 MHz Marker Display

Use this procedure to check the 25 MHz markers throughout the heterodyne band of models 5417A and 5447A. F or models other than 5417A and 5447A, proceed to paragraph 6-9.

This procedure uses the same measurement technique as used in the 500 MHz and 25 MHz marker adjustment procedure to verify that the heterodyne band 25 MHz markers are present and of the correct width. If any problems are found, the unit is defective and no adjustment should be attempted.

Procedure Step 1 Set the 54XXA as in steps 1 through 8 of the 500 MHz and 25 MHz marker adjustment procedure (page 6-20).
Step 2 Press the FREQUENCY key and select CENTER/WIDTH mode; set WIDTH to 0.25 GHz . Set CENTER frequency to the first value listed in Table 6-10.

Step 3 The 25 MHz markers should be displayed on the channel 1 trace. Verify that there is a marker at each 25 MHz point and there are no spurious markers. Use the cursor as necessary to identify each 25 MHz point.
Step 4 Set the center frequency to each of the remaining frequencies in Table 6-10. Verify the markers as in step 3.
Step 5 Press the OUTPUT POWER key and set the power level to 0 dBm . Repeat steps 2 through 4.

This completes the heterodyne band 25 MHz markers verification check for models 5417A and 5447A.

Table 6-10. Set Frequencies for HeterodyneBand Markers Verification Check

| Test | Set Frequency <br> $(\mathbf{G H z})$ | Test | Set Frequency <br> $(\mathrm{GHz})$ |
| :---: | :---: | :---: | :---: |
| 1 | 0.135 | 6 | 1.100 |
| 2 | 0.300 | 7 | 1.300 |
| 3 | 0.500 | 8 | 1.500 |
| 4 | 0.700 | 9 | 1.700 |
| 5 | 0.900 | 10 | 1.900 |

## ALC/RF POWER ADJUSTMENT FOR MICROWAVE BAND MODELS

## 6-9 aLC/RF POWER ADJUSTMENT FOR MICROWAVE BAND MODELS

Use this procedure to make (final) adjustments to the A6 ALC/Frequency Instruction PCB for models 5417A through 5447A. For models 5407A, 5409A, and 5411A, go to paragraph 6-11, ALC/RF Power Adjustment F or RF Band Models, which is located on page 6-31.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. All variable resistors ( Rx ) and test points (TPx) referred to in this procedure are on the A6 ALC/ Frequency Instruction PCB. The variable resistor designations ( Rx ) referenced in the following procedures are for the D35429-3A version of the A6 PCB. For 54XXA's equipped with older versions of the A6 PCB, use the variable resistor designations shown in parenthesis.

Required Equivalent equipment may be used - refer to paraTest Equipment graph 6-2 and to Table 1-2 (in Chapter I - General Service Information):

- Power Meter, with suitable matching power sensor (Figure 6-3)
$\square$ Digital Voltmeter, with 4-1/2 digits resolution (Table 1-2)
$\square$ Oscilloscope, dual channel with two X10 probes (Table 1-2)
- WILTRON RF Detector - to match 54XXA model (Table 1-2)


## A6 PCB Configuration

Verify the jumper configuration of the A6 PCB per table below.

Table 6-11. J umper Configuration for A6 PCB's*

| 54XXA <br> Model | PCB Jumpers <br> (All versions) |  | D35429-3A PCB <br> Jumpers |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | J5 | J6 | J7 | J8 | J9 |
| 5417A | $2 \& 3$ <br> (bottom) | $2 \& 3$ <br> (bottom) | 1 \& 2** | $2 \& 3$ | $1 \& 2$ |
| 5447A | $2 \& 3$ <br> (bottom) | $1 \& 2$ <br> (top) | $1 \& 2^{* *}$ | $2 \& 3$ | $2 \& 3$ |
| All Others | $1 \& 2$ <br> (top) | $2 \& 3$ <br> (bottom) | $1 \& 2^{* *}$ | $2 \& 3$ | either |

* For D35429-4A, -5A, -6A, \&-7A PCB's, remove links from DaughterBoard if performing adjustment prior to Temperature Compensation procedure.
** Use pins $2 \& 3$ if performing adjustment prior to Temperature Compensation procedure.

Table 6-12. 54XXA Leveled Power Variation Specifications (Microwave Modeds)

| $54 X X A$ Model | Without <br> Atten | With <br> Atten |
| :--- | :---: | :---: |
| $5417 \mathrm{~A}, 5430 \mathrm{~A}$, <br> and 5437 A | $\pm 0.5 \mathrm{~dB}$ | $\pm 1.0 \mathrm{~dB}$ |
| $5419 \mathrm{~A}, 5428 \mathrm{~A}$, <br> and 5431 A | $\pm 0.4 \mathrm{~dB}$ | $\pm 0.9 \mathrm{~dB}$ |
| 5436 A | $\pm 1.0 \mathrm{~dB}$ | $\pm 2.5 \mathrm{~dB}$ |
| 5447 A | $\pm 0.75 \mathrm{~dB}$ | $\pm 1.0 \mathrm{~dB}$ |

## Reference Voltage Adjustment

Power
Output
Adjustment

If the ALC Pre-Adjustment procedure (paragraph 6-5) was performed for the unit being adjusted, proceed to the Microwave Band Adjustment Procedure below. Otherwise, perform the Reference Voltage Adjustment procedure contained in paragraph 6-5 (page 6-11), and then continue below.

The pre-adjustment and final adjustment procedures for power output adjustment are identical. Perform the procedure in paragraph 6-5 (page 6-12) at this time as the final adjustment. If the pre-adjustment procedure was performed previously, perform it again to verify the adjustments and to make minor corrections, as required. Then proceed to the next procedurebelow.

## ALC Flatness Adjustment

Proceed as follows:
Step 1 Press the SYSTEM MENU key. Select RE-

SET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.
Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation). For models 5417A and 5447A, set START frequency to 2.0 GHz .
RF Power Output: 5 dB below Reset Power for model (refer to Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points: 401
Graticule: ON

Step 3 Connect an RF detector that matches the model being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel. Press the AUTOSCALE key for channel 1.
Step 4 Observe the channel 1 trace and adjust A6R 90 to obtain a flat trace per the output power flatness specifications in Table 6-12. If a flat trace can not be obtained, move jumper A6P2 to the other end of header J 1 and repeat adjustment of R90.

ALC Operat- Proceed as follows: ing Point Adjustment

Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key.

Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation). For models 5417A and 5447A, set START frequency to 2.0 GHz .
RF Power Output: 2 dB abovereset power level (refer to Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points : 401
Graticule: ON

Step 3 Set Oscilloscope as follows:
Horizontal Sweep: X-Y mode
Channel A vertical sensitivity: 1V/div
Channel B vertical sensitivity:
$0.5 \mathrm{~V} / \mathrm{div}$ (with X10 probe)
CH A input: DC
CH B input: DC
Display: CH A and CH B On

Step 4 Press the 54XXA channel 1 AUTOSCALE key (on).
Step 5 Connect oscilloscope CH A input to the 54XXA rear panel HORIZONTAL OUTPUT connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen.

Step 6 Connect CH B probe to A6TP28; connect the probe ground clip to the 54XXA chassis. The oscilloscope will display a waveform with a negative dc component.
Step 7 F or models 5417A through 5436A: Adjust A6R133 to move the oscilloscope trace more positive until the trace oscillates and/or the 54XXA UNLEVELED LED lights. Now adjust R133 back two turns (trace more negative).

Step 8 For models 5437A and 5447A: Adjust R31 on the multi-band controller to move the oscilloscope trace more positive until the trace oscillates and/or the 54XXA UNLEVELED LED lights. Now adjust R31 back two turns (trace more negative).
Step 9 Reduce the power output level by 12 dB . Observe the oscilloscope display and verify that there are no oscillations present. If oscillations are present, readjust R133 (R31 for 5437/47A) negative or positive until the oscillation stops. Continue the adjustment one turn past the point where oscillation stops.
Step 10 If potentiometer R133 (R31) was readjusted in step 9, again set the output power level to 2 dB above the reset level and confirm no oscillations are present.

For all mi crowave band models except models 5417A and 5447A, go to paragraph 6-11 (page 6-37). For these two models, perform go to the next paragraph.

## ALC/RF POWER ADJUSTMENT FOR RF BAND MODELS

## 6-10 <br> ALC/RF POWER ADJUSTMENT FOR RF BAND MODELS

Use this procedure to make (final) adjustments to the A6 ALC/Frequency Instruction PCB for models 5407A through 5411A. Use this procedure also for the RF (heterodyne) band of models 5417A and 5447A.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. All variable resistors ( $R x$ ) and test points (TPx) referred to in this procedure are on the A6 ALC/ Frequency Instruction PCB. The variable resistor designations ( Rx ) referenced in the following procedures are for the D35429-3A version of the A6 PCB. For 54XXA's equipped with older versions of the A6 PCB, usethe variable resistor designations shown in parenthesis.

| Required | Refer to paragraph 6-5 on page 6-10. |
| :--- | :--- |
| Test Equip- |  |
| ment |  |

A6 PCB Con- Verify the jumper configuration of the A6 PCB per table below.

Table 6-13. J umper Configuration for A6 PCB's* for RF Band Models

| PCB Jumpers <br> (All versions) |  | D35429-3A PCB <br> Jumpers |  |  |
| :---: | :---: | :---: | :---: | :---: |
| J5 | J6 | J7 | J8 | J9 |
| $1 \& 2$ <br> (top) | $2 \& 3$ <br> (bottom) | $1 \& 2^{* *}$ | $1 \& 2$ | $2 \& 3$ |

* For D35429-4A, -5A, -6A, \&-7A PCB's, remove links from DaughterBoard if performing adjustment prior to Temperature Compensation procedure.
** Use pins 2 \& 3 if performing adjustment prior to Temperature Compensation procedure.


## figuration

Power
Output
Adjustment

The pre-adjustment and final adjustment procedures for power output adjustment are identical. Perform the Power Output Adjustment procedure for RF models in paragraph 6-6 on page 6-17 at this time as the final adjustment. If the pre-adjustment procedure was performed previously, perform it again to verify the adjustments and to make minor corrections, as required.

ALC Flatness Proceed as follows:
Adjustment
Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.
Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation).
For models 5417A and 5447A, set sweep 0.01 to 2.0 GHz
RF Power Output: 5 dB below Reset Power for model (refer to Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points : 401
Graticule: ON

Step 3 Connect a RF detector that matches the model being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel. Press the AUTOSCALE key for channel 1.
Step 4 Observe the channel 1 trace and adjust A6R91 to obtain a flat trace per the output power flatness specifications listed in Table 6-14. Press the AUTOSCALE key to increase the display resolution, as necessary. If a flat trace can not be obtained, move jumper A6P4 to the other end of header J 4 and repeat adjustment of R91.

Table 6-14. 54XXA Leveled Power Variation Specifications (RF Models)

| 54XXA <br> Model | Output <br> Z | Without <br> Attenuator | With <br> Attenuator |
| :---: | :---: | :---: | :---: |
| 5407 A | $50 \Omega$ | $\pm 0.3 \mathrm{~dB}$ | $\pm 1.0 \mathrm{~dB}$ |
|  | $75 \Omega$ | $\pm 0.5 \mathrm{~dB}$ | $\pm 1.2 \mathrm{~dB}$ |
|  | $50 \Omega$ | $\pm 0.4 \mathrm{~dB}$ | $\pm 1.1 \mathrm{~dB}$ |
|  | $75 \Omega$ | $\pm 0.6 \mathrm{~dB}$ | $\pm 1.3 \mathrm{~dB}$ |
| 5411 A | $50 \Omega$ | $\pm 0.6 \mathrm{~dB}$ | $\pm 1.3 \mathrm{~dB}$ |
|  | $75 \Omega$ | $\pm 0.8 \mathrm{~dB}$ | $\pm 1.5 \mathrm{~dB}$ |

Step 5 F or models 5417A and 5447A equipped with an internal attenuator, go to the ALC Operating Point Adjustment (next page). For models 5417A and 5447A without an attenuator, go to step 7.
Step 6 F or models 5407A, 5409A, and 5411A: Set the power output level to 2 dB above the reset power level and press the AUTOSCALE key for channel 1. Adjust R112 fully clockwise. If oscillations are present on the trace, adjust R183 (R216) until the oscillations stop. Then go to the ALC Operating Point Adjustment.

## NOTE

If the A6 PCB is equipped with a daughter-board, R216 will be located on the daughter-board.

Step 7 F or models 5417A or 5447A, set the STOP frequency to the upper band edge frequency (8.6 GHz and 20.0 GHz , respectively). Set the power output level to the reset power level. Press the AUTOSCALE key for channel 1.
Step 8 Turn the Main and Relative cursors on and measure the power variation by reading the lowest and highest points on the trace. Verify that the measurement is within the output power flatness specification listed in Table 6-14. Readjust R90 or R91, as necessary.

Step 9 Reduce the power output level by 10 dB , and press the AUTOSCALE key for channel 1. Repeat the power output variation measurement, per step 8; readjust R90 or R91, as necessary.
Step 10 Again set the power output level to the reset value. Repeat steps 8 and 9, as necessary, until no further adjustment is required.

ALC Operat- Proceed as follows:
ing Point Adjustment

Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.
Step 2 Set 54XXA as follows:
Frequency: Full-band sweep (per front panel designation). For models 5417A and 5447A, set sweep 0.01 to 2.0 GHz .
RF Power Output: 2 dB abovereset power level (refer to Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Data Points : 401
Graticule: ON

Step 3 Set Oscilloscope as follows:
Horizontal Sweep: X-Y mode
Channel A vertical sensitivity: 1V/div
Channel B vertical sensitivity:
$0.5 \mathrm{~V} / \mathrm{div}$ (with X10 probe)
CH A input: DC
CH B input: DC
Display: CH A and CH B On
Step 4 Connect a RF detector that matches the model being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel. Press the AUTOSCALE key for channel 1.

Step 5 Connect oscilloscope CH A input to the 54XXA rear panel HORIZONTAL OUTPUT connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen.

Step 6 Set Channel B trace to center screen. Use a X10 probe to connect to A6TP28. (Connect the probe ground clip to the 54XXA chassis.) The oscilloscope will display a waveform with a negative dc component.
Step 7 For models 5417 and 5447A, go to step 10.

## ALC/RF POWER ADJUSTMENT FOR RF BAND MODELS

Step 8 F or models 5407A, 5409A, and 5411A: Adjust A6R183 (R216) until the waveform DC component value is -3.5 V $\pm 0.5 \mathrm{~V}$, as indicated by the oscilloscope trace. Note that this value is nominally 2.5 V below the -1 V "Upper Trip" value shown in Figure 6-6. This difference value is labeled " $A$ " in Figure 6-6. Verify that there are no oscillations present on the trace.


Figure 6-6. RF Models ALC Operating Point Adjustment Point Diagram

Step 9 Reduce the power output level 12 dB and measure the waveform DC component. It should be-5.5V $\pm 0.5 \mathrm{~V}$ (i.e., nominally 2.5 V above the-8V "Lower Trip" value). If so, the adjustment is complete.

Otherwise, note the difference between the measured DC component value and the lower trip value (labeled "B" in figure). Adjust A6R183 (R216) so that difference value " $A$ " (from step 8) is within $\pm 0.5 \mathrm{~V}$ of difference value "B." (from step 9).

Step 10 F or models 5417 and 5447A: Verify that there are no oscillations present on the oscilloscope trace and that the 54XXA UNLEVELED LED does not light. If either condition is present, adjust R133 (for 5417A) or R31 on the multi-band controller (for 5447A) to move the oscilloscope trace slightly more negative until the oscillation and or unleveled conditions stops.

Step 11 Reduce the power output level by 12 dB . Verify that no oscillation or unleveled condition is present. If either condition is present, adjust R133 (for 5417A) or R31 on the multi-band controller (for 5447A) to move the oscill oscope trace slightly more negative until the oscillation and or unleveled conditions stops.
Step 12 For all models: Remove the detector from the RF OUTPUT connector and verify that the UNLEVELED LED remains off.

Step 13 Again set the power output level to 2 dB above the reset value. Verify that the UNLEVELED LED remains off.

For models 5407A, 5409A, and 5411A, go to paragraph 6-10. F or models 5417A and 5447A, go on to the next procedure.

## 6-11 band switch-point ADJUSTMENT

## BAND SWITCH POINT <br> ADJUSTMENT

This procedure ensures that the power difference at the 2.0 GHz band switch point of models 5417A and 5447A is reduced to a minimum.

Procedure Step 1 Press the SYSTEM MENU key. Select RESET and press the SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 2 Set 54XXA as follows:
Channel 1: power mode, INPUT A
Channel 2: OFF
Frequency: Start: 1.950 GHz Stop: $\quad 2.050 \mathrm{GHz}$
RF Power Level : at reset power level (refer to Table 6-4 on page 6-13)
Data Points: 401
Graticule: ON
Step 3 Connect an RF detector that matches the 54XXA being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel.

Step 4 Press the AUTOSCALE key for channel 1.
Step 5 Adjust R56 on the A6 ALC/F requency Instruction PCB until there is no visible step at the 2.0 GHz switch point.
Step 6 Reduce the power output level by 10dB. Press the AUTOSCALE key for channel 1.
Step 7 Adjust R190 on the A6 ALC/F requency Instruction PCB until there is no visible step at the 2.0 GHz switch point.
Step 8 Again set the power output level to the reset value. Repeat steps $\mathbf{5}$ through $\mathbf{7}$ until no further adjustment is required.

Step 9 Set the power output level to 2 dB below the reset value. Verify the RF power difference between the heterodyne band $(<2.0 \mathrm{GHz})$ and the microwave band ( $>2.0 \mathrm{GHz}$ ) does not exceed 1 dB . Repeat at $4 \mathrm{db}, 6 \mathrm{db}$, and 8 dB below reset power level.

## 6-12 <br> TEMPERATURE COMPENSATION ADJUSTMENT

This procedure ensures that the A6 PCB ALC circuits temperature compensation adjustments are properly set. Perform this procedure only if the A6 PCB has been replaced, or if the Down Converter or Directional Coupler on the RF deck have been replaced. The variable resistor designations ( Rx ) referenced in the following procedure are for the D35429-3A version of the A6 PCB. For older versions of the A6 PCB, use the designations shown in parenthesis.

## NOTE

This procedure does not apply for units equipped with D35056-3 and D35056-3 A6 PCB's. If your 54XXA is so equipped, call WILTRON Customer Service (refer to Table 2-1 on page 2-4).

## Required Test Equipment

Equivalent equipment may be used - refer to paragraph 6-2 and to Table 1-2 (in Chapter I - General Service Information):

- Dummy Down Converter Thermistor - WILTRON T38300, or equivalent (see Appendix C).
- Dummy Directional Coupler Thermistor WILTRON T38301, or equivalent (see Appendix C).
$\square$ Power Meter - with suitable matching power sensor (Table 1-2)
$\square$ WILTRON RF Detector - to match 54XXA model (Table 1-2)

Verify the configuration of the A 6 PCB as follows:
$\square$ For D35429-4A, -5A, -6A, \& -7A PCB's, verify that the two links on the daughter PCB have been removed. (These links should have been removed prior to the ALC/Power Output adjustment -refer to paragraph 6-8.) If links are present, remove and put aside for latter use.
$\square$ For D35429-3A PCB's, place jumper J 7 on pins 2 and 3 of P7.

Step 1 If the 54XXA is a 5417A or 5447A, perform steps 2 through 12; for all other models, go to step 12.

Step 2 Press the SYSTEM MENU key. Select RESET and press SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 3 Set 54XXA as follows:
Frequency: CENTER: 2.0 GHz WIDTH: 0.1 GHz
RF Power Output: 5 dB below reset power level (refer to Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Cursors: Main Cursor and RELATIVE Cursor on

Step 4 Connect a RF detector that matches the model being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel. Press the AUTOSCALE key for channel 1.

Step 5 Set Marker M1 to 1.975 GHz in the RF Band and Marker M2 to 2.025 GHz in the Microwave Band. Switch off the 54XXA.

Step 6 Remove the top and side covers of the 54XXA (refer to paragraph 5-2). Disconnect the Down Converter cable at connector J 4 of the A4 M otherboard PCB. Connect one end of the Dummy Down Converter Thermistor, T38300, to the end of the cable, and connect the other end of T38300 to connector J 4. (It is necessary to remove the A5 and A6 PCB's to perform this operation.) Set the T38300 jumper to the "normal" position.

Step 7 Power-up the 54XXA and allow it to warm up for 30 minutes. Press the MARKERS key and note the M1 and M2 marker readings.

Step 8 Turn off the 54XXA. F or units equipped with A6 PCB's, type D35429-4A, -5A, -6A, and -7: connect the two links on the daughter board. F or D35429-3A PCB's, place jumper J 7 on pins 1 and 2 of P 7 . Power-up the unit and allow it to warm up for 10 minutes.

Step 9 Set the T38300 jumper to the "cal" position. Adjust A6R 81 (R104 on the daughter board for older PCB's) so that the RF band marker ( M 1 ) is 0.75 dB less than the value noted down in step $\mathbf{7}$.

Step 10 Disconnect the black wire from the thermistor output of the Directional Coupler on the RF deck. (Refer to Figure 5-7b on page 5-19.) Connect the Dummy Directional Coupler Thermistor, T38301, be tween the black wire and the 54XXA chassis (ground). Adjust A6R81 (R104) so that the microwave band marker (M2) is 0.35 dB less than the value noted in step 7.

Step 11 Turn off the 54XXA and remove the T38300 and T38301 fixtures. Reconnect the black wire to the thermistor output terminal of the directional coupler.

Step 12 For all models except 5417A and 5447A: perform the remainder of this procedure, starting with the next step. F or models 5417A and 5447A, go to step 24.

Step 13 Press the SYSTEM MENU key. Select RESET and press SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 14 Set the 54XXA as follows:
Frequency: CENTER: Mid Band Frequency per Table 6-15. WIDTH: 0 GHz
RF Power Output: 5 dB below reset power level (refer Table 6-4 on page 6-13)
Channel 1: power mode, INPUT A
Channel 2: OFF
Cursors: Main Cursor on
Step 15 Connect a RF detector that matches the model being calibrated between the INPUT A connector and the RF OUTPUT connector on the 54XXA front panel. Press the AUTOSCALE key for channel 1.

## ALC TEMPERATURE <br> ADJUSTMENTS

Step 16 F or RF Band models 5407A, 09A, and 11A: Remove the top and side covers of the 54XXA (refer to paragraph 5-2). Disconnect the Down Converter cable at connector J 4 of the A4 M otherboard PCB, and connect one end of the Dummy Down Converter Thermistor, T38300, to the end of the cable.Connect the other end of T38300 to connector J 4. (It is necessary to remove the A5 and A6 PCB's to perform this operation.) Set the T38300 jumper to the "cal" position.

Step 17 For Microwave Band models 5419A through 5437A : Remove the top and side covers of the 54XXA (refer to paragraph 5-2). Disconnect the black wire from the thermistor output the Directional Coupler on the RF deck. (Refer to Figures 5-8b and 5-9b on pages 5-21 and $5-23$, as appropriate.) Connect the Dummy Directional Coupler Thermistor, T38301, between the black wire and the 54XXA chassis (ground).

Step 18 Power-up the 54XXA and allow it to warm up for 30 minutes. Press the CURSOR key and note cursor reading.

Step 19 Turn off the 54XXA. F or units equipped with A6 PCB's, type D35429-4A, -5A, -6A, and -7: connect the two links on the daughter board. For D35429-3A PCB's, place jumper J 7 on pins 1 and 2 of P7. Power-up the unit and allow it to warm up for 10 minutes.

Step 20 F or Microwave Band models 5419A through 5437A : Adjust R104 (R81 on the daughter board for older PCB's) so that the cursor reading is 0.3 dB less than the value noted down in step 18.

Step 21 For RF Band models 5407A, 5409A, and 5411A: Adjust R81 (R104 on the daughter board) so that the cursor reading is 0.55 dB less than the value noted down in step 18.

Step 22 Turn off the 54XXA and remove the T38300 or T38301 fixtures. For microwave band models, reconnect the black wire to the thermistor output terminal of the directional coupler.

Step 23 For RF Band models 5407A, 5409A, and 5411A: Go to step 27.

Step 24 For all Microwave Band models except 5417A and 5447A: Set the unit to the lower band-edge frequency (per front panel model designation), and put unit in CW mode. For models 5417A and 5447A: Set frequency to 2.0 GHz , and put unit in CW mode.

Step 25 Measure the RF output power level using a power meter, and verify that the power meter reading is within the specifications listed in Table 6-16. If necessary, adjust the RF output power level using A6R 62.

Step 26 Reduce the 54XXA power output level by 10 dB , and verify that the power meter reading is within the specifications listed in Table 6-16 for minimum ALC level. If necessary, adjust the RF output power level using A6R196.

Table 6-16. Output Power Leve Specifications

|  <br> Model | Output Power Level <br> Without Attenuator |  | Output Power Level <br> With Attenuator |  |
| :--- | :---: | :---: | :---: | :---: |
|  | $@$ Reset Power Level | @ Min ALC Level | @ Reset Power Level | @ Min ALC Level |
| 5407 A, or 5409 A <br> w/ $50 \Omega$ Output | $+12 \pm 1.0 \mathrm{~dB}$ | $+2 \pm 1.0 \mathrm{~dB}$ | $+10 \pm 2.0 \mathrm{~dB}$ | $0 \pm 2.0 \mathrm{~dB}$ |
| 5407 A, or 5409 A <br> w/ $75 \Omega$ Output | $+10 \pm 1.2 \mathrm{~dB}$ | $0 \pm 1.2 \mathrm{~dB}$ | $+8 \pm 2.2 \mathrm{~dB}$ | $-2 \pm 2.2 \mathrm{~dB}$ |
| 5411 A w/ $50 \Omega$ Output | $+12 \pm 1.0 \mathrm{~dB}$ | $+2 \pm 1.0 \mathrm{~dB}$ | $+10 \pm 2.1 \mathrm{~dB}$ | $0 \pm 2.1 \mathrm{~dB}$ |
| 5411 A w/ $75 \Omega$ Output | $+10 \pm 1.2 \mathrm{~dB}$ | $0 \pm 1.2 \mathrm{~dB}$ | $+8 \pm 2.3 \mathrm{~dB}$ | $-2 \pm 2.3 \mathrm{~dB}$ |
| $5417 \mathrm{~A}, 5419 \mathrm{~A}, 5428 \mathrm{~A}$, <br> 5437 A, and 5447 A | $+10 \pm 1.0 \mathrm{~dB}$ | $0 \pm 1.0 \mathrm{~dB}$ | $+7 \pm 2.5 \mathrm{~dB}$ | $-3 \pm 2.5 \mathrm{~dB}$ |
| 5430 A | $+10 \pm 1.0 \mathrm{~dB}$ | $0 \pm 1.0 \mathrm{~dB}$ | $+7 \pm 2.9 \mathrm{~dB}$ | $-3 \pm 2.9 \mathrm{~dB}$ |
| 5431 A | $+10 \pm 1.0 \mathrm{~dB}$ | $0 \pm 1.0 \mathrm{~dB}$ | $+7 \pm 2.7 \mathrm{~dB}$ | $-3 \pm 2.7 \mathrm{~dB}$ |
| 5436 A | $+7 \pm 1.0 \mathrm{~dB}$ | $-3 \pm 1.0 \mathrm{~dB}$ | $+4 \pm 3.3 \mathrm{~dB}$ | $-6 \pm 3.3 \mathrm{~dB}$ |

Step 27 F or models 5417A and 5447A, perform the Band Switch Point Adjustment (paragraph 6-9) and then go to step 29. F or all other microwave models, go to step 29.

Step 28 F or RF Band models: Set the frequency to 50 MHz and put unit in CW mode. M easure the RF output power level using a power meter, and verify that the power meter reading is within specification per Table 6-16. If necessary, - and as appropriate - adjust the reset RF output power level (A6R56), or the minimum ALC power level (A6R190).

Step 29 Press the SYSTEM MENU key. Select RESET and press SELECT key. Select RESTORE DEFAULT SETUP and press the SELECT key.

Step 30 Set the 54XXA as follows:
Frequency: full band sweep
RF Power Output: to maximum. (2 dB abovereset power - see Table 6-4)
Channel 1: power mode, INPUT A
Channel 2: OFF
Step 31 Connect an RF detector from the RF output to INPUT A. Press Autoscale and confirm the UNLEVELED LED in not lit.

Step 32 Set the RF power 12 dB below the power level set in step 30. Press AUTOSCALE and confirm the UNLEVELED LED is not lit.

The temperature compensation procedure is completed. No further adjustments should be made.

# Appendix A RF Detector Diode Replacement Procedures 

##  REPLACEMENT PROCEDURES

Series 5400-71XXX RF Detectors and series 560-7XXX RF Detectors are used with 54XXA systems. Paragraph A-2 contains the procedure for replacing defective detector diodes in model 5400-71B75 RF Detectors, and paragraph A-2 contains the procedure for replacing detector diode modules in series 560-7XXX RF Detectors.

## NOTE

Models 5400-71N50 and 5400-71N75 RF Detectors do not have field-replaceable detector diodes. Series $5400-6 \mathrm{NXXX}$ Autotesters also do not.

Required Ad- Whenever the detector diode (or diode module) of justments these RF Detectors is replaced, the two potentiometers that are part of the rf detector PCB subassembly (Figures A-1 and A-4) must be readjusted. The potentiometer readjustment is done after the defective diode is removed, but before the replacement diode is installed.

Test Equip- The procedure in this appendix require a digital ment Re- multimeter (DMM) that has a display resolution of quired
at least 3-1/2 digits. (J ohn Fluke M odel 8840A, or equivalent).

REPLACEMENT OF DETECTOR DIODE FOR MODEL 5400-71B75 RF DETECTOR


Figure A-2. RF Detector Cable Connector Pin Orientation

The model 5400-71B75 RF Detector is equipped with a field-replaceable detector diode. To replace, proceed as follows:

Step 1
Unfasten the four detector housing top cover retaining screws. Remove the top cover.
Unplug the defective diode (Figure A-1) from the PCB subassembly and remove.


Figure A-1. Mode 5400-71B75 RF Detector Housing Layout Diagram

Step 3 Set potentiometer R1 fully clockwise (maximum resistance).
Step 4 Connect the DMM leads between pins 1 and 2 of the rf detector cable connector (Figure A-2). Measure the resistance value, which is the maximum resistance of R1 (approximately $40.5 \mathrm{k} \Omega$ is typical). Record this value; it will hereafter be referred to as "RT".
Step 5 Obtain the " $K$ " value from the replacement diode container label (Figure A-3).
Step 6 Compute the set value for R1 as follows:

$$
\mathbf{R} \mathbf{1}_{\text {set }}=\mathbf{K} \times \mathbf{R} \mathbf{T}
$$

Adjust R1 counterclockwise until the DMM indicates the $R 1_{\text {set }}$ value calculated in step 6.

## DETECTOR DIODE REPLACEMENT MODEL 5400-71B75 RF DETECTOR

Step 8 Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.

Step 9

Step 10

Step 11

Step 12

Obtain the "R o" value from the replacement diode container label.

Adjust R4 until the DMM indicates the "Ro" value. Disconnect the DMM.

Orient the cathode end (white dot) of the replacement diode as shown in Figure A-1 (white dot toward centerline of the detector PCB subassembly). Insert the diode into the socket of the PCB subassembly.

Reinstall the top cover, securing it with the four retaining screws. This completes replacement of detector diode.


Figure A-3. Replacement DiodeContainer Label

REPLACEMENT OF DIODE MODULES FOR SERIES 560-7XXX RF DETECTORS

Series 560-7XXX RF Detectors are equipped with a field-replaceable diode module that contains (in addition to the detector diode) a thermistor, a resistor, and two capacitors. To replace, proceed as follows:

Step 1
Unfasten the four detector housing top cover retaining screws. Remove the top cover.

Unfasten the two retaining screws that hold down the rf detector PCB subassembly (Figure A-4).
Step 3

Step 4

Slide the cable retainer out of the rf detector housing assembly. When the cable retainer clears the housing, disconnect the PCB subassembly from the diode module. Remove spring washer.
Remove fiberglass module retainer from detector housing. This retainer can be removed by prying it out using a small screwdriver, or by pulling it out using short, round nose pliers.


Figure A-4. Series 560-7XXX RF Detectors, Exploded View


Figure A-5. RF Detector Cable Connector Pin Orientation

## Step 5

Step 6

Step 7

Step 8

Step 9

Step 10

Step 11

Step 12

Step 13

Step 14

Remove diode module from rear of connector body by pulling it straight out.
Set potentiometer R1 fully clockwise (maximum resistance).
Connect the DMM leads between pins 1 and 2 of the rf detector cable connector (Figure A-5). Measure the resistance value, which is the maximum resistance of R1 (approximately $40.5 \mathrm{k} \Omega$ is typical). Record this value; it will hereafter be referred to as "RT".

Obtain the "K" value from the replacement diode container label (Figure A-6).

Compute the set value for R1 as follows:

$$
\mathbf{R} \mathbf{1}_{\text {set }}=\mathbf{K} \times \mathbf{R} \mathbf{T}
$$

Adjust R1 counterclockwise until the DMM indicates the $\mathrm{R} 1_{\text {set }}$ value calculated in step 9 .
Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.
Obtain the "Ro" value from the replacement diode container label and adjust R4 until the DMM indicates this value. Disconnect the DMM.

Orient detector housing normally (Figure A-4). Insert replacement diode module into rear of connector body so that center lead is on top.
Orient spring washer so that the two curved flanges point toward the rear of the detector housing and are positioned horizontally (i.e., 3 o'clock and 9 o'clock positions).


Figure A-6. Replacement Diode Module Container Label

| Step 15 | Insert fiberglass module retainer between the re- <br> placement diode module and spring washer. Push <br> down on retainer until fully seated. |
| :--- | :--- |
| Step 16 | Orient PCB subassembly normally as shown in Fig- <br> ure A-4 and insert into detector housing so that <br> leads from replacement diode module mate with con- <br> nectors on PCB subassembly. |
| Step 17 | Insert cable retainer into slot in detector housing. |
| Step 18 | Fasten PCB subassembly into detector housing us- <br> ing two retaining screws. |
| Step 19 | Reinstall the top cover, securing it with the four re- <br> taining screws. This completes replacement of detec- <br> tor diode module. |

## APPENDIX B <br> FABRICATION OF RF DETECTOR SIMULATOR

## B-1 rf detector SIMULATOR

The RF detector simulator (T1492) is a special test aid that is used in the adjustments procedure for the series 54XXA Scalar M easurement Systems (refer to Chapter 6, paragraph 6-2). TheT1492 may be fabricated as illustrated in the figure below. Or, it may be purchased from WILTRON as a special order item. Contact your WILTRON sales office for further details.



REAR VIEW

| Reference <br> Designator | Description | WILTRON Part Number |
| :--- | :--- | :--- |
| R1, R2 | Resistor, Metal Film, $1 \mathrm{M} \Omega, 0.1 \%$ | $110-1 \mathrm{M}-0.1$ |
| R3 | Resistor, Metal Film, $5.11 \mathrm{k} \Omega, 1 \%$ | $110-5.11 \mathrm{~K}-1$ |
| - | Connector Plug, <br> Switchcraft, inc., 09CL4M | $551-271$ |

To fabricate the detector simulator, refer to figures above and proceed as follows:

1. Remove screw that secures connector shell to connector assembly.
2. Remove connector assembly from connector shell and note pin numbers located on front of connector.
3. Solder one end of resistor R1 to pin 3.
4. Solder other end of resistor R1 to the shield post.
5. Solder one end of resistor R2 to pin 4.
6. Solder other end of resistor R2 to the shield post.
7. Solder one end of resistor R3 to pin 1.
8. Solder other end of resistor R3 to the shield post. Return wire from shield post back to pin 2 and solder.
9. Insert connector assembly into connector shell and refasten screw.

Figure B-1. Fabrication of T1492 Detector Simulator

## APPENDIX C FABRICATION OF DUMMY THERMISTOR TEST AIDS

## C-1 т38300 DUMMY THERMISTOR TEST AID

The T38300 Dummy Down Converter Thermistor is a special test aid that is used in the Temperature Compensation Adjustment Procedure (Chapter 6, paragraph 6-10). This test aid may be fabricated as shown below; or, it may be purchased from WILTRON as a special order item. Contact your WILTRON sales office for further details.


FABRICATION DETAIL DIAGRAM

Figure C-1. Fabrication of T38300 Dummy Down Converter Thermistor

## DUMMY THERMISTOR

C-2 T38301 DUMMY THERMISTOR TEST AID

The T38301 Dummy Directional Coupler Thermistor is a special test aid that is used in the Temperature Compensation Adjustment Procedure for series 54XXA Scalar M easurement Systems (Chapter 6, paragraph 6-10). This test aid may be fabricated as shown below; or, it may be purchased from WILTRON as a special order item. Contact your WILTRON sales office for further details.


Figure C-2. Fabrication of T38301 Dummy Directional Coupler Thermistor

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[^0]:    Step 4 Connect a suitable detector from the 54XXA RF OUTPUT connector to INPUT A. Press the channel 1 AUTOSCALE key (on).
    Step 5 Connect oscilloscope CH A input to the 54XXA rear panel HORIZONTAL OUTPUT connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen.

    Step 6 Connect CH B probe to A6TP28. Connect the probe ground clip to the 54XXA chassis. The oscilloscope will display a waveform with a negative dc component.
    Step 7 F or models 5407A, 5409A, and 5411A: Adjust R112 to move the oscilloscope trace more positive until the trace oscillates and/or the 54XXA UNLEVELED LED lights. Now adjust R112 back two turns (trace more negative).
    Step 8 For models 5417A and 5447A: Confirm that the UNLEVELED LED does not light and the oscilloscope trace is not oscillating. If either condition exists, adjust R31 on the multi-band controller for 5447A units, or A6R133 for 5417A units, to move the oscilloscope trace slightly more negative until the oscillation and or unleveled conditions stops.
    Step 9 Disconnect the oscilloscope probe and BNC to BNC cable.

    This completes the RF band pre-adjustment procedure. Proceed to the 500 MHz and 25 MHz Marker Adjustment on the next page.

