

# Technical Guide

## GD70 Personal Cellular Telephone

Handheld Portable  
**EB-GD70**

### Specification



	900 MHz	1800 MHz
Frequency range	Tx: 890 - 915 MHz Rx: 935 - 960 MHz	Tx: 1710 - 1785 MHz Rx: 1805 - 1880 MHz
Tx/Rx frequency separation	45 MHz	95 MHz
RF channel bandwidth	200 kHz	
Number of RF channels	124	374
Speech coding	Full rate/Half rate/Enhanced Full rate	Full rate/Half rate
Operating temperature	-10°C to +55°C	
Type	Class 4 Handheld	Class 1 Handheld
RF Output Power	2 W maximum	1 W maximum
Modulation	GMSK (BT = 0.3)	
Connection	8 ch/TDMA	
Voice digitizing	13 kbps RPE-LTP / 13 kbps ACLEP / 5.6 kbps CELP / VSLEP	
Transmission speed	270.3 kbps	
Diversity	Frequency hopping	
Signal Reception	Double superheterodyne	
Intermediate Frequency	Tx 890 - 915 MHz Rx 935 - 960 MHz	Tx 1710 - 1785 MHz Rx 1805 - 1880 MHz
Antenna Terminal Impedance	50 Ω	
Antenna VSWR	<2.1 : 1	
Dimensions	Height: 132 mm Width: 45.5 mm Depth: 19.5 mm	
Volume	125 cc	
Weight	134 g	
Display	Graphical chip on glass liquid crystal, Alphanumeric 16 x 3 characters, 5 icons and 6 x 1 characters	
Illumination	Green: 4 LEDs for the LCD 8 LEDs for the keyboards 1 LED Incoming call Red: 1 LED Charging indicator	
Keypad	17 keys, Navigation key	
SIM	Plug-in type only	
External DC Supply Voltage	5.8 V	
Battery	3.6 V	
Standby Battery Life DRX 9	Battery Pack (EB-BSD70): 100 hrs Battery Pack (EB-BMD70): 105 hrs Battery Pack (EB-BLD70): 180 hrs	
Conversation Battery Life PL 7, DTX 50%	Battery Pack (EB-BSD70): 240 mm Battery Pack (EB-BMD70): 250 mm Battery Pack (EB-BLD70): 430 mm	

Unless stated these specifications are with Battery Pack (EB-BSD70) fitted.  
Battery life figures are dependent on network conditions.

**Panasonic**  
**GSM**

This Technical Guide is copyright and issued on the strict understanding that it is not to be reproduced, copied, or disclosed to any third party, either in whole or part, without the prior written consent of Matsushita Communication Industrial UK Ltd.

Every care has been taken to ensure that the contents of this manual give an accurate representation of the equipment. However, Matsushita Communication Industrial UK Ltd. accepts no responsibility for inaccuracies which may occur and reserves the right to make changes to specification or design without prior notice.

The information contained in this manual and all rights in any designs disclosed therein, are and remain the exclusive property of Matsushita Communication Industrial UK Ltd.

Other patents applying to material contained in this publication:

BULL CP8 PATENTS

Comments or correspondence concerning this manual should be addressed to:

Customer Support Department,  
Matsushita Communication Industrial UK Ltd.,  
Colthrop,  
Thatcham,  
Berkshire.  
RG19 4ZD.  
ENGLAND

© 1998 Matsushita Communication Industrial UK Ltd.

# CONTENTS

<b>1 INTRODUCTION</b>	
1.1 Purpose of this Guide	1
1.2 Structure of the Guide	1
<b>2 INTERFACES AND TEST POINTS</b>	
2.1 Introduction	3
2.2 Interfaces	3
<b>3 RF OVERVIEW</b>	
3.1 Introduction	9
3.2 Functional Description	10
3.3 RF & Accessory Connector	12
<b>4 TRANSMITTER</b>	
4.1 Introduction	13
4.2 Functional Description	13
<b>5 RECEIVER</b>	
5.1 Introduction	15
5.2 Functional Description	15
<b>6 BASEBAND OVERVIEW</b>	
6.1 Introduction	21
6.2 Functional Description of the PCB	21
<b>7 GEMINI</b>	
7.1 Introduction	29
7.2 Functional Description	29
<b>8 VEGA</b>	
8.1 Introduction	33
8.2 Functional Description	33
<b>9 POWER SUPPLIES</b>	
9.1 Introduction	37
9.2 Overview	37
9.3 Power-up	37
9.4 Power-down	38
9.5 Power Management	39
<b>10 ACCESSORIES</b>	
10.1 Handsfree Unit - Circuit Description	43
10.2 Dual Charger	46

This page is left intentionally blank.

# **1 INTRODUCTION**

## **1.1 Purpose of this Guide**

This guide contains technical information for the Panasonic GD70 personal cellular telephone system operating on the GSM network. Procedures for installing, operating and servicing (e.g. disassembly and testing) the telephone system are provided in the associated Service Manual.

## **1.2 Structure of the Guide**

The guide is structured to provide service-engineering personnel with the following technical information on the GSM mobile telephone:

1. Interface details and relevant test points.
2. Functional description of each section of the mobile telephone.
3. Detailed description of each section of the mobile telephone.

This page is left intentionally blank.

## 2 INTERFACES AND TEST POINTS

### 2.1 Introduction

This section provides details on connections between the RF and Baseband PCB and other interfaces on GD70.

### 2.2 Interfaces

SIM 5 V		1		26		SIM CLK
SIM IO		2		27		GND
GND		3		28		SIM RST
GND		4		29		GND
BATID		5		30		IFAGCEN
BAT TEMP		6		31		PLL CLK
VBAT		7		32		PLL SD
VBAT		8		33		PLL STRB
VBAT		9		34		TX PLL EN
VBAT		10		35		GND
GND		11		36		NOT USED
AFC		12		37		BUZZ-
GND		13		38		VIB ON
PARAMP		14		39		OCE
DQ		15		40		LO EN
DQX		16		41		RXON2
DI		17		42		RXON1
DIX		18		43		GND
PCNnGSM		19		44		TXON1
UQX		20		45		PAON
UQ		21		46		GND
UIX		22		47		RF ON
UI		23		48		PLCONT
GND		24		49		GND
OSC_13M		25		50		GND

Figure:1 GD70 Interboard Connector

D70-0201

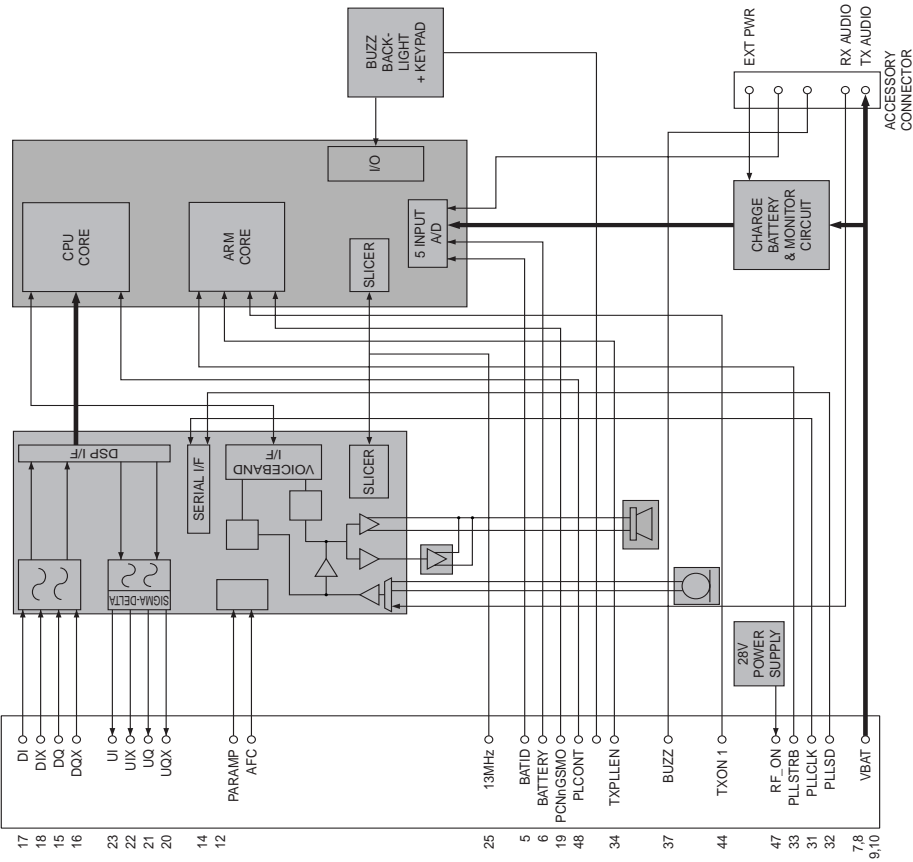
#### 2.2.1 Baseband and RF

This details the 50-way connector between the RF and baseband PCB.

No.	Signal Name	RF <=> LOGIC	Total	Function	Connection	Status
1	SIM_5V	<==	1	5.0 Volt supply for SIM		5 V $\pm$ 5% 20 mA max
2	5V_SIM_IO	<=>	1	SIM Interface: Data	GEMINI pin 100	
3	GND	==>	12	Battery Ground		
4	GND	==>	12	Refer to pin 3		
5	BAT_ID	==>	1	Attached battery type: Li+/No battery or NiMH	VEGA pin 37	H: Li or no battery L: NiMH
6	BAT_TEMP	==>	1	Battery attached/detached detection, battery temperature monitoring	VEGA pin 38	H: Abnormal M: Li or NiMH L: No battery
7	VBAT	==>	4	Battery Supply Voltage		
8	VBAT	==>	4	Refer to pin 7		
9	VBAT	==>	4	Refer to pin 7		
10	VBAT	==>	4	Refer to pin 7		
11	GND	==>	12	Refer to pin 3		
12	AFC	<==	1	Control voltage for 13 MHz TCVCXO		

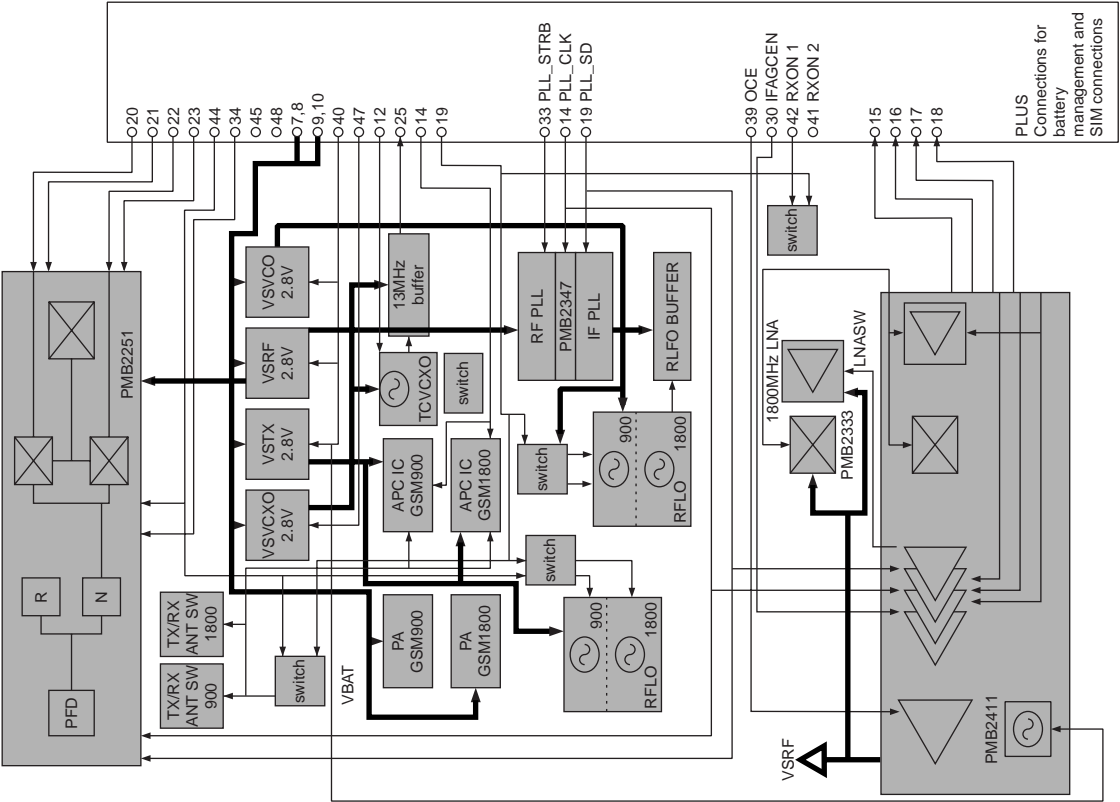
## INTERFACES AND TEST POINTS

No.	Signal Name	RF <=> LOGIC	Total	Function	Connection	Status
13	GND	==>	12	Refer to pin 3		
14	PARAMP	<==	1	Ramping waveform for PA Control Circuit		
15	DQ	==>	1	Downlink Q signal		
16	DQX	==>	1	Downlink nQ signal		
17	DI	==>	1	Downlink I signal		
18	DIX	==>	1	Downlink nI signal		
19	PCNnGSM	<==	1	Select GSM1800 or GSM900 Mode	GEMINI pin 70	H: GSM 1800 L: GSM 900
20	UQX	<==	1	Uplink nQ signal		
21	UQ	<==	1	Uplink Q signal		
22	UIX	<==	1	Uplink nI signal		
23	UI	<==	1	Uplink I signal		
24	GND	==>	12	Refer to pin 3		
25	OSC_13MHZ	==>	1	13 MHz Master Clock		
26	5V_SIM_CLK	<==	1	SIM Interface: Clock	GEMINI	3.25 MHz clock
27	GND	==>	12	Refer to pin 3		
28	5V_SIM_RST	<==	1	SIM Interface: Reset		
29	GND	==>	12	Refer to pin 3		
30	IFAGCEN	<==	1	AGC Serial Interface: Enable	GEMINI pin 62	H: Enabled L: Disabled
31	PLL_CLK	==>	1	PLL & AGC Serial Interface: Clock		
32	PLL_DATA	<==	1	PLL & AGC Serial Interface: Data		
33	PLL_STRB	==>	1	PLL Serial Interface: Enable		H: Enabled L: Disabled
34	TX_PLL_EN		1	Tx PLL Enable	GEMINI pin 61	H: Enabled L: Disabled
35	GND	==>	12	Refer to pin 3		
36						
37	BUZZ-	<==	1	Buzzer On/Off control		
38	VIB_ON	<==	1	Vibrator On/Off control		H: Vibrator On L: Vibrator Off
39	OCE	<==	1	Downlink I/Q dc error offset calibration		
40	LO_EN	<==	1	Enable VSVCO & VSTX Regulators, RF & IF Synthesizer IC		H: Enabled L: Disabled
41	RXON2	<==	1	Enable IF, Demodulator and Baseband stages		H: Enabled L: Disabled
42	RXON1	<==	1	Enable LNA and 1st Mixer & RF LO Buffer		H: Enabled L: Disabled
43	GND	==>	12	Refer to pin 3		
44	TXON1	<==	1	Enable IF Modulator, APC loop		H: Enabled L: Disabled
45	PA_ON	<==	1	Enable VSRF supply to TX buffers		H: Enabled L: Disabled
46	GND	==>	12	Refer to pin 3		
47	RF_ON	<==	1	Enable VSVCO & VSRF Regulators		H: Enabled L: Disabled
48	PL_CONT	<==	1	Select sensitivity of PA Control Circuit		
49	GND	==>	12	Refer to pin 3		
50	GND	==>	12	Refer to pin 3		



D70-0202

Figure:3 Logic board and Interfaces



D70-0203

Figure:2 RF board and Interfaces

## 2.2.2 External Interface

GD70 has two external connectors:

1. a multi-way connector for use with a handsfree data;
2. additional contacts for charging the battery pack while in the desktop charger;


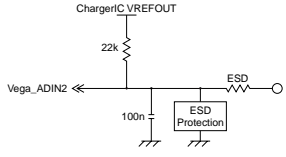

All interfaces are electrically and mechanically compatible with GD70.

### Main Unit <==> External I/O

No.	Name	H/H <==> EXT	Total	Function	H/H Circuit
1	GND	==>	6	Ground	
2	PA_ON	==>	1	Gating of spectrum analyser for Transmitter performance testing L: Off, Hi - Z: On)	
3	NLOGIC_PWR	==>	1	Accessory Power Control signal. In the handsfree this is logical ORed with IGNITION in order that the software can maintain the Handsfree power-on state if the user is in a call and that the IGNITION is switched off. L: Power-on, Hi-Z: Power-off	
4	IGNITION	<==	1	IGNITION is used in 2 cases. 1) Determine the mode of operation of the H/H when the Handsfree accessory is attached. L: At a suitable time enter dummy sleep mode and therefore minimise the drain on the car battery (nLOGIC_POWER = Hi - Z) H: Normal mode 2) Satisfy 2nd of 2 conditions for sending initialise Testset command and entering Testset mode. (see nADP_SENSE for 1st condition) L: Condition 2 satisfied H: Enter Testset mode not satisfied	
5	VBAT	<==>	1	The pin is either an input or an output depending upon the battery connection. 1) Battery/Dummy battery connected: Output supply terminal for attached accessories. 2) No connection: Low current input supply terminal for non-RF performance checking in Testset Mode or Flash programming.	
6	NH/F_SENSE	<==	1	Handsfree sense line L: connected H (internal pull-up): disconnected	
7	NRADIO_MUTE	==>	1	Radio Mute L: mute, Hi-Z: unmute)	
8	RX_AUDIO	==>	1	Accessory Receiving Audio -16 dBm0 = 76.7m Vrms	
9	No connection				
10	EXT-PWR	<==	2	Power supply for battery charging, Power ON/ Off control and accessory control circuits. Voltage: 5.8 ± 0.2 V Current: 650 ± 50 mA	

No.	Name	H/H <=> EXT	Total	Function	H/H Circuit
11	NON_HOOK	<==	1	Indicates if the optional second handset is on or off hook. In handsfree operation, if the optional handset is not fitted this signal defaults to on hook. (Low.)	
12	SERIAL_OUT	==>	1	Downlink Serial Data (Baud rate is same as SERIAL_IN)	
13	SERIAL_IN	<==	1	Uplink Serial Data The baud rate is dependant upon the attached accessory, whether operating in Testset Mode or Flash Downloading. SMS cable: 9600 bps RS232 Direct cable: 38.4 kbps Data adapter: 33.8 kbps Testset: 9600 bps Flash Download: 56 kbps	
14	NADP_SENSE	<==	1	NADP_SENSE has 5 possible states. The state is determined by the value of the pull-down resistor in the attached accessory/testset. NADP_SENSE has 2 purposes as follows: 1) To identify an attached accessory. Open (H): No attached accessory 82 kΩ ± 1% (MH): Headset Adapter 56 kΩ ± 1% (M): SMS Cable 33 kΩ ± 1% (ML): RS232C Direct Cable GND (L): Data Adapter 2) Determine whether the 1st of 2 conditions are satisfied for sending the initialise Testset command on SERIAL_OUT, and entering Testset mode (see IGNITION for 2nd condition). H/MH: Condition 1 satisfied M/ML/L: Enter Testset Mode not satisfied	
15	NH/F_ON	==>	1	Accessory Sending & Receiving Audio paths unmute L: unmute, Hi-Z: mute	
16	GND	==>	6	Refer to pin 1	Refer to pin 1
17	TX_AUDIO	<==	1	Accessory Sending Audio -16 dBm0 = 40.4 m Vrms	
18	GND	==>	6	Ground connection of Dual Charger	Refer to pin 1
19	GND	==>	6	Ground connection of Dual Charger	Refer to pin 1
20	GND	==>	6	Ground connection of Dual Charger	Refer to pin 1
21	GND	==>	6	Ground connection of Dual Charger	Refer to pin 1
22	CHARGE_ON	<=>	1	The Dual Charger shall hold CHARGE_ON to the middle level unit a H/H is inserted into the front slot. H: 2.0<=V<=3.0 volts; Dual Charger detects connection of H/H M: 1.0<=V<2.0 volts; Unconnected L: 0.0<=V<1.0 volts; Dual Charger detects connection of H/H	
23	EXT_PWR	<==	2	The Dual Charger shall control switching of the power supply to the front slot (corresponds to EXT_PWR) based on the state of the CHARGE_ON signal. H: EXT_PWR supplied L: When the H/H can determine whether or not to set CHARGE_ON. After the insertion of the H/H, EXT_PWR shall be subsequently supplied within <b>TBA</b> hours	Refer to pin 8

**Battery Connector**

No.	Name	H/H <=> EXT	Total	Function	H/H Circuit
1	VBAT	<==	1	Positive battery terminal. Li+ (2 cells in parallel): 3.6 V nom. NiMH (3 cells in series): 3.6 V nom.	
2	BAT_TEMP	<==	1	BAT_TEMP has 2 purposes. 1) Determine whether a battery is attached to the H/H. 2) Monitor battery temperature for the purposes of charging. H: Abnormal battery M: Li+ or NiMH charging L: No battery or abnormal battery	
3	GND	<==	1	Negative battery terminal	
4	BAT_ID	<==	1	BAT_ID is used to identify the type of attached battery. H: Li+ or no battery L: NiMH	See charging ASIC specification

**SIM Interface**

Pin	Signal
1	GND
2	5 V
3	Not connected
4	Reset
5	Serial input/output
6	Clock
7	Not connected
8	Not connected

## 3 RF OVERVIEW

### 3.1 Introduction

#### 3.1.1 General Specifications

GD70 is a Dual Band Product incorporating two switchable transceivers one for GSM900 and another GSM1800 band. The transmit and receive bands for the mobile are given in the table below:

	Tx	Rx
GSM900	890-915	935-960
GSM1800	1710-1785	1805-1880

Other salient technical features are as follows:

	GSM900	GSM1800	Units
Rx Bandwidth	25	75	MHz
Tx Bandwidth	25	75	MHz
Duplex Spacing	45	95	MHz
Number of Channels	124	374	
ARFCN (Channel Numbers)	1-124	512-885	
1st Tx Channel	890.2	1710.2	MHz
Last Tx Channel	914.8	1784.8	MHz
1st Rx Channel	935.2	1805.2	MHz
Last Rx Channel	959.8	1879.8	MHz
Maximum Tx Power	33.0 (Class 4) (PL5)	30.0 (Class 1) (PL0)	dBm
Minimum Tx Power	5.0 (PL19)	0.0 (PL15)	dBm

#### 3.1.2 Description of RF PCB

All the RF circuitry is contained on one PCB. The RF PCB has six layers made from FR4 material (Epoxide woven glass fabric copper-clad laminate as specified in BS4584 Part 102 and prepeg as specified in BS4584 Part 103). Top and bottom layer tracks are gold-plated to prevent oxidation and enable better soldering. The board thickness is 0.9 mm ( $\pm 0.1$  mm).

The majority of the components are on one side of the PCB leaving as much as possible of the opposite side to be a complete ground plane; this is used to provide RF shielding. The RF board is connected to the baseband digital board via a 50-way dual in-line connector. A metallised plastic chassis is used to separate the RF and the Logic PCB's. When the chassis is sandwiched between the RF and the Logic PCB's the ground plane of the RF board together with the chassis forms an effective shielded enclosure which prevents spurious emissions. The chassis has also been designed to provide smaller walled sections which are used to isolate sensitive RF areas such as the VCTCXO and the VCO from high level interferers such as the PA output.

3.2 Functional Description

The major building blocks for the RF design are the Siemens transmit (Tx) and receive (Rx) ICs, Fujitsu RF-IF dual PLL and the antenna subsystem.

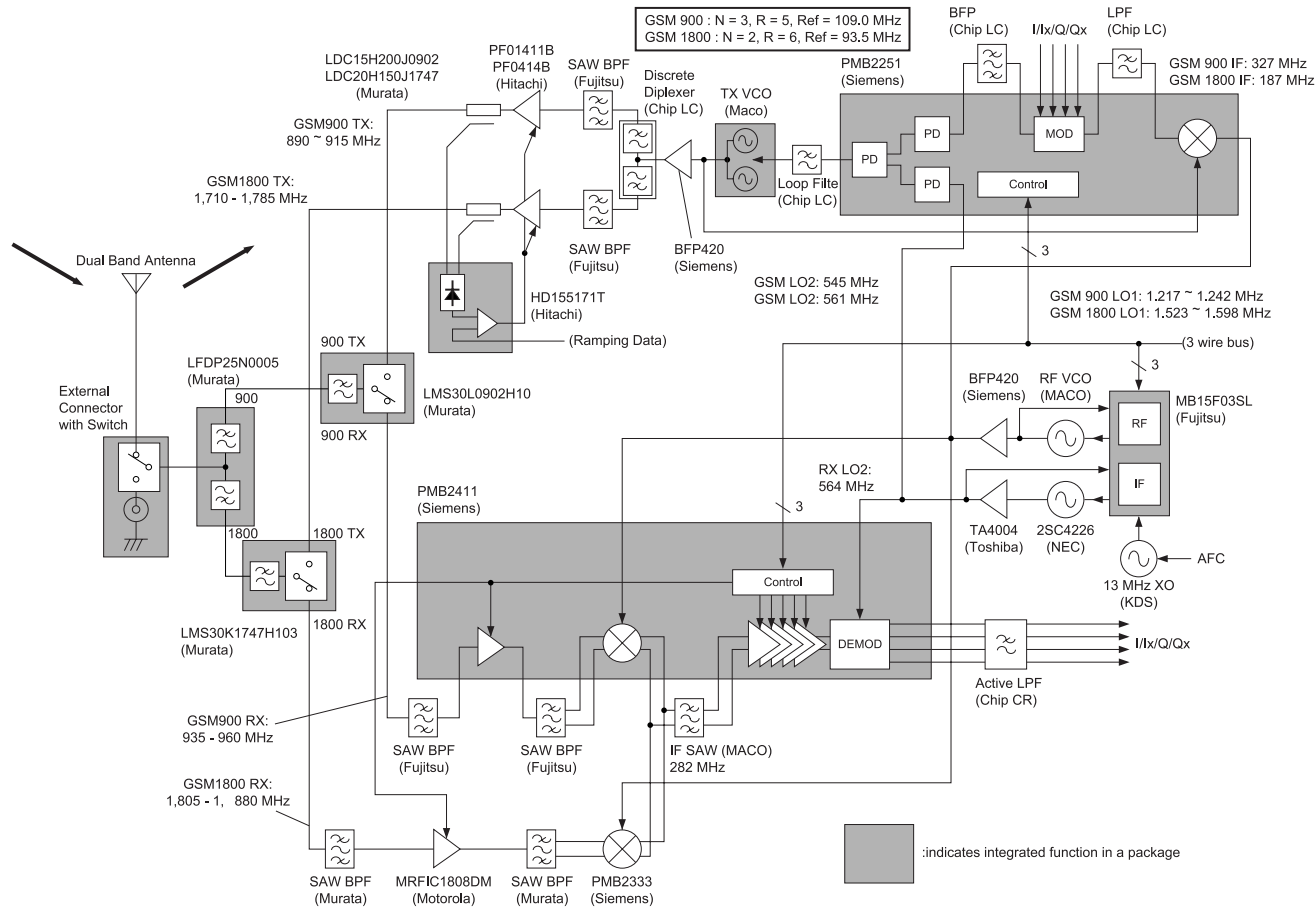


Figure:1 RF Block Diagram

D70-0301

3.2.1 Frequency Plan

The GD70 frequency plan is shown below.

	Tx	Rx	Tx IF	Rx IF	RFLO Tx	RFLO Rx
GSM900	890-915	935-960	327	282	1217-1242	1217-1242
GSM1800	1710-1785	1805-1880	187	282	1523-1598	1523-1598

	Fcomp(MHz)	R	N	Tx IF LO(MHz)	Rx IF LO(MHz)
GSM900	109	5	3	545	564
GSM1800	93.5	6	2	561	564

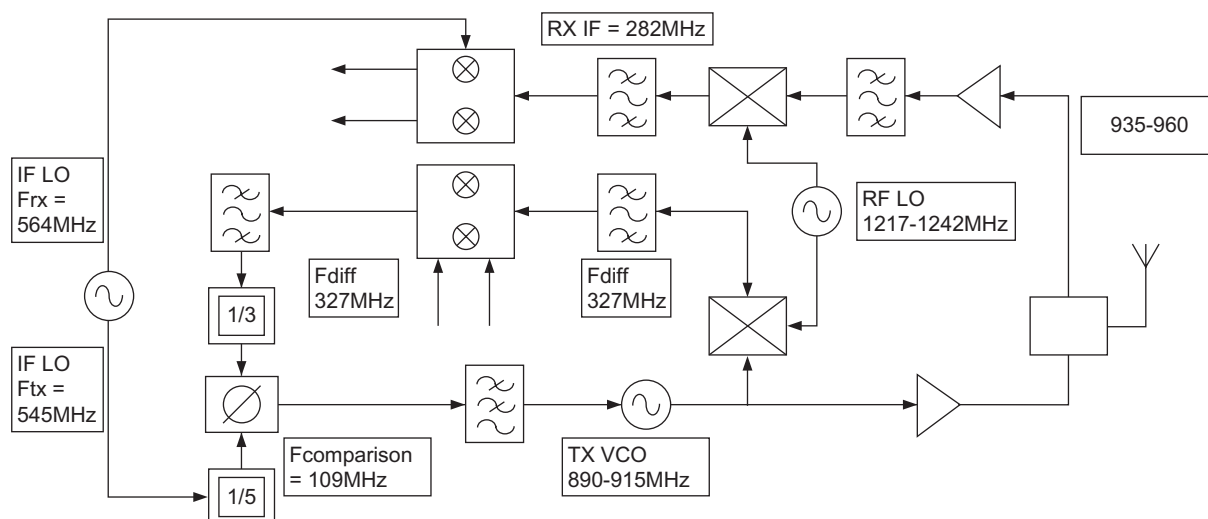


Figure:2 GSM 900 frequency plan

D70-0302

### 3.2.2 Functional Description of the PLLs

#### 1st Local Oscillator

The 1st local RF Oscillator runs from 1217 MHz to 1598 MHz depending on the mode of operation.

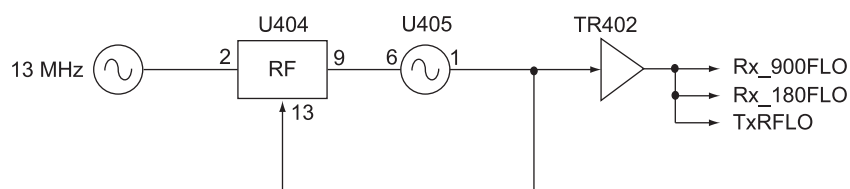


Figure:3 1st Local Oscillator

D70-0303

U404 is a dual PLL IC. The reference signal is generated by the 13 MHz clock and received on pin 2. The output from pin 9 on the U404 drives the VCO. U405 is the RF VCO, whereby the input from pin 6 controls the frequency of oscillation. The output of the VCO is from pin 1. This output is split, with one feed going back into the loop and the other to the amp TR402.

From the output of TR402 there are three feeds:

- GSM 900 receiver;
- GSM 1800 receiver;
- Transmitter.

In GSM 900 mode (a) the oscillator operates from 1217 MHz to 1242 MHz. In GSM 1800 mode (b) the oscillator operates from 1523 MHz to 1598 MHz. The output from the transmitter (c) will be the same as the receiver mode (a) or (b).

## 2nd Local Oscillator

The 2nd local RF Oscillator operates at three frequencies 545, 561 and 564 MHz.

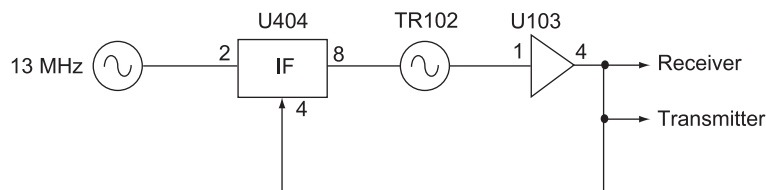


Figure:4 2nd Local Oscillator

D70-0304

U404 is a dual PLL IC. The reference signal is generated by the 13 MHz clock and received on pin 2. The output from pin 8 on the U404 drives the VCO. TR102 and associated components form the VCO, whereby the output feeds the amplifier U103. This output from the U103 is split into three, with an Rx & Tx feed being returned to the PLL IC.

The 2nd local oscillator operates at the following frequencies:

- GSM 900 transmitter = 545 MHz;
- GSM 1800 transmitter = 561 MHz;
- Receiver = 564 MHz.

### 3.2.3 Antenna

The antenna is a fixed helical type.

A mechanical RF switch is used to route the RF signal from the external antenna for handsfree operation and test purposes.

### 3.2.4 Transmit and Receive

The transmit and receive paths of GD70 are covered in their own specific chapters later in this manual.

## 3.3 RF & Accessory Connector

In previous models the RF signal is routed to the accessory connector which contains a micro-switch. If the switch is open the RF signal is routed to the handsfree unit, if closed the signal is routed back up the RF PCB to the antenna. This routing of the RF signal up and down the RF PCB invariably has a finite power loss associated with it.

In addition the GD70 has a limited PCB area and the routing of the RF signal in this way reduces further the available PCB area required for the Dual Band circuit.

To alleviate these problems the RF connector is located close to the PA module. This reduces the loss and hence the PAs do not have to be driven so hard. This allows the power supply voltage to be lower, thus improving battery performance.

## 4 TRANSMITTER

### 4.1 Introduction

This section provides a technical description of the transmitter circuit of the RF circuit. A circuit diagram of the whole system is provided in the Service Manual (MCUK981201C8).

The uplink frequencies for the GSM 900 and GSM 1800 can be calculated as follows:

#### 4.1.1 Uplink Frequencies GSM 900

$$\begin{aligned}
 \text{Uplink frequency} &= 890 \text{ MHz} + (\text{ARFCN} \times 0.2 \text{ MHz}) \\
 &\text{e.g. for CH55} \\
 &890 \text{ MHz} + (55 \times 0.2 \text{ MHz}) \\
 &= 890 \text{ MHz} + (11 \text{ MHz}) \\
 &= 901 \text{ MHz}
 \end{aligned}$$

#### 4.1.2 Uplink Frequencies GSM 1800

$$\begin{aligned}
 \text{Uplink frequency} &= 1710 \text{ MHz} + ((\text{ARFCN} - 511) \times 0.2 \text{ MHz}) \\
 &\text{e.g. for CH512} \\
 &1710 \text{ MHz} + ((512 - 511) \times 0.2 \text{ MHz}) \\
 &= 1710 \text{ MHz} + (0.2 \text{ MHz}) \\
 &= 1710.2 \text{ MHz}
 \end{aligned}$$

### 4.2 Functional Description

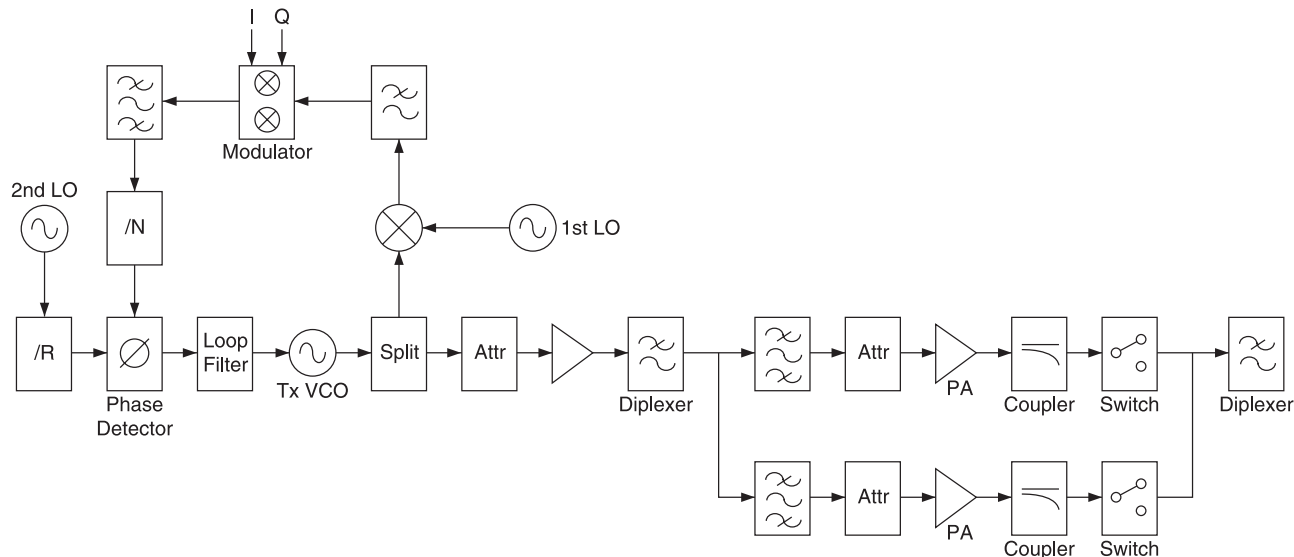


Figure:1 Transmitter

D70-0401

The transmitter design is based on an IQ Modulator. The architecture has been carefully chosen to enable the GSM transmitter noise in receiver band requirements to be met without the need for a duplexer. This was a very important consideration in the design of the transmitter as the area required by two duplexers would be too large for the radio design to fit in the desired small area.

The Modulation loop uses a modular VCO which contains two VCOs, one for the 900 MHz band and the other for the 1800 MHz band. The required VCO is selected by a control line, PCNnGSM. The output from the Tx VCO is split into two, one feeding the mixer within the modulation loop and the other feeding the PA through a PA buffer and bypass filtering. There are resistive pads before the PAs and the PA buffer to help with impedance matching and level adjustment.

## TRANSMITTER

A discrete diplexer is used after the PA buffer which provides low pass filtering for the 900 MHz band and high pass filtering for the 1800 MHz band. The switching between the receiver and the transmitter for any band is achieved by means of pin diode switches. The antenna ports of these switches are connected to the antenna or the handsfree RF connector. The handsfree connector incorporates a mechanical switch which enables the signal to be routed either to the antenna or to the handsfree connector depending on the operation required.

The RF LO is also a modular VCO which contains two VCOs, one for the 900 and the other for the 1800 MHz bands. The operation is similar to the Tx VCO in that the required RF VCO is switched by two control lines.

The IF VCO is a discrete design. Both the RF and IF LOs are designed around a dual PLL with the IF frequency range up to 600 MHz and the RF frequency range up to 2 GHz.

The 13 MHz oscillator design, similar to all of the previous designs, employs a modular TCVCXO with a buffer. The operation is similar to that of the G600 where the buffer is switched off during idle mode to increase the standby time.

### 4.2.1 GSM1800 Frequency Plan

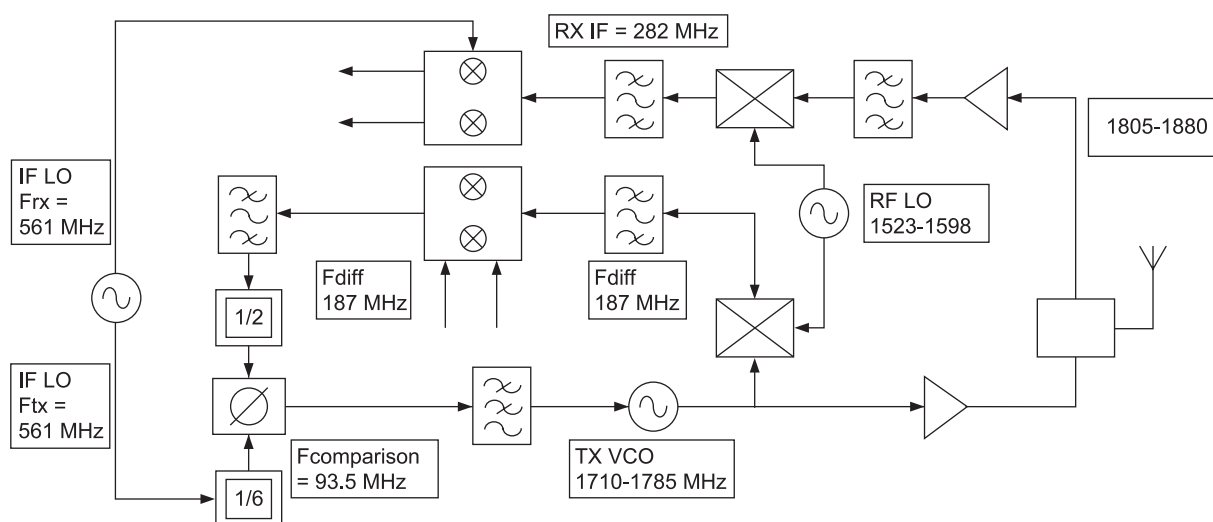


Figure:2 Frequency Plan

D70-0402

Two advantages of the new frequency plan are the narrower tuning range requirement for the IF VCO and a high IF frequency for the GSM1800 to enable better filtering of the 3rd harmonic of the Tx IF signal.

In either band, GSM900 or GSM1800, the Rx IF is fitted at 282 MHz. Therefore, the 2nd LO is at 564 MHz for receiver modes. For this choice of IF, no receiver blocking is believed to occur due to harmonics of 13 MHz, 3.25 MHz, harmonics of 282 MHz falling into the Rx bands or due to harmonics of the 2nd LO mixing with harmonics of the 1st LO and causing blocking signals to occur in any Rx channel.

In GSM900 transmit mode, the 2nd LO is reprogrammed to 545 MHz via the auxiliary synthesizer. Since this is close to 564 MHz, it should not be necessary to switch an inductor to do this - the resonator should have sufficient range to cover both of these frequencies.

In GSM1800 transmit mode, the 2nd LO is reprogrammed to 561 MHz. This is even closer to the Rx frequency of 564 MHz and should not present a problem.

The 1st LO provides low-side injection for the GSM1800, since the PMB2251 mixer ports are only specified up to 2 GHz, also the RF input port of the MB15F03SL only increases up to 1.8 GHz.

The Tx VCO will be the on-channel in either the GSM900 or GSM1800 modes of operation.

The RF LO should not normally require re-tuning between transmit and receive modes, but only when monitoring adjacent cells.

## 5 RECEIVER

### 5.1 Introduction

This section provides a technical description of the receiver section of the RF circuit. A circuit diagram of the whole system is provided in the Service Manual (Order No. MCUK981201C8).

The downlink frequencies for the GSM 900 and GSM 1800 can be calculated as follows:

#### 5.1.1 Downlink Frequencies GSM 900

$$\begin{aligned}
 \text{Downlink frequency} &= 935 \text{ MHz} + (\text{ARFCN} \times 0.2 \text{ MHz}) \\
 &\text{e.g. for CH55} \\
 &935 \text{ MHz} + (55 \times 0.2 \text{ MHz}) \\
 &= 935 \text{ MHz} + (11 \text{ MHz}) \\
 &= 946 \text{ MHz}
 \end{aligned}$$

#### 5.1.2 Downlink Frequencies GSM 1800

$$\begin{aligned}
 \text{Downlink frequency} &= 1805 \text{ MHz} + ((\text{ARFCN} - 511) \times 0.2 \text{ MHz}) \\
 &\text{e.g. for CH512} \\
 &1805 \text{ MHz} + ((512 - 511) \times 0.2 \text{ MHz}) \\
 &= 1805 \text{ MHz} + (0.2 \text{ MHz}) \\
 &= 1805.2 \text{ MHz}
 \end{aligned}$$

### 5.2 Functional Description

The main building block for the Dual Band Receiver is the Siemens IC PMB411 V1.1. The receiver is a double superhet type with the first IF at 282 MHz (IF path common to both frequency bands).

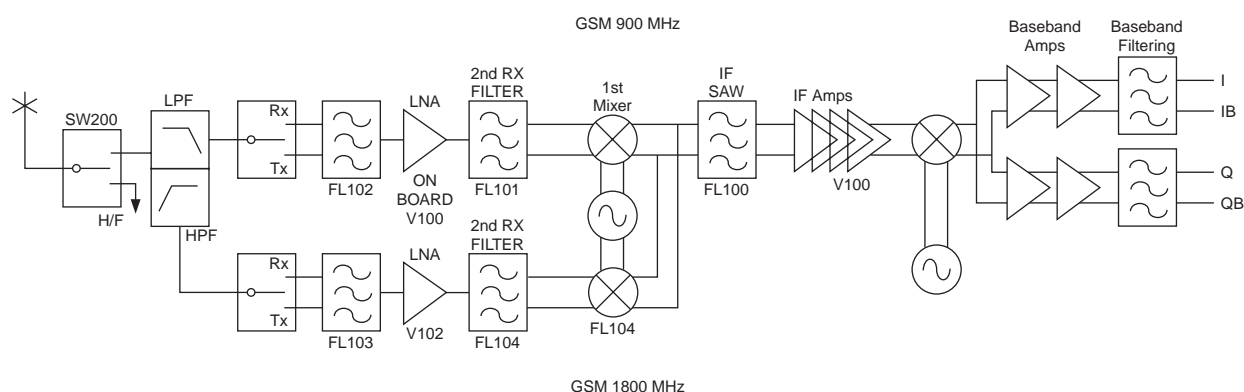


Figure:1 Receiver IC PMB411 V1.1

D70-0501

The Rx IC contains the following stages:

1. GSM900 LNA.
2. GSM900 RF mixer.
3. Gain controlled 5-stage IF amplifier.
4. I,Q quadrature down converter.
5. Baseband Op Amps for further amplification and some filtering of the baseband I,Q signals.

### 5.2.1 GSM900

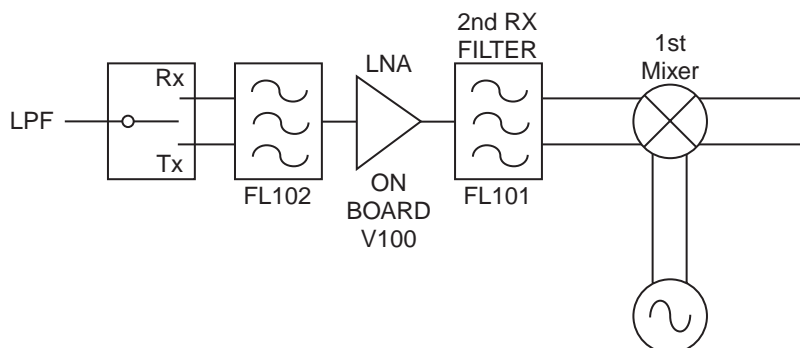


Figure:2 GSM900 Receiver

D70-0502

RF input to the receiver is either via the antenna or via the H/F RF connector for test purposes. The input signal from the antenna or the H/F RF connector is fed into the GSM900 onboard LNA through the GSM900 LPF Diplexer port, through the GSM900 Tx/Rx switch and finally through the unbalanced GSM900 Rx SAW filter. The diplexer band splits the two GSM frequency bands whilst the pin switches route the signal flow from the receiver and the transmitter as required. The receiver 1st SAW filter provides the roofing filter for the Rx front end.

The LNA gain can be controlled via a three-wire bus between a typical value of 19 dB and approximately -3 dB. The LNA gain reduction is required for operation under strong signal conditions where input power levels are greater than about -40 dBm. Typical NF for the LNA is 2.4 dB and the third order intercept point at its input is -4 dBm.

The output from the LNA goes through a differential BP SAW filter and is differentially fed into the 1st down-converter mixer. The mixer has a third order intercept point of -2 dBm with a maximum SSB noise of 9dB. The LO for the mixer is generated by a PLL (Fujitsu MB15F03SL) employing a modular VCO. The output from the VCO is buffered by an RF MMIC amplifier. The LO frequency range for the GSM900 is 1217 to 1242 MHz.

The IF output at 282 MHz from the mixer is filtered by the differential IF SAW filter before it is fed into the gain-controlled IF amplifiers. The use of differential filters eliminates the need for baluns and provides some cost and space advantage.

The IF amplifier is a five stage cascaded section. The gain is controllable by a three-wire bus from -10 to +70 dB in 2 dB steps. This function is used for AGC purposes.

The output from IF amplifiers is fed into two quadrature mixers where it is converted down to baseband. The IF LO is generated at 564 MHz by an external discrete VCO. An on-chip divider on the Rx IC divides this by two and also produces two outputs in quadrature to generate the baseband I and Q signals. The outputs from the mixers are connected to external pins through a pair of buffers. Two on-chip Op Amps are used to amplify the AC signal from the mixers to meet the overall signal budget requirements.

The DC level at the output of the Op Amps is 0.95 V with a 1.25 Vpp single ended AC swing sufficient to drive the baseband IC VEGA (see Section 8).

The coupling between RF output and the baseband input has been designed as a DC coupling in order to minimise the turn-on time of the Rx IC for the purpose of current optimization.

5.2.2 GSM900 Signal Levels

The signal levels through the receiver IC for the GSM900 are given below.

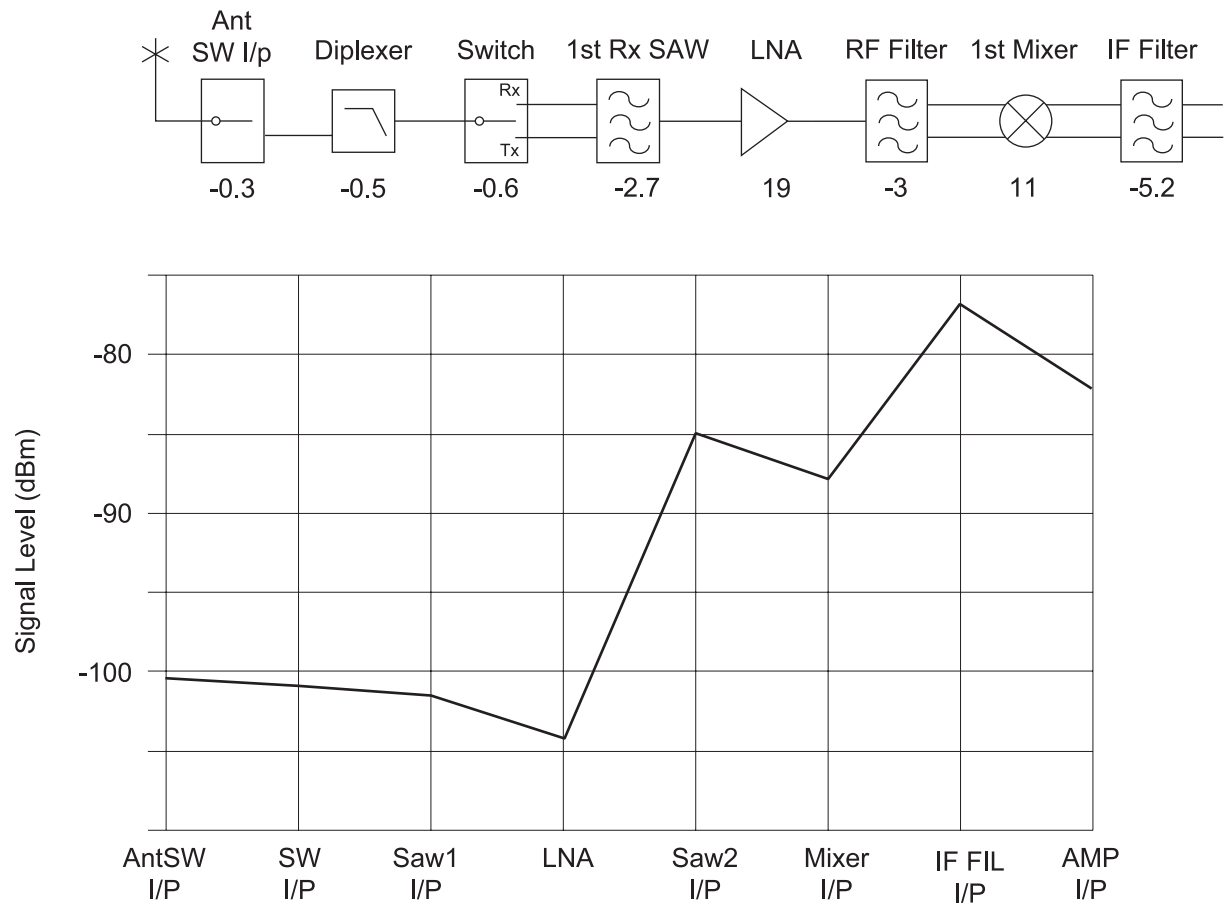


Figure:3 GSM900 Nominal and Worst Case Signal Levels

D70-0503

### 5.2.3 GSM1800

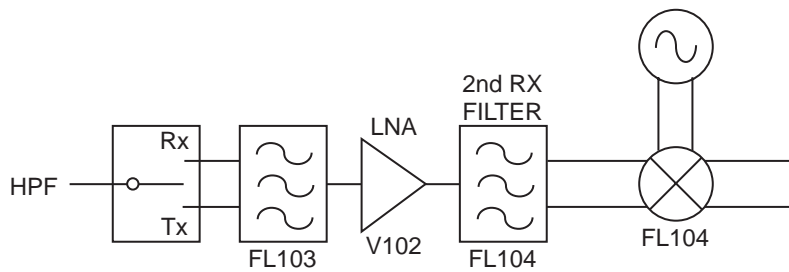


Figure:4 GSM1800 Receiver

D70-0504

RF input to the receiver is either via the antenna or via the H/F RF connector for test purposes. The input signal from the antenna or the H/F RF connector is fed into the GSM1800 external LNA through the GSM1800 LPF Diplexer port, through the GSM1800 Tx/Rx switch and finally through the unbalanced GSM1800 Dielectric filter. The diplexer band splits the two GSM frequency bands whilst the pin switches route the signal flow from the receiver and the transmitter as required. The receiver Dielectric filter provides the roofing filter for the Rx front end.

The LNA gain can be controlled via a three-wire bus on the PMB2411 between a typical value of 18 dB and approximately -19 dB. The LNA gain reduction is required for operation under strong signal conditions where input power levels are greater than about -40 dBm. Typical NF for the LNA is 2.0 dB and the third order intercept point at its input is -5 dBm.

The output from the LNA goes through an unbalanced BP SAW filter and is differentially fed into the 1st down-converter mixer, via a single-ended to differential matching network. The mixer has a third order intercept point of -1 dBm with a maximum SSB noise of 11dB. The LO for the mixer is generated by a PLL (Fujitsu MB15F03SL) employing a modular VCO. The output from the VCO is buffered by an RF MMIC amplifier. The LO frequency range for the GSM1800 is 1523 to 1598 MHz.

The IF output at 282 MHz from the mixer is then fed into the common IF path as previously described for the GSM900.

5.2.4 GSM1800 Signal Levels

The signal levels through the receiver IC for the GSM1800 are given below.

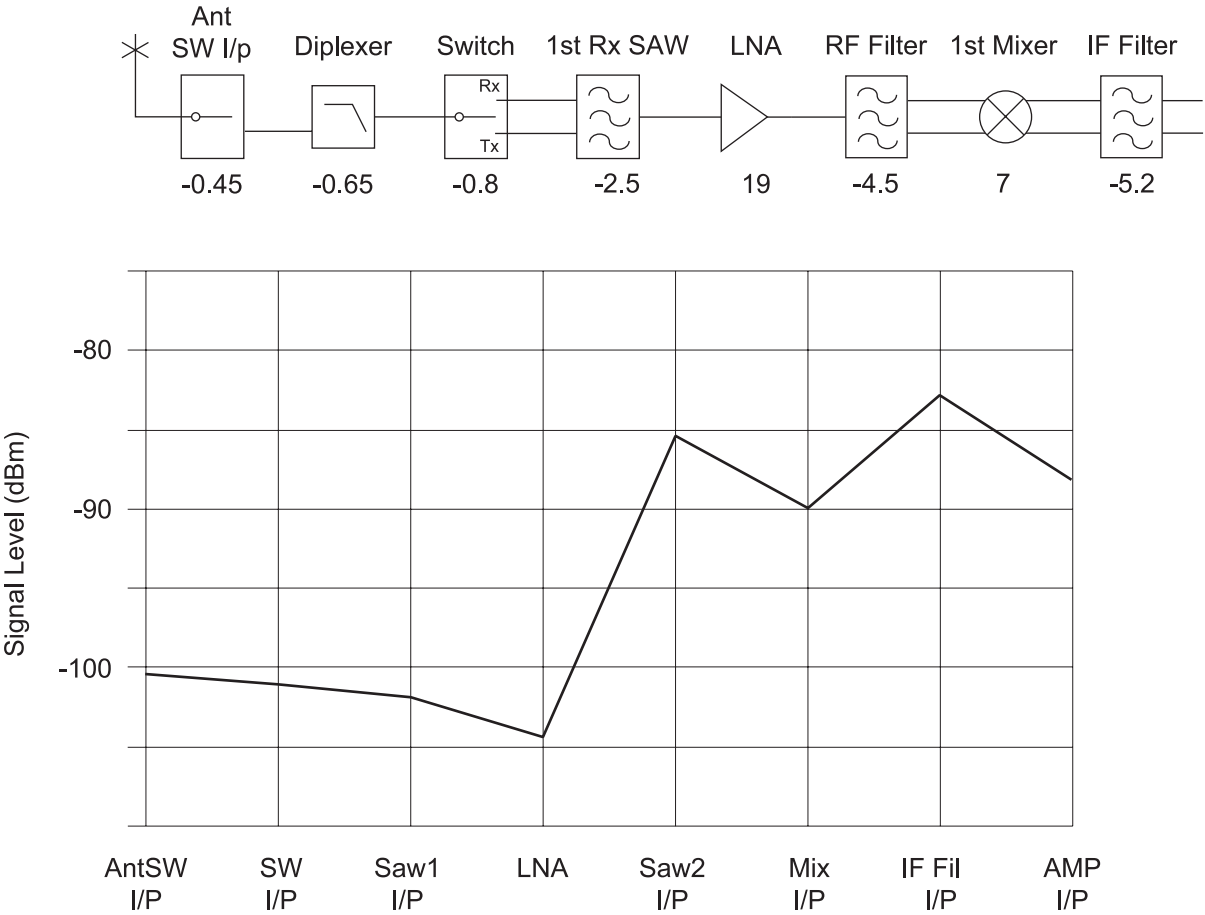


Figure:5 GSM1800 Nominal and Worst Case Signal Levels

D70-0505

This page is left intentionally blank.

## 6 BASEBAND OVERVIEW

### 6.1 Introduction

All Baseband circuitry is contained on one PCB. The Baseband PCB has six layers made from FR4 material. Top and bottom layers are gold-plated to prevent oxidation and enable better soldering. The board thickness is 1.0 mm (+0.0, -0.1 mm).

The Baseband board is connected to the RF board via a 50 dual in line connector.

A metallised plastic chassis is used to separate the Baseband and the RF PCBs. The continuous chassis design is important for EMC purposes. When the chassis is sandwiched between the Baseband and the RF PCBs the ground plane of the RF board together with the chassis forms an effective shielded enclosure, which prevents spurious emissions.

### 6.2 Functional Description of the PCB

The GD70 baseband is based around a 2 chip GSM chipset developed by Texas Instruments. One chip (GEMINI) carries out signal processing with DSP and CPU, and the other chip (VEGA) contains the analogue interface chip. The highly integrated nature of these components means each contain a large number of functions.

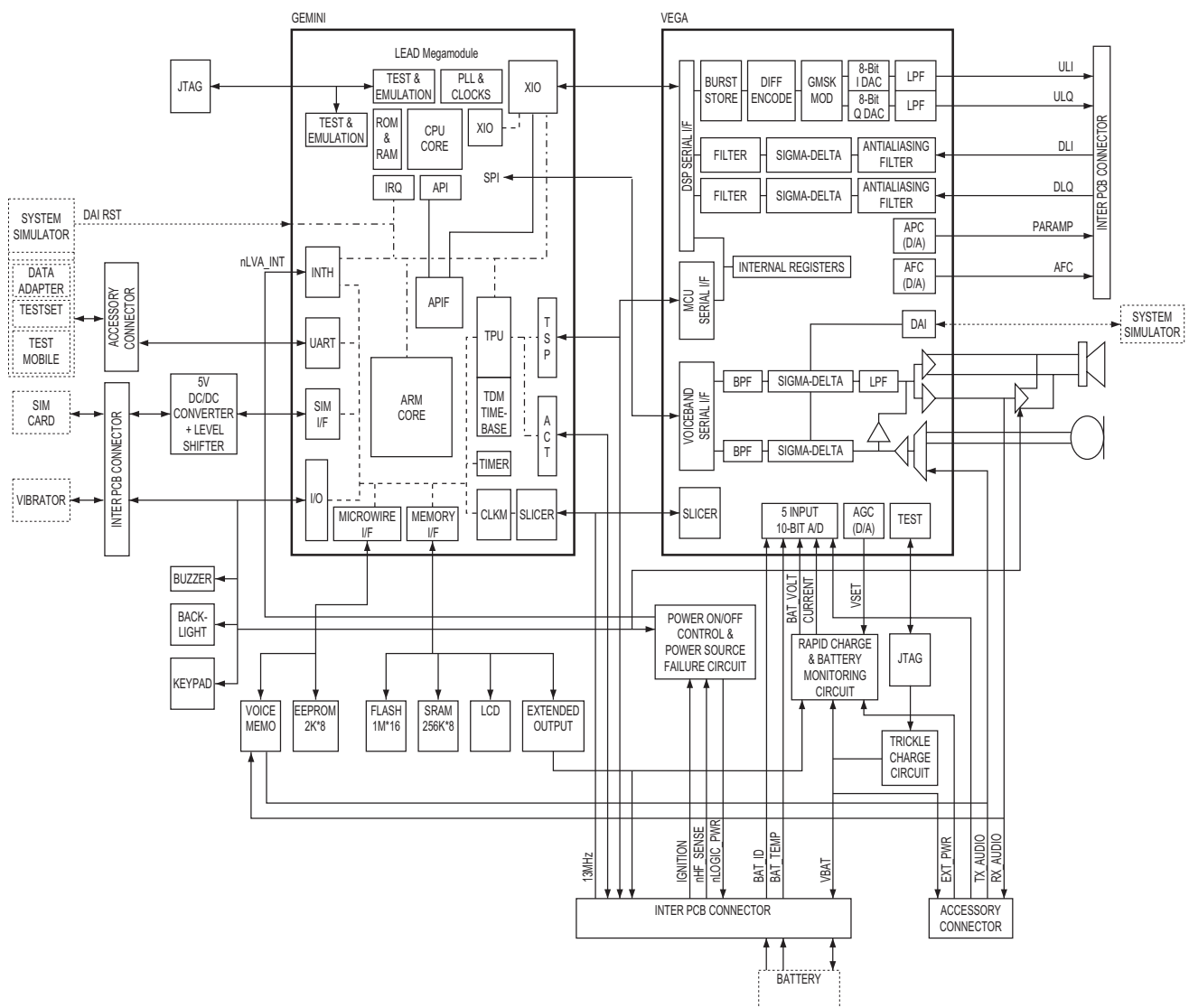


Figure:1 Baseband Block Diagram

D70-0601

### 6.2.1 Keypad

The Keypad has a 5 x 5 matrix allowing 25 keys to be scanned on a key being pressed, a keypad interrupt is generated. To find which key is pressed the software must assert each column in turn and read which row is active.

To eliminate key bounce, the key press must then be confirmed twice at about 20 ms intervals.

The Keyboard scanning is software controlled. Key pressed is indicated by an interrupt, but key release is controlled by software.

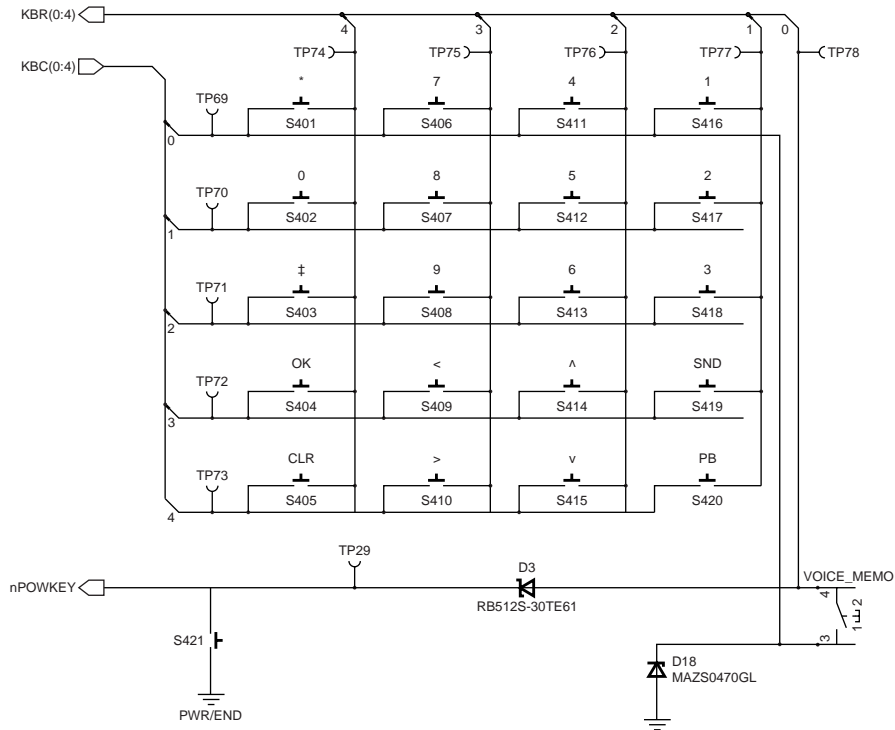


Figure:2 Keypad Matrix

D70-0602

### 6.2.2 Subscriber Identity Module (SIM)

The SIM interface is designed to support 5 V SIMs.

The GD70 GEMINI process is unable to support 5 V tolerant inputs. Therefore, in order to Interface GEMINI with a 2.8 V supply, and the SIM with a 5 V supply, it is necessary to include a level shift. U3 is able to perform the required level shift. In addition the device includes a switched capacitor charge pump DC/DC converter to generate the 5 V SIM supply from VBAT.

### 6.2.3 Time Processing Unit (TPU)

The TPU provides the GSM TDMA timing requirements for the system, external timing signals are provided by an area of Microcode within the GEMINI chip.

GEMINI Pin	Description
65	VEGA BENA
71	VEGA OCE
67	VEGA BULON
68	VEGA BDLON
69	PA_ON
70	PCNnGSM
118	RF signal RXON1
119	RF signal RXON2
58	VEGA_SEL
59	PLL_STRB
64	RF signal TXON1
61	TX_PLL_EN
62	IFAGCEN

### 6.2.4 CPU Memory

The memory requirements for GD70 are:

1. 16 Mbit 3 V FLASH organised as 1M \* 16;
2. 2 Mbit 3 V RAM organised as 256k \* 8;
3. 16 kbit 3 V Serial EEPROM as 2k \* 8.

### 6.2.5 LCD

The LCD assembly is a subassembly comprising of LCD glass and driver chip on a flexible PCB with connection to the Logic PCB via zebra strip connections.

A 96 x 58 pixel graphical display is used to give maximum information. It can also display Chinese characters and large numbers. For example, 12 x 2 line or 16 x 3 line, both with 2 lines of icons.

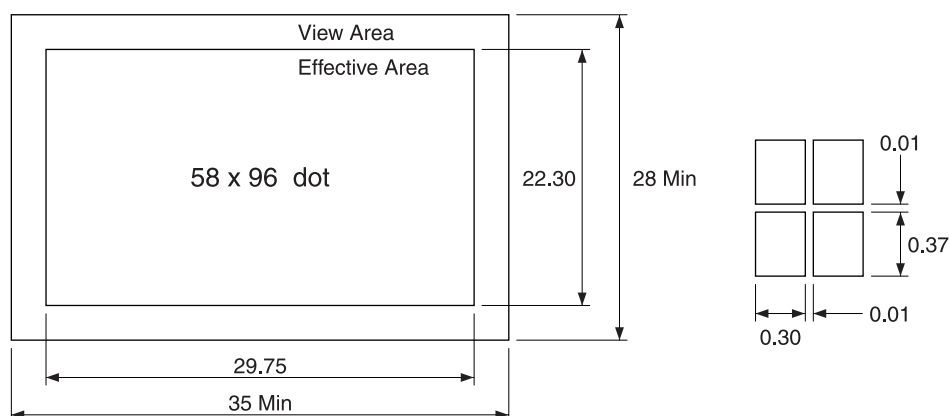


Figure:3 LCD Dimensions

D70-0603

## 6.2.6 Microphone

The microphone is an omni-directional type as used with previous models. GSM requires that when in Handheld use the sending audio frequency response must fit within the mask shown below.

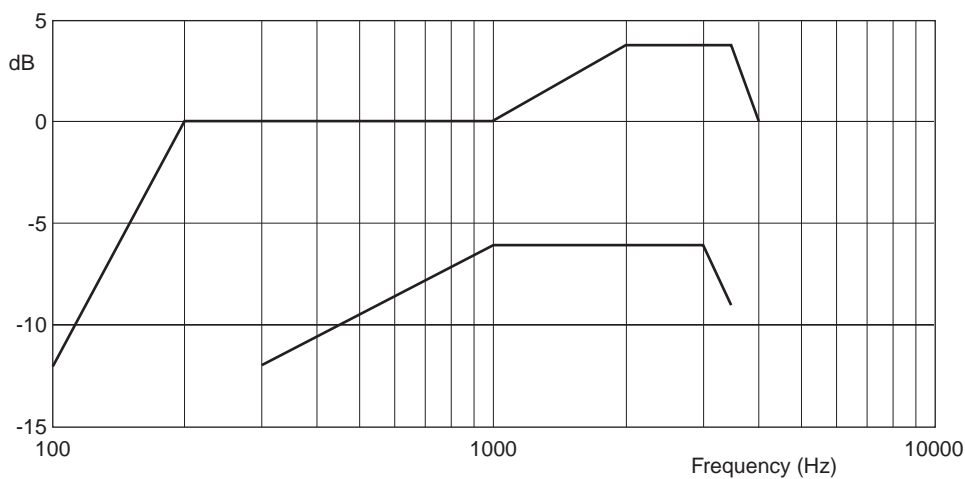


Figure:4 Handheld GSM Transmit Audio frequency response mask

D70-0604

When using the Handsfree feature GSM requires that the sending audio frequency response must fit within the mask shown below.

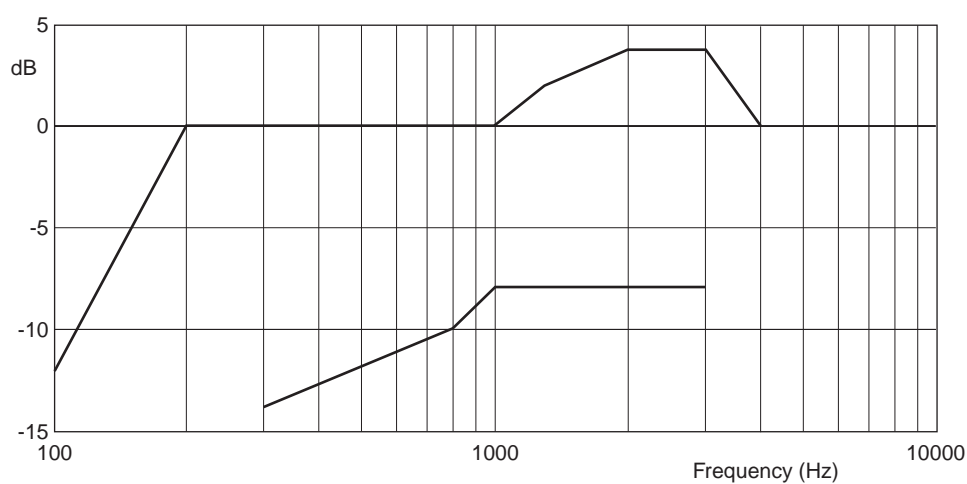


Figure:5 Handsfree GSM Transmit Audio frequency response mask

D70-0605

6.2.7 Speaker

To meet Handsfree volume requirements with a single Li+ battery, a low impedance (dynamic) type must be used. GSM requires that the receive audio frequency response in Handheld use must fit within the mask shown below. GD70 is designed to meet Handheld requirements with a type 1 artificial ear.

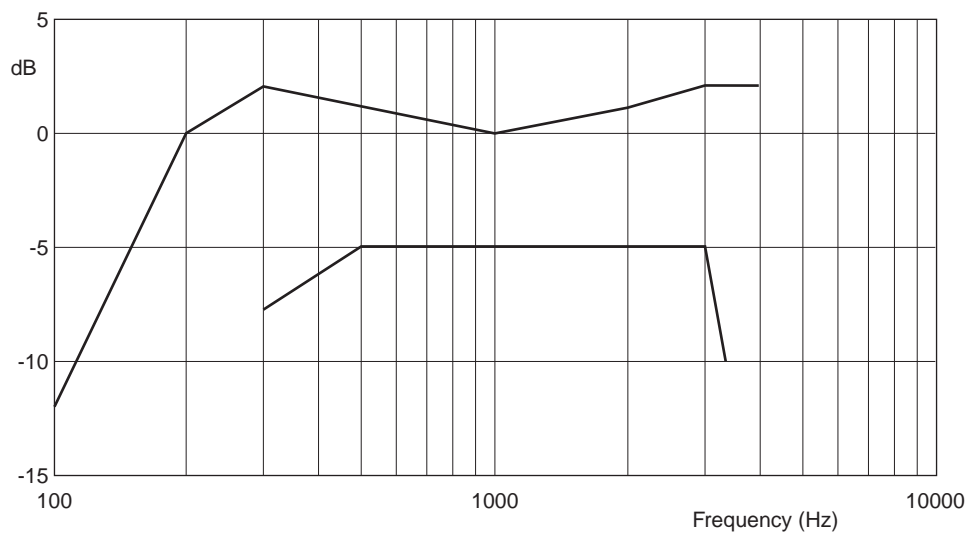


Figure:6 Handheld GSM Receive Audio frequency response

D70-0606

Volume levels			
Volume level	PGA	Volume	Total Gain
1	3dB	0dB	3dB
2	0dB	0dB	0dB
3	-3dB	0dB	-3dB
4	-3dB	-6dB	-9dB

When using the internal Handsfree feature, the receive audio frequency response must fit within the mask shown below.

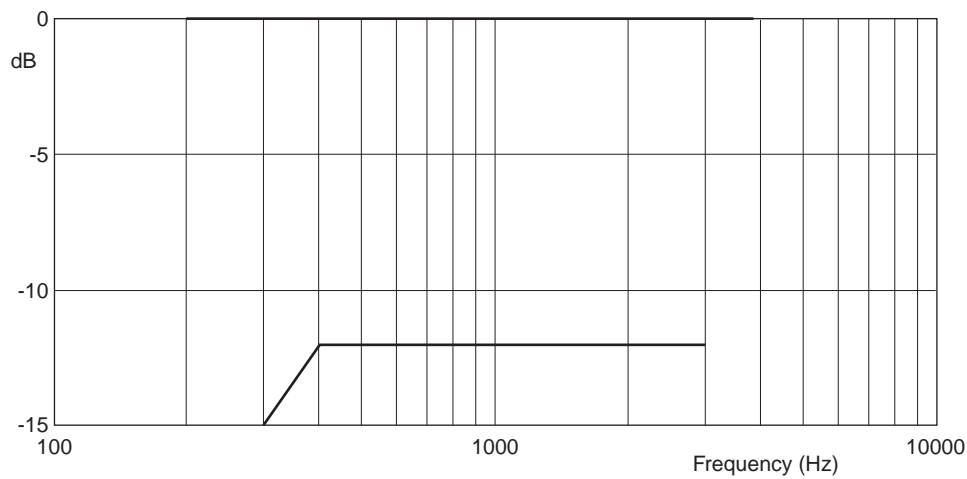


Figure:7 Handsfree GSM Transmit Audio frequency response mask

D70-0607

6.2.8 Internal Handsfree

In Handheld mode the speaker is driven by the ear-piece amplifier inside VEGA. For internal Handsfree operation, the ear-piece amplifier is disabled and the speaker is driven using an external power amplifier via the auxiliary speaker output in VEGA. The power amplifier can be enabled and disabled by the INTERNAL\_HF signal.

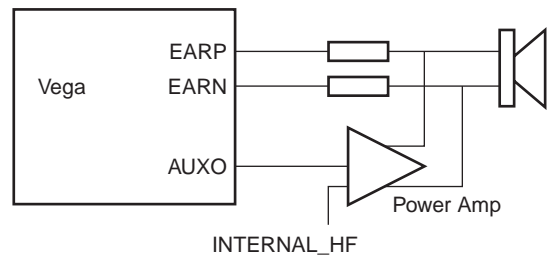


Figure:8 Speaker connection for Handheld and Handsfree use D70-0608

6.2.9 Buzzer

The volume level of the buzzer is defined by the 6 bit PWM register setting in GEMINI I/O. The buzzer tone is then superimposed on this level using software.

Timer 1 in GEMINI is used to time the period between switching the buzzer on and off to make the tone. For more complex buzzer ringing tones, the buzzer volume level can also be altered after each time-out of timer 1.

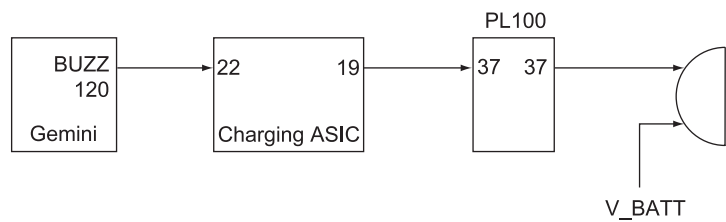


Figure:9 Buzzer Control Circuit D70-0609

6.2.10 Timers

Two 16 bit general purpose timers which can be used either as auto-reload or 1 shot timers to provide interrupts to the ARM CPU. The timer clock duration is defined by a prescaler and 16 bit register. The Timer unit receives a 928 kHz clock from the GEMINI clock module. A combination of prescaler and timer register gives a time range of 1.078  $\mu$ sec to 9.039 sec.

Timer	Function	Setting
1	Buzzer Timer	Tone frequency
2	Watch Dog Timer	3 sec

## 6.2.11 USART

The serial port is compatible with an Intel 8251 and has six pins.

USART Pin Assignments			
Signal Name	Pin No.	Function	I/O
TXD	113	USART serial data Tx	O
RXD	111	USART serial data Rx	I
DTR	114	Used as I/O pin	O
DSR	110	Used as I/O pin	I
TXE	115	Used as I/O pin	O
RXE	116	Used as I/O pin	O

This page is left intentionally blank.

## 7 GEMINI

### 7.1 Introduction

Gemini contains the DSP, CPU and GSM timing functions and many peripheral functions. The software for the DSP is contained in masked ROM.

### 7.2 Functional Description

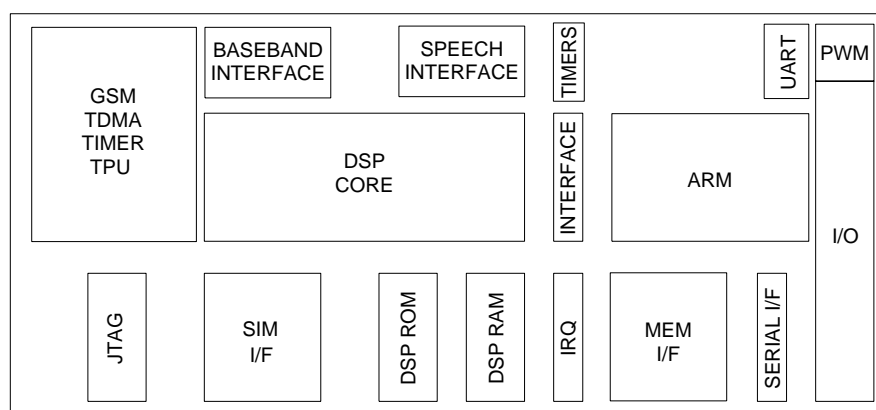


Figure:1 GEMINI Block Diagram

600-0701

#### 7.2.1 Digital Signal Processor

The Digital Signal Processor (DSP) core is compatible with the Texas Instruments TMS350C5xx family of DSPs. Included in the DSP core is an interface to the CPU by a shared memory interface.

The DSP memory is also located within GEMINI. The ROM code size is determined by the size of the software.

#### 7.2.2 CPU

The CPU is a 32 bit RISC CPU with 16 bit instruction set. The CPU is designed to access 32 bit memory and peripherals; a further module within the GEMINI chip allows access to 8 or 16 bit memory.

Memory Access Times		
Clock Speed	Memory Access Time	Additional Access time per wait state
19.5 MHz	41 ns	51 ns
13 MHz	67 ns	77 ns
9.75 MHz	91 ns	102 ns
6.5 MHz	144 ns	154 ns
4.875 MHz	194 ns	204 ns
3.75 MHz	298 ns	308 ns

For 120 ns access FLASH and RAM a 13 MHz clock gives 1 wait state access to both devices.

### 7.2.3 Memory Interface

The memory interface allows the 32 bit CPU to access 16 and 8 bit devices, and allows the addition of wait states to memory access. The memory interface allows between 0 and 7 wait states to be added. The ROM area is hardware write protected, a FLASH write enable bit in the ROM wait state configuration register can be used to enable write access the ROM area.

CPU Memory MAP				
Device Name	Start address	Size	Use	Bus width
ROM	0000:0000	2M	FLASH 1 Mbytes	16 bits
RAM	0020:0000	2M	RAM 256 kbytes	8 bits
BUS CNTRL	0040:0000	1M	wait state registers	16 bits
API RAM	0050:0000	8k	CPU/DSP shared ram	16 bits
TPU RAM	0050:4400	1k	GSM timer Microcode RAM	16 bits
APIC	0050:4000	1k	CPU/DSP interface controller	16 bits
SIM	0050:4800	1k	SIM interface	16 bits
TSP	0050:4C00	1k	Timed Serial port	16 bits
INTH	0050:5000	1k	Interrupt controller	16 bits
TPU REG	0050:5400	1k	GSM timer registers	16 bits
CLKM	0050:5800	1k	Clock control module	16 bits
TIMER	0050:5C00	1k	software timers	16 bit
APIF	0050:6000	1k	ARM peripheral interface	16 bit
UWIRE	0050:6400	1k	Synchronous Serial port	16 bit
ARMIO	0050:6800	1k	Keypad, buzzer, LCD & I/O	16 bit
8251	0050:6C00	1k	UART	16 bit
CS2	0060:0000	2M	LCD driver	8 bit
nCS0	0080:0000	2M	Extended I/O	8 bit
nCS1	00A0:0000	2M	not used	-

### 7.2.4 Interrupt Handler

The ARM CPU has 2 interrupts, FIQ is a Fast non-maskable interrupt and IRQ is a standard maskable interrupt.

Gemini has 11 interrupt sources. The Interrupt handler assigns priorities to these interrupts and routes them to either the FIQ or IRQ inputs of the ARM CPU. Additionally, the interrupt handler controls waking up of the CPU on receiving an unmasked interrupt, if the CPU is in sleep mode.

For GD70 the FIQ interrupt is reserved for the power supply fail priority interrupt.

Interrupt Level Assignments		
Interrupt source	Description	Interrupt detection
IRQ_TIM1	Buzzer timer	Edge sensitive
IRQ_TIM2	operating system timer	Edge sensitive
IRQ_API	DSP Interface interrupt	Edge sensitive
IRQ_EXT	Power supply fail interrupt	Level sensitive
IRQ_USART	UART Interrupt	Level sensitive
IRQ_ARMIO	Keypad Interrupt	Low for 1 clk period
IRQ_FRAME	Frame Interrupt	Edge sensitive
IRQ_PAGE	Page Interrupt	Edge sensitive
IRQ_TIM_GSM		Edge sensitive
IRQ_TSP	Timed serial port Interrupt	Edge sensitive
IRQ_SIM	SIM Interrupt	Level sensitive
IRQ_F_USART	Fast interrupt from USART	Level sensitive
IRQ_RSS	Radio subsystem interrupt	Edge sensitive

## 7.2.5 General Purpose I/O

The general purpose I/O includes keypad scanning, 2 PWM ports and 16 general purpose I/O lines. The general purpose I/O lines are multiplexed onto other functions, if I/O is selected the other function is unavailable.

I/O Pin Assignments					
Signal Name	Pin No.	IO_CTRL	Function	Status	I/O
I/O 0: NLDCDS	117	0	μWIRE_VOICECS		N/A
I/O 1: RXE	116	1	LOGIC_PWR	H = PSU kept on L = PSU off	O
I/O 2: TXE	112	1	nEXT_PWR		1
I/O 3: DTR	114	1	HF_ON	H = Handsfree On L = Handsfree Off	O
I/O 4: DSR	110	1	nIGNITION	H = IGNITION Off L = IGNITION On	I
I/O 5: EXTINT	109	0	nLVA_INT		N/A
I/O 6: NRSTOUT	106	1	PL_CONT	H = Low RF Power level L = High RF power level	O
I/O 7: SIM_RnW	105	1	CHARGE_LED	H = Charging LED on L = Charging LED off	O
I/O 8: SIM_PWCTRL	104	1	SIM_PWRCNT	H: SIM 5V Enable L: SIM 5V Disable	O
I/O 9: SIM_CD	95	1	nON_HOOK	H = Off hook 2nd Handset L = On hook 2nd Handset	I
I/O 10: LT	134	0/1	LT	Backlight On: LT (PWM) Backlight Off: I/O (10) = Low	O
I/O 11: ARMCLK	73	1	nHF_DETECT	H = No Hands Free L = Hands Free connected	I
I/O 12: TSPACT(0)	65	0	BENA		N/A
I/O 13: NPWRCS	56	1	VEGA_PWDN		O
I/O 14: nCS1	50	X	N/C		N/A
I/O 15: nCS0	48	0	nCS0		N/A

Specific I/O are reserved for the backlight, buzzer and keyboard. The luminosity of the backlight and the loudness of the buzzer are controlled by a PWM (Pulse Width Modulation).

The PWM are outputs only.

I/O Pin Assignments		
Signal	Gemini Pin	Use
LT	134	LED backlight 6 BIT PWM
BU	120	Buzzer 6 BIT PWM

The PWM is clocked at 13/3 MHz.

Tones are generated by using timer 1 to switch the buzzer PWM on and off at the frequency of timer 1. By altering the value of timer 1 ringing tones can be played.

During Handsfree operation the ringing tone is derived from the DSP using its tone generator.

This page is left intentionally blank.

## 8 VEGA

### 8.1 Introduction

VEGA contains the interface circuits to the Audio, RF and auxiliary analogue functions for the baseband circuit.

### 8.2 Functional Description

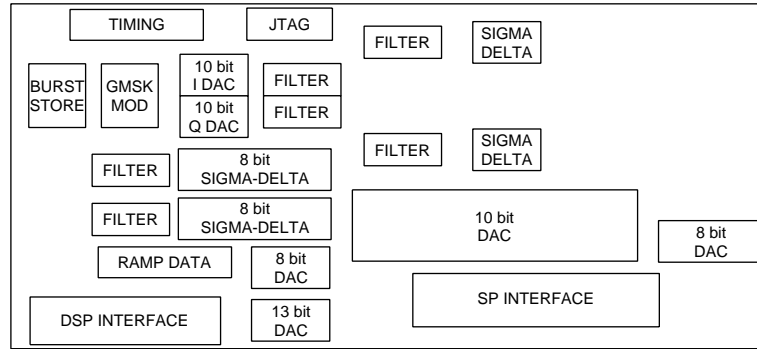


Figure:1 VEGA Block Diagram

600-0801

#### 8.2.1 Uplink I and Q

VEGA performs GMSK modulation on Data samples received from GEMINI at 270 kbits per second.

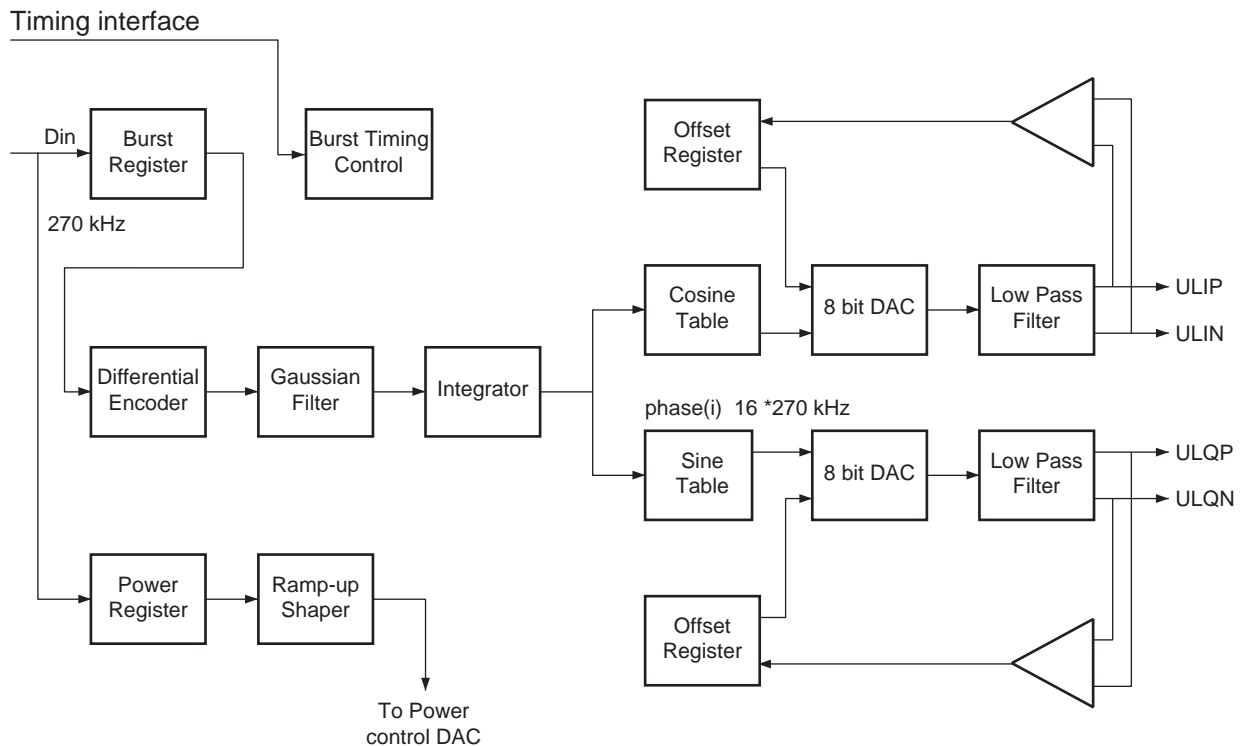


Figure:2 Functional structure of the baseband uplink path

600-0802

8.2.2 Downlink I and Q

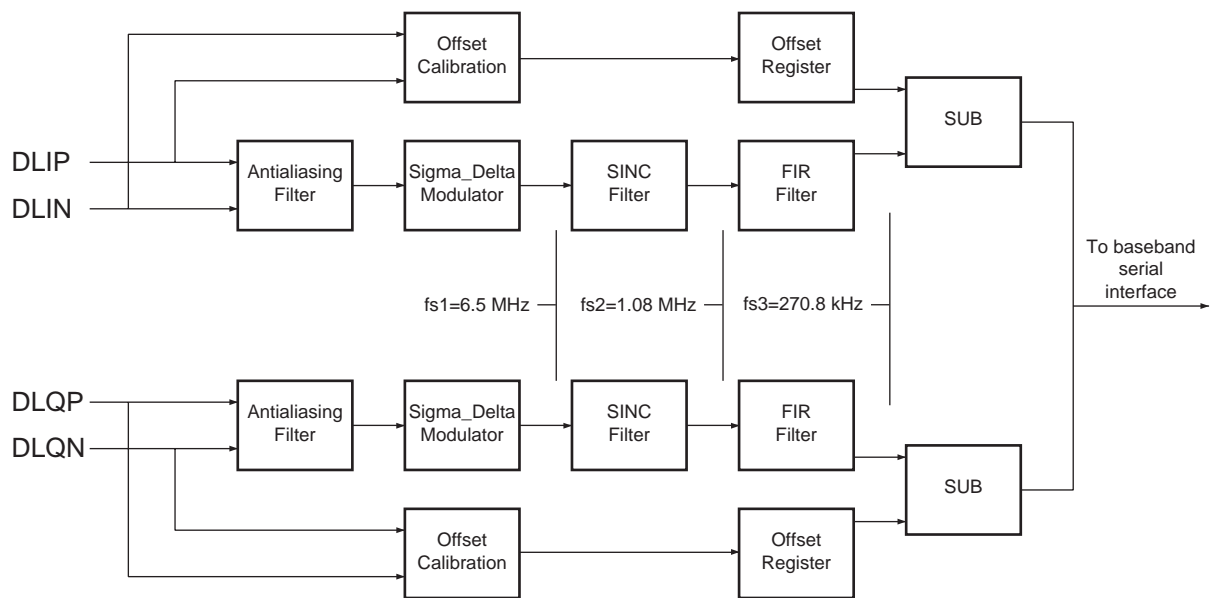


Figure:3 Functional structure of the baseband downlink path 600-0803

8.2.3 Power Amplifier Ramp

The PA Ramp is formed by 2 D/As. The first, a 5 bit D/A, defines the ramp shape; the second, an 8 bit D/A, defines the maximum level.

The ramp shape is defined by 64 steps. The shape can be defined differently for rising and falling ramps. Typically a raised cosine shape will be used as a starting basis of the ramp shape.

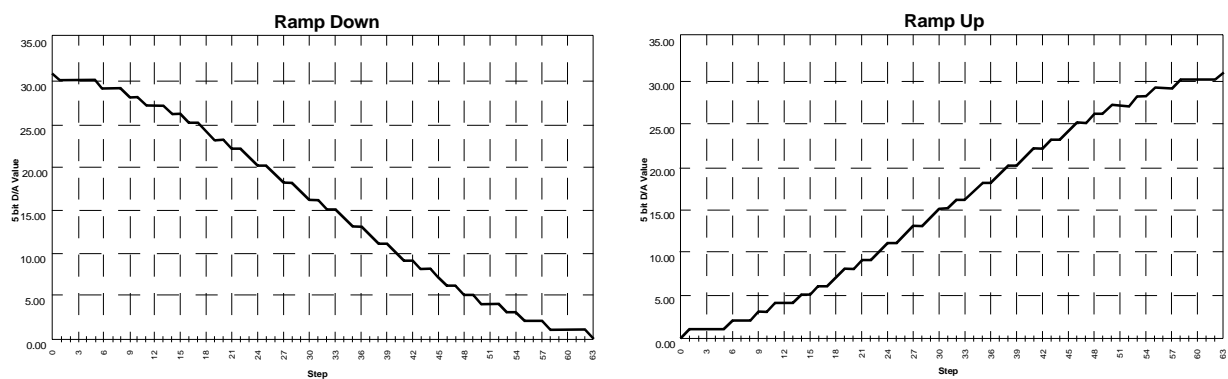


Figure:4 Example for the PA ramp 600-0804

The raised cosine shape will be modified to compensate for RF circuit characteristics.  
The ramp time is selectable between each step being 1/16 of a bit and each step being 1/8 of a bit giving a maximum ramp time of either 14.77  $\mu\text{s}$  or 29.53  $\mu\text{s}$ .  
An 8 bit value is used to program the ramp output level.

### 8.2.4 AFC Control

The 13 MHz system clock frequency is controlled by a 13 bit sigma-delta D/A in the VEGA chip

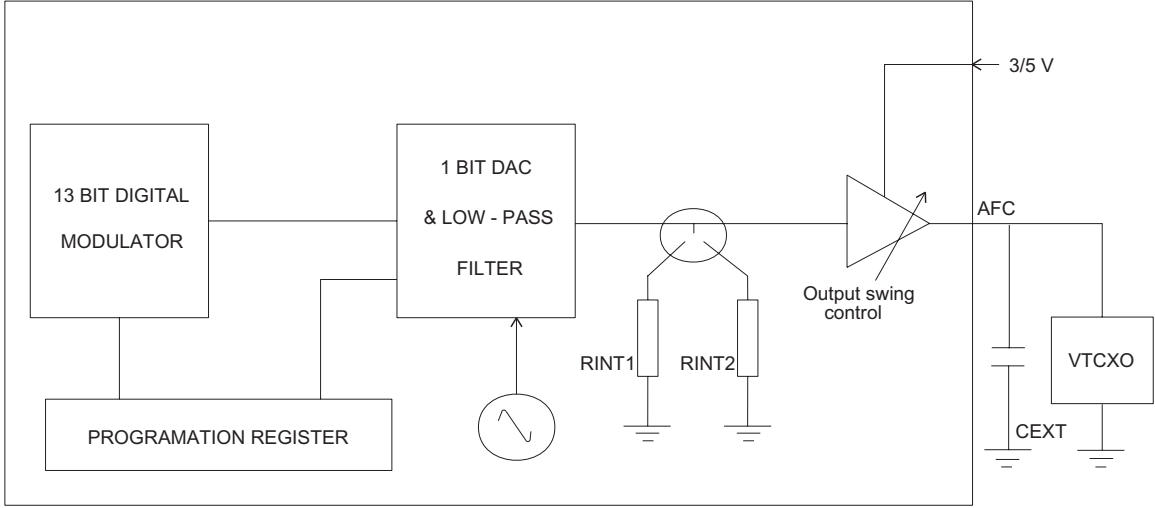


Figure:5 AFC block diagram

600-0805

### 8.2.5 Audio

VEGA provides the analogue interface for the digital audio samples processed by the DSP in GEMINI.

#### Voice Uplink Path

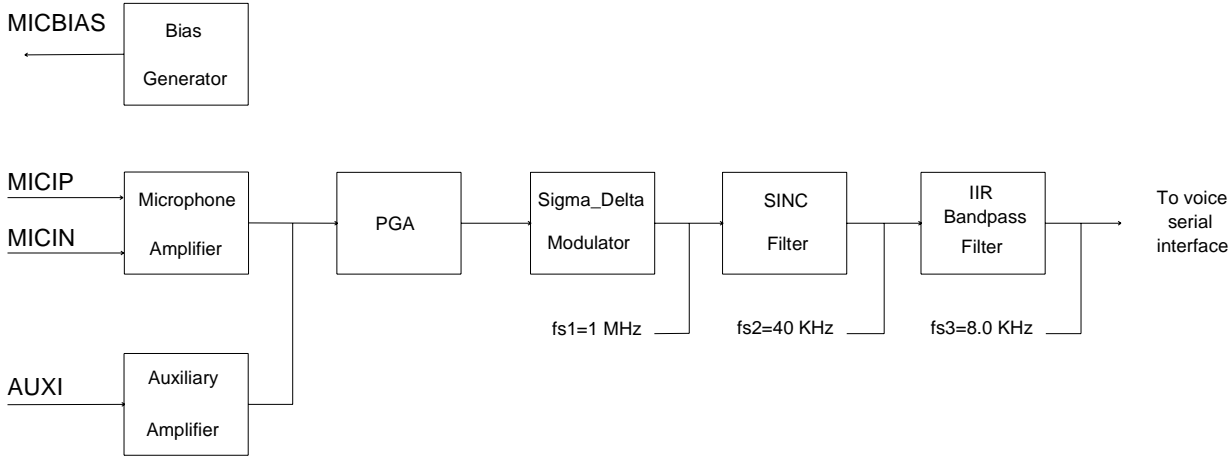


Figure:6 Voice ADC block diagram

600-0806

Voice Downlink Path

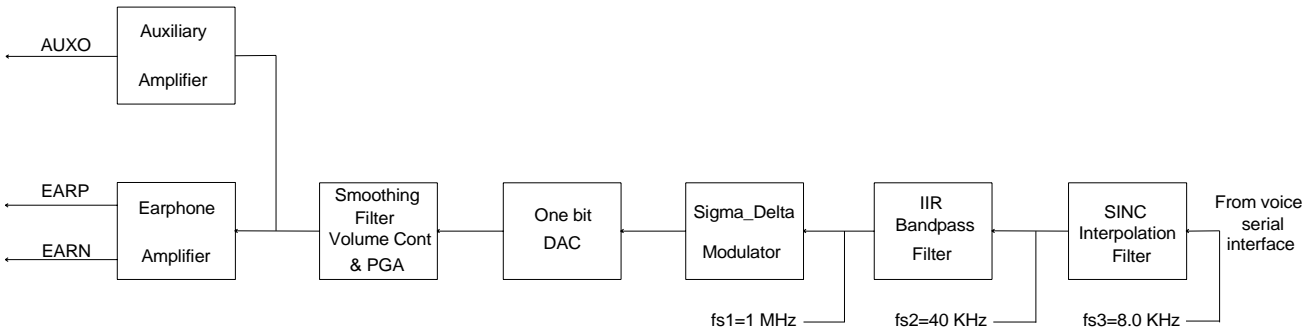


Figure:7 Voice DAC block diagram 600-0807

8.2.6 Auxiliary A/D

VEGA provides 5 A/D inputs. G520 takes advantage of the A/D inputs on VEGA allowing external power to be monitored with just 2 resistors each and no need for a buffer transistor.

VEGA input	Pin Number	Use	Range
ADIN0	36	Battery Voltage	0 = 0V 3FFh = 5.5 V
ADIN1	37	Battery Type	0~144h = Ni-MH 145~3FFh = Li-ION
ADIN2	38	Battery Temperature	372h = -20°C 16Dh = +25°C 06Bh = +70°C
ADIN3	39	nADP_SENSE	385~3FF = No accessory 28D~384 = Headset Adaptor 1E4~28C = SMS Cable 0E7~1E3 = RS232 Direct Cable 000~0E6 = Data Adaptor
ADIN4	40	Current	0h = 0 mA 3FFh = 1200 mA

8.2.7 Charging Voltage Control DAC

Vega provides 10 bits DAC for AGC control. GD70 does not need to control Rx gain by DAC. Therefore, GD70 will use this DAC for charging control, where the output is able to accurately control charging voltage for Li+ battery. GD70 has electrical volume for calibration of this DAC.

## 9 POWER SUPPLIES

### 9.1 Introduction

This section describes the Power Supply Unit (PSU) used on the GD70 logic PCB and the method by which it is controlled. The Battery life during GSM1800 operation benefits from lower transmit power and higher PA efficiency and is therefore more efficient than when operating in GSM900.

This section has detailed information on:

1. An overview of the circuit functionality.
2. Powering-up the phone.
3. Powering-down the phone.
4. Power management.

### 9.2 Overview

The logic circuit uses three separate power supplies as follows:

1. 2.8 Volts supply is used for the main power supply, 2V8 provides power to the digital part of the baseband circuit (Gemini, Memory and LCD). A2V8 is used to power the analogue part of the baseband circuit (Vega and voice memo).
2. 2.5 Volts is provided to power internal blocks within the Gemini, this will be replaced by a 1.8 V supply for the smaller die size Gemini ICs.
3. 5.0 Volts is provided to power the SIM and the SIM interface. This is generated by a switched capacitor charge pump which shifts the nominal 3.6 V battery voltage up to 5 V.

The RF circuit uses four power supplies each provided by a separate 2.8 Volt regulator. They are VSVCO and VSTX which are present when the LO\_EN signal is present, and VSRF and VSVXCO which are present with the signal RF\_ON. The power amplifiers are powered directly from the battery VBATT.

### 9.3 Power-up

The power-up procedure has two phases. If an initial check to see if the battery is in good condition is successful, the second phase determines the source of the power-up request, key press, external power, accessory, etc. and acts accordingly.

The phone can be defined as powered-on whenever the linear regulators are active. It is not always obvious to the user that the phone is powered-on as it may be in one of four modes:

Mode	Description
Sleep	In this mode the CPU has been prevented from deactivating the linear regulators by EXT_PWR. There is no CPU activity.
Charge	The CPU is alive but may perform <i>only</i> battery charging functions and monitor the power key.
Restricted	LEDs light, beeps, can charge battery etc. but it is <i>not</i> permitted to use the radio.
Active	The mobile is fully functional; LEDs light, beeps, search for network etc.

#### 9.3.1 Battery Condition

The CPU must check the battery condition before deciding to power-up. The CPU can measure battery voltage and temperature. If the temperature measurement is invalid, giving a ridiculous temperature reading, a non-standard battery has been fitted, the battery is missing or the whole phone is operating far outside its specified temperature range. In any of these cases the phone must not power-up. The CPU will regularly monitor the battery condition while the phone is on.

If EXT\_PWR is present the regulators will be forced on and the CPU will not be able to deactivate them. If the CPU wants to power-down, all it can do is to enter sleep mode.

Battery Voltage (V)	Temp. reading	EXT_PWR_SENSE	Result
X (don't care)	invalid	0.5 V	Power-down (battery fault)
X	invalid	1.2 V	Sleep (battery fault)
<3.0	X	<0.5 V	Power-down (low battery)
<3.5	valid	1.2 V	LOW
>3.5	valid	X	OK

### 9.3.2 Power-up Sequence

The power-up sequence can be initiated by pressing the power key or by the presence of an external power source on the signal EXT\_PWR. Both enable the linear regulators and the CPU becomes active. The CPU must then check the battery condition; if the phone is not required to power-down or sleep immediately, the result must be OK or LOW. The CPU then checks to see if a hands-free unit is connected by polling the nHF\_SENSE signal, LOW when HF is connected.

Now the CPU can make the decision whether to remain powered-up or not according to the truth-table below. In each case the active parameters are shaded.

Battery Condition	HF	EXT_PWR_SENSE	nIGNITION	KBR0	LOGIC_PWR	Mode
OK	X	X	X	1	1	active
LOW	X	>1.2 V	X	1	1	restricted
OK or LOW	no	>1.2 V	X	0	1	charge
OK	yes	>1.2 V	<0.5 V	0	1	active or charge
LOW	yes	>1.2 V	<0.5 V	0	1	restricted or charge

With a hands-free, the phone can be configured via the MMI to power-up and down with transitions of the vehicle ignition. These are sensed by the CPU on nIGNITION, LOW when the ignition is on.

Any other state than those in the table will cause the phone to deactivate the PSU by setting STAY\_ALIVE LOW.

While the CPU is active, it must monitor the battery condition and accessory connectivity and change state accordingly.

Current Mode	HF	EXT_PWR_SENSE	nIGNITION	KBR0	Battery Condition	New Mode
Charge	X	X	X	1	OK	active
Charge	X	1.2 V	X	1	LOW	restricted
Restricted	X	X	X	0	OK	active

## 9.4 Power-down

There are two power-down procedures:

Procedure	Description
Normal power-down	In this case, the software has full control over the power-down procedure. Calls can be terminated gracefully etc. In some cases the PSU is not deactivated but there is a change of operating mode.
Emergency power-down	This situation is caused by battery removal and is flagged by EXTINT. In this case the CPU only has time to perform a subset of the normal procedure. The priority is to prevent corruption of SIM data.

The truth-table for the power state transitions are shown below, the cause of a transition is shaded. In some cases the phone does not power-down completely but may enter a state of reduced functionality, e.g. from active to charge mode.

When the new mode is OFF or sleep, the CPU will set STAY\_ALIVE LOW.

Current mode	Battery Voltage	HF	Nignition	EXTINT	KBR0	EXT_PWR_SENSE	power-down	New mode
X		X	X	1	X	<0.5 V	normal	OFF
X	X	X	X	0	X	X	emergency	OFF
X	X	X	X	1	1	<0.5 V	normal	OFF
active	<3.5 V	X	X	1	0	>1.2 V	normal	restricted
active	<3.5 V	no	X	1	1	>1.2 V	normal	charge
active	<3.5 V	yes	>2.5 V	1	1	X	normal	OFF
active	<3.5 V	yes	<0.5 V	1	1	>1.2 V	normal	charge
active	<3.5 V	yes	>2.5 V	1	0	X	normal	OFF
active	X	no	X	1	1	>1.2 V	normal	charge
active	X	yes	<0.5 V	1	1	>1.2 V	normal	charge
active	X	yes	>2.5 V	1	1	X	normal	OFF
active	X	yes	>2.5 V	1	0	>1.2 V	normal	OFF
active	X	X	X	1	0	<0.5 V	normal	OFF

## 9.5 Power Management

The power supply circuit supplies regulated power to the base-band parts, controls battery charging and monitors battery usage.

The Power Management section consists of five parts as follows:

1. Power Source.
2. Power On/Off Control & Power Source Failure.
3. Voltage Regulation.
4. Battery Charging & Monitoring.
5. Accessory Control.

The power amplifiers used in the GD70 operate from a nominal 3.6 Volts. GD70 derives this 3.6 Volts from two Lithium Ion batteries connected in parallel, or as an option, three NiMH cells connected in series. The PAs used operate at full specification between 3.0 and 3.6 Volts. They are powered directly from the battery supply to maximise the power available to them.

### 9.5.1 Power Source

Given the high-end nature of the GD70, Lithium-ion (Li+) cells are used for the standard battery pack. The advantages of using Li+ cells are reduced weight, size and improved gravimetric and volumetric energy densities compared to that of the Nickel-Metal-Hydride (NiMH).

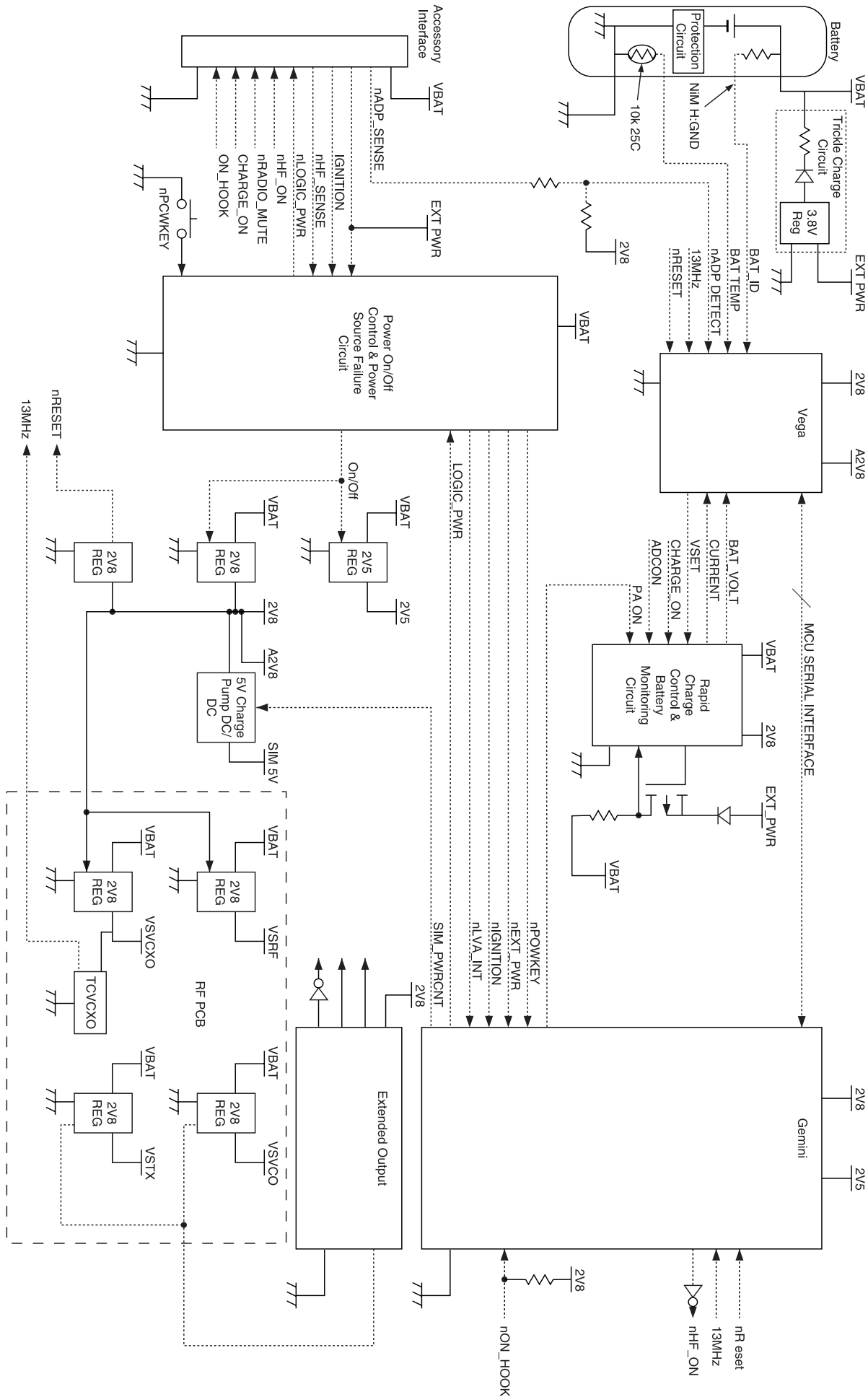


Figure:8 Power supply block diagram

D70-0901

### 9.5.2 Power On/Off Control & Power Source Failure

The hardware model for the Power On/Off Control and Power Source Failure functions can be expressed by the following boolean expression and logic diagram.

$$\overline{\text{On/Off}} = \overline{\text{VBAT}} + (\overline{\text{LOGIC\_PWR}} \cdot (\overline{\text{nLVA\_INT}} + (\text{nPOWKEY} \cdot \text{nIGNITION} \cdot \text{nEXT\_PWR})))$$

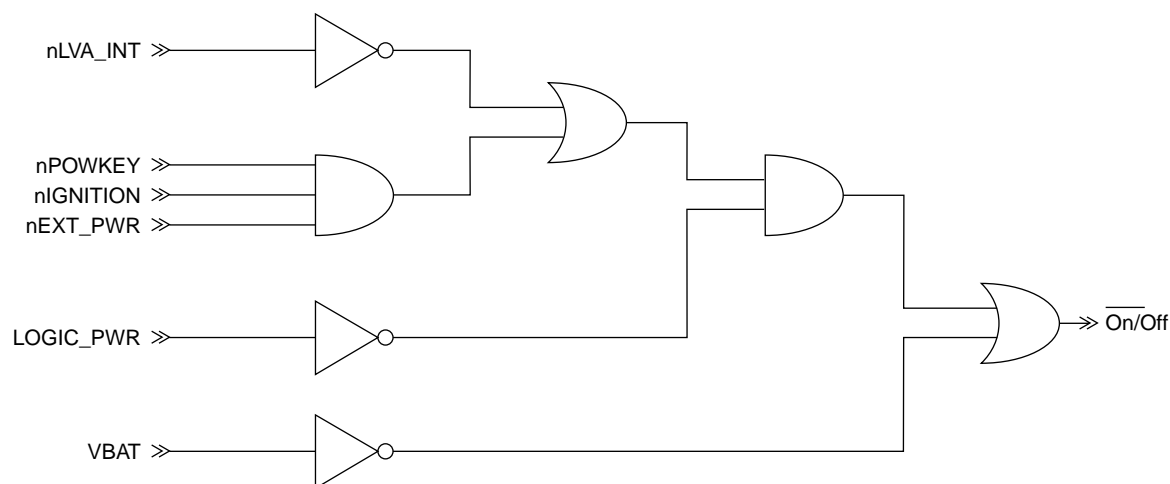


Figure:9 Power On/Off Control & Power Source Failure Logic Diagram

D70-0902

$\overline{\text{On/Off}}$ : Initially this active low signal is under Hardware control, the purposes of which are as follows:

- 1) Enable 2V8, A2V8 & 2V5 voltage supplies to Baseband.
- 2) Enable VSRF & VSVCXO voltage supplies to RF.
- 3) Generation of 13 MHz Master Clock signal.
- 4) Set nRESET signal LOW.
- 5) Wait approximately 200 ms for the voltage output of the regulators and 13 MHz Clock to become stable. Allow reset of GEMINI and VEGA internal blocks.
- 6) Set nRESET HIGH causing the ARM processor to start from address 0.

nLVA\_INT: Power Source Failure Interrupt. Active low signal generated by Low Voltage Detector circuit when VBAT drops below 2.7 V.

nPOWKEY: Active low signal generated by Hardware upon the Power-On Key being pressed.

nIGNITION, nEXT\_PWR and LOGIC\_PWR.

VBAT: 3.6 V nominal battery supply provided either by 2 x Li cells in parallel or 3 x NiMH cells in series.

### 9.5.3 Voltage Regulation

The GD70 has the following power sources:

#### D2V8 : Baseband power supply for digital circuitry (GEMINI, Memory and LCD)

Voltage:	2.8 V $\pm$ 2.5 %
Current:	140 mA max.
Dropout:	100 mV max.

#### 2V5 : Power supply for GEMINI process version 2533C10 (ARM, DSP and ASIC)

Voltage	2.5 V $\pm$ 2.5 %
Current	120 mA max.
Dropout:	400 mV max.

### **1V8 : Power supply for GEMINI process version 1833C07 (ARM, DSP and ASIC)**

Voltage	1.8 V $\pm$ 2.5 %
Current	120 mA max.
Dropout:	150 mV max.

Will replace the 2V5 supply when the 1833C07 process is available.

### **A2V8 : Baseband power supply for Analogue circuitry (VEGA and Voice-Memo)**

Voltage	2.8 V $\pm$ 2.5 %
Current	60 mA max.
Dropout:	150 mV max.

### **SIM5V : SIM power supply (SIM & GEMINI/SIM interface)**

Voltage	5.0 V $\pm$ 5 %
Current	20 mA max.

### **EXT\_PWR : Power supply for battery charger**

Voltage	5.8 V $\pm$ 0.2 V
Current	650 mA $\pm$ 50 mA

**2V5 :VSVCO, voltage supply for VCO, only turned on when LO\_EN signal is high**

**2V5 :VSTX, voltage supply for the transmitter, only turned on when LO\_EN signal is high**

**2V5 :VSRF, voltage supply for RF circuit, only turned on when RF\_ON signal is high**

**2V5 :VSVXCO**

## **9.5.4 Battery Charging & Monitoring**

The status of the LCD battery icon is determined by the value of BAT\_VOLT returned from VEGA, the battery ICON has 4 states.

The battery charging is controlled by the CPU within the phone. If rechargeable cells are detected and the temperature is within specified limits the charger starts a rapid charge algorithm.

When the battery is NiMH, charging is determined by  $\delta V$  with time, temperature and voltage safe-guards. When the battery is Li+, charging is determined by constant current and constant current voltage with time, temperature, current and voltage safe-guards. A current limit no greater than the maximum charge current for any battery option must be provided by the external power source.

In the case of deeply discharged batteries there may not be enough power in the battery to initiate a charge. Therefore, the charging circuit must automatically start to trickle charge until there is enough power to switch on the phone.



