# RF Power Meter 6960 

Including Option 3964-650 (GPIB Interface)

## AMENDMENT RECORD

The following amendments are incorporated in this manual.

| Amendment <br> No. | Date | Issued at serial no.: |
| :---: | :---: | :---: |
| Am. 1 | Mar. 85 | 518 |
| Am. 2 | July 86 | 1069 |
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| Am. 4 | Nov. 87 | 1820 |

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2 Installation These chapters are contained in a
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6 Replaceable parts
7 Servicing diagrams

## HAZARD WARNING SYMBOLS

The following symbols appear on the equipment
Symbo1 Type of hazard Reference in manual

| Static sensitive device | Vol. 2, Page (iv) |
| :--- | :--- |
| Supply voltage | Vol. 2, Page (iii) |

Note ...
Each page bears the date of the original issue or the code number and date of the latest amendment (Am. I, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus $\rightarrow . f \ldots$ to show the extent of the change. When a chapter is reissued the triangles do not appear. Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded $\mathrm{C} 1, \mathrm{C} 2$ etc.

## NOTES AND CAUTIONS

## ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

## Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers
$\triangle$ Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

## Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

## Primary fuses

$\triangle$ Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A .

Make sure that only specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

## CAUTION: STATIC SENSITIVE COMPONENTS

Components identified with the symbol $\triangle$ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.
(I) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.
(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.
Metallic tools earthed either permanently or by repeated discharges.
A low-voltage earthed soldering iron.
An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.
(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.
(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

## WARNING: HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges, care should be taken, particularly when servicing the equipment, to avoid minor cuts.

Lithium: A lithium battery is used in this equipment. Under no circumstances must any lithium battery be crushed, incinerated or disposed of in normal waste. They must be separately and securely packed and any exposed electrical connections adequately insulated to avoid a short circuit occurring during transit. They must be clearly identified to show the nature of the hazard and then disposed of in a safe manner by an authorized toxic waste contractor.

## WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

## Chapter 4

## TECHNICAL DESCRIPTION

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## OVERALL CIRCUIT DESCRIPTION

1. Refer to the 6960 block diagram shown in Fig. 1. The r.f. sensor gives a low d.c. voltage when power is applied. This d.c. signal is converted to an a.c. signal by the signal chopper enabling high gain, low noise amplifiers to be used.
2. The chopped signal is fed to the first amplifier which is split into two parts, the first part being in the r.f. sensor package and the other in the power meter. The signal is then passed to the spike blanking circuit which removes spikes on the edges of the square wave signal produced by the signal chopper. The following buffer also corrects for sensor non-linearities. The signal is then fed to the 1 st attenuator which, together witb the 2 nd attenuator controls the gain of the amplifier strip in 10 dB steps. The 2nd and 3rd amplifiers provide the rest of the required gain. The 4th amplifier, together with the gain $\mathrm{D}-\mathrm{A}$, provides fine adjustment of the a.c. gain.


Eig. 1 RE Power Meter 6960 block diagram
3. The phase synchronous detector then synchronously de-modulates the a.c. signal. Timing signals for the signal chopper, spike blanking and the detector are provided by the timing logic. The recovered d.c. signal passes to the peaking meter and, via a switch to the comparator.
4. The microprocessor ( $\mu \mathrm{P}$ ) runs the program stored in read only memory. Data storage is achieved by using non volatile RAM (Random Access Memory) • Outputs from the microprocessor drive the zero D-A, the 14 bit D-A, the gain D-A, the recorder D-A, the attenuator drives, the liquid crystal display, the GPIB interface and the power reference. Inputs to the microprocessor are taken from the comparator, the keyboard and the GPIB interface.
5. Power for all of the stages is provided by the PSU.

## DETAILED TECHNICAL DESCRIPTION

## Analogue p.c.b.

6. Refer to Chap. 7, AAOI circuit diagram.
7. First amplifier (sheet I). ICI and associated components form the second part of the 1 st amplifier, the first part being in the power sensor assembly. When using the 6910 series sensors this amplifier has a gain of approximately 1000 . Fig. 2 shows a simplified complete amplifier.
8. AC gain is controlled by the components in the emitter circuit of the power sensor transistor. DC bias for the transistor is set by RI to RS. C2, C6 and C9 control the high frequency response and the capacitor in the sensor controls the low frequency response. The amplifier has a band-pass characteristic centred at the chop rate of 925 Hz .


Fig. 2 First amplifier
9. $\underline{0}$ VA control. Ie2, RIO, RII and TRI provide a very low offset source follower which provides an earth reference from the signal ground in the power sensor. This earth reference, indicated by 0 VA , is used by the rest of the a.c. gain stages. DI, D2 and R9 ensure that the earth reference only moves a small amount (about 0.5 V ) when no sensor is connected to the power meter.

ID. Spike blanking. The spike blanking circuitry, R114, Cl6 and IC3c, remove spikes that are generated on the leading and trailing edges of the chopped d.c. signal from the r.f. sensor (see Fig. 3). IC3c and CI6 act as a sample and hold circuit. The hold period is from when the signal chopper changes state and lasts for a period of $180 \mu \mathrm{~s}$. RI14 reduces errors caused by the hold time interfering with large signal levels at high r.f. power levels. IC4b acts as a high impedance buffer for the signal from the sample and hold.


Fig. 3 Spike blanking
11. First attenuator. Precision resistors RI4 and R15 with IC3a, IC3b form a switchable, divide by 100 attenuator for range changing (see Table 1). C23 together with the two resistors forms a high-pass filter for bandwidth control.

TABLE 1 ATTENUATOR CONTROL

| Range | Total | Attenuator switches |  |  |  |  |
| :---: | :---: | :---: | :--- | :--- | :--- | :--- | :--- |
|  | IC3a | IC3b | IC10a | IClOb | IC10c |  |
| 1 | None | ON | OFF | ON | OFF | OFF |
| 2 | $1 / 10$ | ON | OFF | OFF | ON | OFF |
| 3 | $1 / 100$ | OFF | ON | ON | OFF | OFF |
| 4 | $1 / 1000$ | OFF | ON | OFF | ON | OFF |
| 5 | $1 / 10000$ | OFF | ON | OFF | OFF | ON |

12. Second amplifier. IC4a with feedback components R22 and R23 form the second amplifier. The gain is approximately 25 . C35 controls the high frequency roll off.
13. Second attenuator. R24 to R26 and ICI0 form the second attenuator. The principle of operation is the same as the first attenuator described above. This attenuator also has a divide by 10 setting.
14. Third amplifier. The third amplifier stage has a gain of about 35. Resistors R30 and R31 control the gain of IClla. C38 controls the high frequency roll off.
15. Fourth amplifier. The fourth amplifier is different from the other amplifier stages, in that its gain can be controlled very precisely. It is basically a standard gain stage (ICllb, R3?, R38), but having both inverting and non-inverting inputs. The main signal is applied to the non-inverting input which has a gain of approximately 3 . When a signal is applied to R37 and the inverting input, from the gain D-A which uses the main signal as its reference, the gain of the amplifier is reduced. This allows the gain to be finally controlled over the range $I$ to 3 .
16. Phase synchronous detector (sheet 2). The input a.c. signal is restored to d.c. by this circuit. Samples of the signal are taken on each half cycle by closing the switches ICI4a and IC14d alternately, with c49 and C50 charging up to the sample voltage during the time the switch is closed. These sample and hold capacitors must be able to charge and discharge rapidly to ensure a fast response to changes in signal level. The time constant is determined by the effective impedance of the switch and the qutput of 4th amplifier ICllb and the value of C49 and C50. Together theSe allow an almost complete sample to be obtained within the sample period.
17. When the power meter is on the most sensitive range (range 1 ), resistors R53 and R54/R115 are placed in series with the coupling switches. These increase the charge time of the capacitors so forming a very low frequency lowpass filter.
18. ICI5 acts as an instrumentation amplifier offering a high impedance to C49 and CSO so maintaining their charge and allowing a shift of earth reference to the 0 VC reference used throughout the d.c. stages. Precision resistors $\mathrm{R} 34,35,36$ and 42 ensure that the gain on each input is the same otherwise linearity errors would result if these differed.
19. The output from ICISb is then fed to the peaking meter via R78 and the comparator, ICI?, via switch ICI6b. This output is also used for the levelling output after being passed through the low-pass filters, R58 and C60, and buffer ICI8b.
20. Comparator and A-n conversion. The comparator output is taken to the Serial Input Data (SID) pin of the processor. The inverting input is driven from the 14 -bit D-A. The non-inverting input is driven from either the phase-synchronous detector or the Zener diode in the sensor. This arrangement allows the processor to make successive approximation analogue-to-digital conversions. To do this the processor sets the most significant bit of the 14-bit D-A. It then reads SID to check the output of the comparator. If the output of the comparator is high the data is kept; if not the bit is set to reset. The processor continues by setting each bit in turn, deciding whether to keep or discard each bit until all 14 bits have been checked.
21. Sensor Zener diode drive. The Zener diode in the sensor is used to decide which type of sensor is in use. The Zener diode is driven fom a 5 mA constant current circuit consisting of R77, RII6, DID, DII and The voltage from the Zener diode is scaled by RI12 and RI13 before being applied to the comparator.
22. The type of sensor in use defines the required scaling and linearity corrections that must be applied to give a true power reading. Table 2 indicates the Zener voltages used with the appropriate scaling and corrections that are applied.

TABLE 2 SENSOR ZENER VOLTAGES

| Zener <br> oZtage | Sensor <br> Type No. | Sensor <br> top power | Thermo-electric sensor <br> Zinearity correction | Diode sensor <br> Zinearity correction |
| :---: | :---: | :---: | :---: | :---: |
| 2.7 | 0920 | D $\mu \mathrm{W}$ | NO | YES |
| 3.3 | - | ID $\mu \mathrm{W}$ | NO | NO |
| 3.9 | Spare | - | - | - |
| 4.7 | - | 30 mW | NO | NO |
| 5.6 | 6910 | 100 mW | YES | NO |
| 6.9 | 6912 | 100 mW | YES | NO |
| 9.2 | - | IOW | YES | NO |
| 10.0 | - | $100 ~ W$ | YES | NO |

23. Timing logic (sheet I). ICs 5 to 9 and their associated components provide all the timing signals for the power meter. Outputs from this section of circuitry drive the signal chopper in the power sensor, the spike blanking and the phase synchronous detector. The basic frequency of operation is 925 Hz .
24. The master oscillator is IC5 which is a gated astable (4047) set permanently on by its control lines. Three outputs are provided by rC5; pin 13 is at twice the 925 Hz chop rate and pins 10 and II provide complementary 925 Hz square waves.
25. The output from rC5 pin 13 drives IC6 which is wired as a monostable with a period of $180 \mu \mathrm{~s}$. The timing components of IC6 are RI8, R55 and C24. The output from IC6 provides the sample/hold timing for the spike blanking switch, rC3c.
26. The output from IC5 pin 13 also drives the input of one half of $1 C 7$, a precision dual monostable. The first monostable provides the delay before the sample pulse required by the phase synchronous detector. This then drives the second monostable providing sample pulses on each half cycle of the chopped waveform. Two NAND gates, part of ICB, are used to direct the pulses to the correct sample switch in the detector.
27. Both of the 925 Hz signals from IC5 are used to derive the chopper drive signals for the power sensor. Both signals are delayed at the input of IC9, a dual D-type bistable, by the action of R27, C32 and R28, C33. Outputs at pins 1 and 13 are out of phase, with the signal from pin 13 having the greater duration and leading that from pin 1 by a fractional amount. The difference in phase relationship ensures a predetermined signal chopper f.e.t. on/off sequence of operation.
28. Fig. 4 shows the relationships of the timing signals.


IC $8 \quad$ (3)
SAMPLE 1
rC 8 (4)
SAMPLE 2
29. D-A converters. The 14 -bit D-A (sheet 2 ) is a CMOS multiplying D-A converter. Its digital inputs are generated on processor p.c.b. AA02. The D-A Ie21, with operational amplifiers IG22 and IG23, is arranged to give a bipolar output of approximately $\pm 6.2 \mathrm{~V}$. Resistors R72 and R76 adjust any offsets generated by the operational amplifiers and R70 adjusts the centre point of the D-A output.
30. The -6.2 V reference required by the D-A circuit is generated from an ultra-stable Zener diode, D13. The Zener diode is driven from a 7.5 mA constant current source consisting of R74, R75, DI4 and TR6.
31. Serial D-A's. The Gain D-A (sheet J) Zero D-A and Recorder D-A (both sheet 2) are all based on the same type of multiplying D-A converter, the AD 7543. This device is special in that data is loaded into it serially (see Fig. 5). The DAC's logic circuitry consists of a 12 -bit serial-in parallel-out shift register and a 12 -bit DAG input register. Serial data at the SRI pin is clocked into the shift register on the trailing edge of STB3. Once the shift register is full its contents are loaded into the DAC input register by sending LDI low. These control signals are derived on the processor p.c.b. AA02.


Fig. 57543 Serial V-A
32. The Gain D-A is arranged for unipolar output using lC13. See 'Fourth amplifier' above for more details of how this D-A is used.
33. The Zero D-A circuitry provides a small voltage which is sent to the sensor to null out any offsets generated by the signal chopper. The D-A, ICI9 and IC20a provides a unipolar 0 to +6.2 V output. This is fed to operational amplifier IC20b which also has a -6.2 V reference input. This provides a -3.1 V to +3.1 V output from IC20b pin 7 which is then scaled down by R67 and R68 before going to the sensor. The -6.2 V reference for ICI9 and amplifier 1C20b is generated by a low drift Zener diode, D12.
34. The Recorder D-A provides a 0 to +10 V output for use with chart recorders etc. The -10 V reference voltage to do this is generated from the ultrastable -6.2 V reference DJ3. It is amplified to -10 V by ICI8a and associated components. R 81 is used to adjust the -10 V to give the correct scaling to the recorder output. R82 provides the ability to null out any offset on IC25, part of the D-A circuit.
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35. Power supply (sheet 3). Four basic d.c. supplies are required by the 6960 Power Meter. positive and negative IS V rails are used for all the amplifiers, a 5 V low current rail is used for the timing circuitry and a high current 5 V for the processor and GPIB boards. Basically there are three parts to these supplies; a raw d.c. supply, switching regulators and in all cases, except for the high current 5 V supply, linear regulators.
36. The raw d.c. supply is provided by mains transformer TI, bridge rectifier DI5 and reservoir capacitor C82. The primary circuit of TI is switched to cater for mains supply inputs of 115 V and 230 V . This raw d.c. supply varies from about 10 V to 20 V depending on the actual supply voltage.
37. The +15 V and -IS V supply rails are derived from a step-up switching regulator set for approximately 20 V out, followed by linear regulators to give IS V. This ensures clean supply rails for the amplifier stages.
38. The theory of the switching step-up regulator is as follows (refer to Fig. 6): when the switch closes, the applied voltage (Va) drops to almost zero (Va-Vs), and the voltage Vin-Vs is applied across the inductor, causing the inductor current to increase linearly. Because the applied voltage is less than the output voltage, the diode is reverse biased and current cannot flow to the output. Again, when the switch opens, the inductor current cannot change instantly, and the applied voltage changes to the total of the output voltage plus the diode voltage. At this time current can flow through the diode to the load capacitor, and the inductor current decreases at a linear rate, determined by Vout-Vd-Vin. Timing adjustments control the average diode current (Id) so it is equal to the load current. If the load current is less than the maximum output current, off time is increased by a dead time with no current to the output. Input current can flow during both on and off times, so the average input current is always greater than the output current.
39. IC26 contains most of the components required by this type of regulator. The switched d.c. is also used to provide a simple negative supply. C8S a.c. couples the switching power to d.c. restoration diode D17. DI8 then rectifies it. with C86 providing the output capacitance.


Fig. 6 Step-up voltage regulator
40. The positive and negative outputs from the switching regulator are filtered by L2, L3, C87 and C88 before being applied to the inputs of the linear regulators. IC 27 is the +15 V three terminal regulator and Ie28 the -15 V regulator. C 89 and e90 decouple the outputs of IC 27 and IC28 to reduce noise and possible oscillations. D32 to D35 protect the regulators if one or other fails.
41. The low current +5 V is used by the timing logic. This is derived from the +15 V rail by series resistor R89 and Zener diode D19.
42. The high current +5 V is used by the processor board, AA02; the display board ABO 1 and the GPIB board. The regulator is of the step-down switchmode type.
43. The basic theory of the step-down switchmode regulator (refer to Fig. 7) is as follows: When switch $S$ closes, the voltage Va rises close to Vin (Vin-Vs), and the voltage Va-Vout is applied across the inductor causing the current to rise from zero. This current flows from the switch through the inductor and into the load and output capacitor. When the instantaneous inductor current, $i L$, is less than the load current, the capacitor provides the extra current and Vout decreases slightly. When iL exceeds the output current the remaining current flows into the capacitor, increasing Vout; iL will increase until the switch is turned off. At this instance, since the inductor current cannot change instantly, Va falls to $-V d$ so diode $D$ can turn on and provide the inductor current. The voltage across the inductor is now -(Vout-Vd) so the change in inductor current will be negative. The inductor current continues to fall toward zero until $S$ turns on again and the cycle is repeated. The electronics in the system controls the on and off time of $S$ so that the average inductor current equals the output current; the average capacitor current will be zero, and Vout will remain constant.


Fig. 7 Step-down voltage regulator
44. The controlling of the +5 V regulator is performed by IC29. Transistors TR7 and TR8 level shift and amplify the output from IC29 to drive the m.o.s. f.e.t. TRIO which acts as the switch. TR9, D22 and C95 ensure that there is sufficient drive voltage available on the gate of TRIO to turn it on properly. L4 is the switched inductor; C98 the output capacitor and D23 the recovery diode. Voltage feedback is via R96 and R97, allowing the output voltage to be set correctly.
45. Additions to the basis supply provide over-current and over-voltage protection. Resistors RI05 and RI06 sense the current flowing into the inductor. When the voltage across the resistor reaches approximately 0.6 V , TR13 is turned on; which turns on thyristor D27. This removes the gate drive from the m.o.s. f.e.t. switch, TRIO. The thyristor is held on by the current flowing through l.e.d. D29, and series resistor RIIO. When the output voltage
exceeds 5.6 V , Zener diode D 30 starts to conduct and will fire thyristor D31 when enough current is flowing through the Zener diode. When D31 is turned on, a very high current is drawn from the supply and the current limit circuit comes into operation.
46. The +5 V supply is filtered by the action of L5 and C99.

## Power reference

47. Refer to Chap. 7, AC 04 circuit diagram.
48. The power reference supplies a low spurii 50 MHz carrier levelled at 1.00 mW . The reference oscillator is enabled by a digital control signal applied to the transistor switches TRI and TR2. Applying 0 V turns TRI off thus turning TR2 on, enabling the power reference. When a positive voltage of greater than 1.5 V is applied to RI, TRI turns on, turning TR2 and the power reference off.
49. TR3 and associated components form a modified Hartley oscillator that can be level controlled by the second gate on the m.o.s. f.e.t. Output is coupled from the source of TR 3 by $C B$ to the matching and harmonic rejection circuit consisting of CIO to CI2 and L3. The matching circuit then feeds detector D2 and d.c. blocking capacitor C18. As the source impedance of a levelled circuit is $0 \Omega$ a $50 \Omega$ source resistor is required. This is combined with a 2 dB attenuator in RII. R12 and RI3 form the rest of the attenuator which then passes r.f. power to the output.
50. The output from the detector diode, $D 2$ feeds one side of the levelling comparator ICla. The -6.2 V voltage reference input is buffered by IClb, the gain being set by R15, R16, RI8 and R19. The resultant reference voltage is fed via D3 which is used to provide temperature compensation for D2, to the non-inverting input of ICla. The output of ICla drives the level control gate of the oscillator transistor TR3.

Processor p.c.b.
51. Refer to Chap. 7, AA02 circuit diagram.
52. The processor board contains an $8085 \mathrm{AH}-2 \mathrm{CPU}$, buffers for the address and data lines, address decoding, EPROM, non-volatile RAM, programmable peripheral interfaces (PPIs) and reset circuitry. Components and their interconnections are briefly described below, full descriptions of the 8085 CPU and 8255 PPIs can be found in "MCS85 Users Manual" publishec by Intel Corporation. The purpose of the c.p.u. is to control the instrument by means of the address and data buses. The program is contained in the EPROM and data is stored in the non-volatile RAM. The c.p.u. is an 8 -bit n.m.o.s. microprocessor with interrupts, and features a multiplexed address/data bus.
53. The c.p.u., IC3, uses a 10 MHz crystal for its clock generator. This is internally divided down to give a 5 MHz operating frequency. At power-on a reset is applied to IC3 pin 36. The reset instruction RESET IN, lasting for at least three full clock cycles synchronizes with the internal clock and resets the following:-
(I) Program counter is cleared.
(2) Instruction register is cleared.
(3) Interrupts are disabled.
(4) All tri-state bus lines are floated (ALE is not tri-state).

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54. Address decoding. Address and data lines are multiplexed, pins A8-A15 are output-only lines carrying the high-order byte of memory addresses. ADOAD7 are bi-directional lines which output the low-order byte of memory addresses and also double as a bi-directional data bus. The top four address lines, A12-A15 are decoded by lC7 3 to 8 decoder to give addressing blocks of 4 k in the bottom half of the memory map.
55. Wait states. The operation of the c.p.u. is directed into read and write sequences called machine cycles. These may contain from 3 to 6 clock cycles (or T states) with the instruction fetch MCl containing a minimum of four T states and the remainder three (see Fig. 8). A memory read must occur within three clock periods for in this time lC3 places the input into the instruction register.


Fig. 8 Machine cycle. Wait state and Fetoh instruction (AAOZ)
56. Slower input/output devices require more time to respond therefore it is necessary to delay the input to the instruction register. Provision for this is made by the ability of the c.p.u. to generate a 'Wait clock periods'. The READY signal line is sampled by the c.p.u. at the clock period T2, if this is at logical low a Wait clock period will follow, further Wait clock periods would be generated until the READY signal line is asserted high One Wait clock period only is required by the 6960, the clock periods and signals generated in the first machine cycle are shown in Fig. 9. IC6 and ICIOc,d circuit holds the READY line low for one count only then asserts high, the next clock period T 3 then follows.
57. As only Wait states are required by PPls ICI2 and ICI3, the Wait clock period is generated only when address line AI4 goes high, i.e. for addresses in the range 4000 H to 7 FFFH .
58. Address and data buffering. IC4 Address buffer is an octal transparent latch and de-multiplexes the low-order address and data lines by means of the ALE (Address Latch Enable) signal. Timing requirements cause some noise spikes on the output latched address lines; these are caused during the transition from Data to Address and are to be expected.
59. IC5 Data buffer is an octal bus transceiver and buffers data to and from the data bus (DO-D7). The direction of the transceiver is controlled by the read (RD) signal from the c.p.u. Data is sent to the c.p.u. when the read line is logical low.
60. EPROM. The instrument operating program is contained in IC8, which is an ultraviolet erasable EPROM. The EPROM is an $8 \mathrm{k} \times 8$-bit device.
61. The EPROM is accessed when its CE enable line is logical low. The outputs remain tri-state until the output enable, OE, line goes low. At this time the data from the location in the EPROM specified by the state of address lines A0 to AI2 is placed on the data bus. Fig. 9 shows the decoding for the EPROM and other devices.
62. RAM. The random access memory is a $2 \mathrm{k} \times 8$-bit c.m.o.s. device. This allows a small battery to provide standby power making the RAM non-volatile. The select line from decoder IC7 is inverted by ICIOb before being NANDed with the c.p.u. Reset line. The NAND gate is made up from D6 to D9, RI7, RI8 and TR2. The output from TR2 collector drives IC9 CS. When the 6960 is powered down TR2 is turned off by the reset circuitry ensuring that no locations of the RAM can be written to as the +5 V supply fails.
63. The direction of data to and from IC9 is controlled by the output enable, OE, and write enable, WE, control lines. When WE is logical high and $O E$ is low, data is output from the RAM to the data bus. If $D E$ is high and WE is low data is written into the RAM.
64. When the 6960 is powered down, the standby power for IC9 comes from Lithium battery BI. The battery is isolated from the +5 V power supply by special diodes DIO and DII. DIO has extremely low reverse leakage so that no power passes from the battery to the supply rail. DII has a very low forward voltage so that the battery can be used until the voltage out is approximately 2 V . The expected lifetime of the battery is a minimum of 5 years and possibly 10 years.

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| ADDRESS HEXADECIMAL <br> B000 |  | ADDRESS LINES |  |  |  | SELECTED IC |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | AI5 | AI4 | AI3 | AI2 |  |
|  | - | 0 | I | I | I | SPACE |
| 7000H | $\begin{gathered} \text { PPI 2 } \\ (3 \mathrm{LOCATIONS}) \end{gathered}$ | 0 | I | I | 0 | ICI2 |
| 6000H | $\begin{gathered} \text { PPI I } \\ (3 \text { LOCATIONS }) \end{gathered}$ | 0 | I | 0 | I | ICI3 |
| 4000H | $$ | 0 | I | 0 | 0 | $\begin{aligned} & \text { AAII } \\ & \text { IC7 } \end{aligned}$ |
|  | GPIB CONTROLLER ( $B$ LOCATIONS) | 0 | 0 | I | I | $\begin{aligned} & \text { AAII } \\ & \text { lel } \end{aligned}$ |
| $3000 \mathrm{H}$ |  |  |  |  |  |  |
| 27 FFH 2000 H | $\begin{array}{r} \text { DATA AREA } \\ +(\text { RAM }) \end{array}$ | 0 | 0 | I | 0 | IC9 |
| IOOOH |  | 0 | 0 | 0 | 1 | ICB |
|  | PROGRAM | 0 | 0 | 0 | 0 | 1 CB |
| 0000H |  |  |  |  |  |  |

Fig. 9 Memomy decoding
65. Reset control. The reset control circuitry is used to inform the c.p.u. of a power-down situation and to ensure that the c.p.u. itself powers down clearly. Fig. 10 shows a simplified diagram of the reset control circuit. The TRAP, non-maskable, interrupt is used to inform the c.p.u. of an impending loss of supply. When this interrupt occurs, the c.p.u. stores the current front panel settings in STORE 0 so that they may be recalled on power-up. When the RESET IN line on the c.p.u. becomes logical low the c.p.u. halts any processing and sends all outputs to a tri-state mode.

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Fig. 10 Simplified reset control cirouit
66. The first half of dual rectriggerable monostable ICI, is triggered by a.c. derived from the secondary of the mains transformer. Thus the monostable remains triggered until the mains supply is removed. The pulse duration of ICI part I is set to 27 ms so that supply frequencies as low as 45 Hz may be used. When the monostable is no longer triggered the QI low output goes high, raising the TRAP interrupt. At the same time QI high goes low which sends the RESET IN line of the c.p.u. low 4.5 ms later. During this time the settings are stored in RAM. The 4.5 ms delay is generated by delay network R5 and C3. QI low is NANDed together with the c.p.u. RESET IN line by IC2a. The output from the NAND gate is fed via D3 to the clear, Cl , input of the monostable. This ensures that the monastable remains in the same state even if the mains supply recovers. Potential divider R22 and R23 also ensure that the monostable stays un-triggered until the +5 V rail has reached a satisfactory value.
67. The front panel key RESET fires the second monostable after a 200 ms delay fixed by R7 and C5. This monostable has a duration of 180 ms . The Q2 low output is taken to the clear input ( Cl low) of the first monostable. Therefore the RESET key has the same function as turning the supply off, but allows the c.p.u. to be reset without removing any supplies, ensuring stability of the 6960 amplifiers etc.
68. The dual monostable and the NAND gates, ICI and IC2, are supplied with power via D4 and storage capacitor C4. This ensures that the CPU, TRAP and RESET IN lines remain steady until all power has been removed from the rest of the processor board.
69. PP1s. ICI2 and ICI3 are general purpose Programmable Peripheral Interface (PPI) devices type 8255. Each has 24 I/O pins which may be individually programmed in two or three groups. These are three major modes of operation but only one of these is used. For more details of the 8255 it is best to refer to the Intel publication 'MCS-85 User's Manual'. In the operating mode selected the I/O pins are split into groups of 8 which may be used as either input or output pins. Table 3 shows how the groups are allocated and the circuitry to which each goes.

TABLE 3 PPI PORT ALLOCATIONS

| PPI | Port | In or Out | Bit | Controls or Reads |
| :---: | :---: | :---: | :---: | :---: |
| I | A | Input | 0 | Keyboard ABOI |
|  |  |  | 1 |  |
|  |  |  | 2 |  |
|  |  |  | 3 |  |
|  |  |  | 4 |  |
|  |  |  | 5 |  |
|  |  |  | 6 |  |
|  |  |  | 7 |  |
| ICI3 | B | Input | 0 |  |
|  |  |  | I |  |
|  |  |  | 2 |  |
|  |  |  | 3 |  |
|  |  |  | 4 |  |
|  |  |  | 5 |  |
|  |  |  | 6 |  |
|  |  |  | 7 |  |

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TABLE 3 PPI PART ALLOCATIONS (continued)

| PPI | Port | In or Out | Bit | Controls or Reads |
| :---: | :---: | :---: | :---: | :---: |
|  | C | Output | $\begin{aligned} & 0 \\ & \text { I } \\ & 2 \\ & 3 \\ & 4 \\ & 5 \\ & 5 \\ & 6 \\ & 7 \end{aligned}$ | Serial D-A and DISPLAY STROBE LINES <br> CAL D-A LOAD <br> ZERO D-A LOAD <br> RECORDER D-A LOAD <br> DISPLAY DRIVER LOAD <br> POWER REFERENCE ON/OFF <br> REAR PANEL BLANKING OUTPUT <br> LOCAL LOCKOUT TO RESET CONTROL |
| $\begin{gathered} 2 \\ \text { ICI2 } \end{gathered}$ | A | Output | $\begin{aligned} & 0 \\ & 1 \\ & 2 \\ & 3 \\ & 4 \\ & 5 \\ & 5 \\ & 6 \\ & 7 \\ & \hline \end{aligned}$ | 14-BIT D-A LEAST SIGNIFICANT BIT <br> 14-BIT D-A MOST SIGNIFICANT BIT <br> SOURCE I ) CONTROL WHICH OF SIGNAL OR <br> SOURCE 2 ) HEAD ZENER Tp BE MEASURED <br> GAIN CONTROL A <br> GAIN CONTROL B <br> GAIN CONTROL C <br> GAIN CONTROL D <br> GAIN CONTROL E <br> SPACE <br> FILTER CONTROL I <br> FILTER CONTROL 2 |
|  | B | Output | $\begin{aligned} & 0 \\ & \text { I } \\ & 2 \\ & 3 \\ & 4 \\ & 4 \\ & 5 \\ & 6 \\ & 7 \\ & \hline \end{aligned}$ |  |
|  | C | Output | $\begin{aligned} & 0 \\ & \text { I } \\ & 2 \\ & 3 \\ & 4 \\ & 4 \\ & 5 \\ & 6 \\ & 7 \end{aligned}$ |  |

Keyboard and display p.c.b.
70. Refer to Chap. 7, ABOI circuit diagram. Components on this p.c.b. can be split into two distinct parts. These being the key switches and the display drivers.
71. The liquid crystal display (1.c.d.) drivers ICI and IC2, are serial input devices thus they only have 3 control lines but provide up to 32 segment drives from each i.c. The serial data is clocked in by a falling edge on the CLX input line. This data is then loaded to the display drive by a logical high on the LOAD signal line. The two integrated circuits are cascaded so that 3 lines control both ICI and IC2.

GPIB interface module
Circuit diagram: Chap. 7, GPIB p.c.b. circuit diagram
72. This module is an optional item and only fitted to 6960 when remote facilities are required. The module when connected to the rear panel, allows direct connection from a GPIB talker/listener device and implements the full IEEE 488 specifications (no control function).
73. ICI (8291 GPIB talker/listener integrated circuit) is connected to the microprocessor system providing both talker and listener capabilities. IC2ICS transceivers are used to translate the negative true logic and act as drivers. IC6d/IC6c provides the logic low level for the receive instruction T/RI to IC4, pins 7,9; or the talker high level for IC2,IC3,IC4 and also provides the additional buffering necessary for the three lCs in line. Also fitted on the interface module are the GPIB bus terminator loads RI-R6, the address switch SWI, and its buffer IC7.
74. The function of the board is to provide buffering between the general purpose interface bus and the 8291 GPIB handler. The external controller directs the flow of data on the bus and designates when the 6960 is to send data and when it must receive it. The bus uses 16 signal lines to connect all units of a system in parallel. These lines are sub-divided into data, transfer and interface management buses as shown in Fig. 11.


Fig. 11 Interface bus structure
75. Data bus, comprises 8 data input/output lines DO-D7 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.
76. Interface management bus, manages the orderly flow of data across the interface and consists of 5 wires carrying the following signals

Interface clear (IFC); sent by the system controller to clear all device interfaces so that they set to an initial condition.

Remote enable (REN); sent by the controller to enable instruments to be placed under remote control.

Attention (ATN); sent by the controller to indicate that an address or command is on the data lines.

End or identify (EOI); an instrument or controller signal sent to indicate the end of a message.

Service request (SRQ); sent to a controller by an instrument to indicate that it needs service. This can be programmed using the 'SR' program code, details of which are given in the Operating Manual, Vol. I, Chap. 3, SRQ (Service Request) Function.
77. Handshake or data transfer bus, co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are :

Not ready for data (NRFD); asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data, DAV can then be signalled if further data is to be processed.

Data valid (DAV); asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC); asserted by a listener when receiving information from the data lines. Release of the NDAC line tells the data source that new data can be submitted.

## 78. Bus operation

(i) A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition.
(ii) The controller then sets up which instruments are to be listeners by asserting ATN and handshaking the personalized listen address of these instruments over the bus. Similarly the controller designates the talker (only one instrument may talk at a time) by sending its talk address, again with an ATN asserted.
(iii) On removing ATN the talker is then able to place data on the data lines D0 to D7, the transfer of this is controlled by the handshake process and is received by all addressed listeners. The talker typically concludes the sequence by asserting EOl and the controller then resumes control.
(iv) Both the talker and the listeners may be switched by the controller into an inactive state by asserting 1 FC or sending OTA (other talk address) and UNL (un1isten) on the data bus.
79. Handshake procedure, the handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. A typical handshake is as follows:
(i) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.
(ii) When all listeners are ready to receive data NRFD is removed with NDAC at this time asserted.
(iii) After a delay to allow the data bus to settle, talker asserts DAV to show data is valid and may be accepted.
(iv) Data byte is transferred, then listeners assert NRFD. When all the listeners have accepted the byte NDAC is removed to signify receipt.
(v) Talker removes DAV, listeners assert NDAC, and the bus reverts to its initial condition ready for the next data byte, a typical cycle is shown below in Fig. 12.


Fig. 12 Handshake procedure

## Software description

80. On power-up the processor sets up a stack pointer at the highest working location in RAM, initializes the 8255 PPIs; the display is then set to read '6960' whilst a simple test is made on all RAM locations. The TRAP interrupt is enabled at this point. A checksum byte stored on power-down is checked to ensure data retention. The D-As are then set as the data requires. The program issue is then displayed in the form 'I 5 n ' for $1 / 2$ second. At this point, if any key is pressed the program jumps to the calaid routines. The 8291A GPIB chip is initialized and the GPIB address is displayed if the chip is present.
81. The main program loop operates as follows:- If it is the first measurement; the range switches are set; the range offset is looked up; the range limits are looked up; the settling time is calculated from the average number; the averaging sample number is set to zero; a single A-D conversion is carried out and stored as the previous average; the measurement counter is reset; if settling time is enabled the status byte in the GPIB output string is set to an'S'; and the number of conversions required on the inside averaging loop is looked up if in the fast operating mode (GPIB only) else the default value of 400 is used.
82. The inside averaging loop checks to see if any key has been pressed. If so, the program jumps to the keyboard routines. An A-D conversion then takes place and is averaged with the previously stored data. The loop is repeated until the required number of conversions has taken place.
83. The head Zener is then measured by performing an A-D conversion with the switches set to read the diode. The data from the conversion is then used to work out which Zener diode is in use. Data regarding linearity correction and sensitivity are saved.
84. The measured power data is then compared with the range limits stored previously. The program jumps to the range error routine if the limits are exceeded and an SRQ is raised if necessary.
85. The data is then converted into the binary floating point format required by the MATHS package. The range offset is added at the same time.
86. If the filter is in (Range I) the data is corrected for the gain error of the filter.
87. The out side average (the one selectable from the front panel) is then performed.
88. A check on the sign of the data is carried out and if -ve and the dB mode is selected, UNDERRANGE is flagged and the program jumps to the range error routine.
89. The data is then range corrected so that the top reading on the centre range is 1.000 .
90. Diode or thermocouple linearity correction is then applied as required.
91. CAL FACTOR correction is then applied.
92. The RECORDER OUTPUT D-A is then set as required to the following rules:If in linear mode ( W ), output is a V to +S V for each range. If in dB mode, output is +S V for the top of range 3 with a gain of $1.0 \mathrm{v} / \mathrm{la} \mathrm{dB}$.
93. Duty cycle correction is then applied.
94. The resultant data is then turned to mW dependent on the sensitivity of the sensor as indicated by the HEDTYP.
95. The data is then turned to dBm and any dBrel offset added as required.
96. The attenuation offset is then applied if required.
97. The final routine in the MAIN loop basi.cally drives the display and GPIB output. It can be split into various parts:
(I) Round the data according to the amount of averaging that is being applied. This is range dependent in the dB mode.
(2) The settling time is checked if enabled. If the settling time has been reached a flag is set to indicate this.
(3) The measurement result is loaded into the GPIB output buffer and also displayed.
98. If in the GPIB talk only mode the GPIB output buffer is output to the GPIB.
99. An SRQ is raised if SRQ on end of measurement was required.
100. If not in the HOLD mode (GPIB only), the program jumps back to the start of the main loop.
101. If in the HOLD mode, a check is made to see if local lockout is set; if not the program runs round a loop checking for the LOCAL key else it halts the processor.

## Chapter 5

## MAINTENANCE

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## INTRODUCTION

1. This chapter contains information for keeping the equipment in good working order, checking overall performance, fault finding and re-alignment procedures. Before attempting any maintenance on the equipment you are advised to read the preceding chapter containing the technical description.
2. In the case of difficulties which cannot be resolved with the aid of this book, please contact your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.
3. When making tests to verify the instrument meets the stated performance limits, allowances must be made for the uncertainty of the test equipment used.
4. Integrated circuits and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reverse polarity and excessive heat or radiation and the use of insulation testers.

## Static sensitive devices

5. The CMOS integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge.

## Fault location

6. Some aid to fault finding is provided by the typical d.c. voltage and signal levels. Tables given are not extensive but are intended as a pointer to further investigation. It is emphasized that each fault table should be studied having regard for the others, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

## DC voltages

7. Voltages given approximate those which can be expected using a $20 \mathrm{k} \Omega / \mathrm{V}$ meter on a typical 6960 connected to an a.c. supply of 220 to $240 \mathrm{~V}, 50 \mathrm{~Hz}$.

Board layout and preset components
8. Printed circuit board layouts can be seen in Chap. 7, Servicing Diagrams. Preset and select-in-calibration (SIC) components are also identified there. A further plan view of the presets and their function can be seen in this chapter.

## ACCESS AND LAYOUT

Layout, top view (see Fig. 1)
9. To remove top and bottom outer covers simply unscrew the two retaining screws in the rear panel feet; remove the feet and the diecast surround, then slide each cover to the rear and lift off.
10. To remove the processor p.c.b., AAO2/l, first unscrew the six self-tapping screws holding the $p, c, b$. to the side frames. Carefully disconnect the three multiway connectors from the p.c.b. Do not place the p.c.b. assembly on a metallic surface or the battery may be damaged.


Fig. 1 : Layout, with AAO2/1 disconnected

## Dismantling front panel assembly

11. Disconnect all sockets that connect the front panel assembly to the rest of the instrument. Remove the four screws holding the side panels to the front panel assembly. The front panel assembly can now be pulled forward and partially removed. The supply switch and its cover must either be disconnected or removed before the front panel can be completely removed. When replacing the front panel assembly as a unit, disconnect the wires from the supply switch at the rear panel fuses and voltage change-over switch.
12. The p.c.b. can now be removed by removing the six screws holding it to the front panel metal work.
13. On re-assembly ensure that all of the push-buttons operate freely and that the display is centred in its surround.

## Dismantling rear panel assembly

14. Disconnect the two cables that join the rear panel assembly to the analogue p.c.b. Unsolder the wires from the supply switch at the fuses and voltage change-over switch. Remove the two screws at the ends of the GPIB assembly support plate and lift out the GPIB assembly. The rear panel assembly can now be pulled away after removing 6 screws ( 4 in one side and 2 in the other).

## Access to power reference p.c.b.

15. The power reference assembly must first be removed from the instrument.

Remove the two screws holding the mounting plate to the side panel. The four self tapping screws holding the screening can now be removed. When the plate has been removed and the connector pulled off, the p.c.b. may be withdrawn from the box.

## PERFORMANCE AND INTERNAL SIGNAL TESTS

## Switch-on calibration checks

16. Performing the calibration procedure at switch-on demonstrates that the instrument's measuring circuits are functioning.

Switch-on: At switch-on the $6960^{\circ}$ s LCD should first display "6960" followed by the software issue number e.g. "IS 7" and then the GPIB address (if GPIB is fitted). If no sensor is connected the LCD will then display the error code
"Er 2". Otherwise the instrument should, with no r.f. power applied to the sensor, display either a very low power reading or five dashes and the "under range" annunciator.

Autozeroing: Press [AUTO ZERO]. This should cause the LCD to display the five dashes and the "zero" annunciator. As each of the 6960"s five ranges is zeroed, one of the dashes is blanked. When all dashes have been blanked, all ranges are zeroed. After zeroing, the instrument returns to the range previously set, or (if no range was set), to auto- range. With no r.f. power applied, a low power reading or the five dashes and "under range" annunciator, are again displayed.

Autocalibration: Press [LINEARITY FACTOR] and from the bar chart on the sensor labelled LIN F, enter the linearity factor. Press [CAL FACTOR] and enter the 50 MHz reference calibration factor given on the sensor. (For 6910 and 6913 sensors the default figure of 100 applies and no entry is required).

Connecting a 6910 series sensor to the power reference and pressing [AUTO CAL] causes the sensor to be calibrated to the $0 \mathrm{dBm}, 50 \mathrm{MHz}$ power reference signal. When autocalibration is completed the reference is switched off (if not previously selected), but if switched on again by pressing [POWER REF] the display should read 0 dBm or 1.00 mW if autocalibration has been successful.

6920 series sensors are calibrated to -30 dBm , and the 0 dBm reference signal should be applied to these sensors via the supplied calibrated 30 dB attenuator.

## Performance specifications

17. The performance specifications listed in Table 1 below are reproduced from the SPECIFICATION section in the Operating Manual (Chapter 1, Page 4).
18. The specifications designated TYPE are implicit in the design of the 6960 and are therefore not tested for in the production of the instrument.
19. The specifications designated PRODUCTION are tested for and/or set by adjustment in production. Those PRODUCTION specifications which are also designated (TEST) have their production tests reproduced in the Performance Tests sub-section. Those which are also designated (ADJUSTMENT) are set by adjustments described in the ADJUSTMENT AND CALIBRATION section. (Note that the performance is adjusted to well within the specification).
20. 

Table 1 : Performance specifications


Continued overleaf.
Chap. 5

Table 1 : Performance specifications (continued)

| SPECIFICATION | DESIGNATION |
| :--- | :--- |
| Response time |  |
| Range 1 : 1 s selectable | TYPE |
| Ranges 2 to $5: 25$ ms using GPIB and |  |
| trigger modes. 250 ms (display update) |  |
| selectable. |  |

## Performance Tests

(COVERS ON)

## Introduction

21. These tests check the three specifications routinely tested in production which are not directly adjustable by the user: namely zero set, zero carryover, and instrumentation accuracy. There is a single test combining the zero set and zero carryover specifications.
22. The specifications tested apply to the 6960 only, but in order to test them a Marconi Instruments 6910 or 6920 series RF sensor must be connected to the instrument. Results for both 6910 series and 6920 series sensors are given. It is preferred that a 6910 series detector is used to minimize any, possibility of inaccuracies due to drift. If a 6920 series sensor is used, excessive handling and violent temperature changes should be avoided.
23. The format for the tests is:

> Specification
> Test equipment
> Test arrangement
> Procedure
> Table of results
24. Where a test instrument type number is preceded by "MI", this is a Marconi Instruments product.
25.

Zero set/carryover
SPECIFICATION

```
Zero set error : +/- 1% of full scale of range 1.
Zero carryover : +/- 0.03% of full scale of operative range (when
                zeroed on most sensitive range).
```

Test equipment
None required
Test arrangement
6960
POWER METER


RF Sensor $6910 / 6920$

Series
Fig. 2 : Arrangement for zero set/zero carryover test

## Procedure

(1) Press [AUTOZERO] and wait until complete.
(2) Set [AVERAGE] to 50, [UNITS] to Watts.
(3) Set [RANGE] to 1.
(4) Wait 15 s for averaging to be completed.
(5) Note zero error reading in the results table, below.
(6) Repeat (3), (4) and (5) for ranges 2 to 5.
(7) Check that zero set/carryover error does not exceed specified limits.

Results

| Range | 6910 series sensors |  |  | 6920 series sensors |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | F.S.D. | Error limits | Reading | F.S.D. | Error 11mits | Reading |
| 1 | $10 \mu \mathrm{~W}$ | $+/-0.10 \mu \mathrm{~W}$ | 00 | 0.010 nW | +/-0.010 nW |  |
| 2 | $100 \mu \mathrm{~W}$ | $+/-0.13 \mu \mathrm{~W}$ |  | 0.013 nW | +/-0.013 nW |  |
| 3 | 1 mW | +/- 0.4 uW |  | 0.04 nW | +/-0.04 nW |  |
| 4 | 10 mW | +/-3.1 1 W |  | 0.31 nW | +/-0.31 nW |  |
| 5 | 100 mW | +/-30.1 $\mu \mathrm{W}$ |  | 3.01 nW | +/-3.01 nW |  |

26. 

Instrumentation accuracy

| SPECIFICATION |  |
| :---: | :---: |
| Maximum instrumentation error | Watts mode : $+/-0.5 \%$ <br> dBm mode $:+/-0.02 \mathrm{~dB}$ <br> dB REL mode : $+/-0.02 \mathrm{~dB}$ |


|  | TEST EQUIPMENT |  |
| :--- | :--- | :--- |
| Description | Minimum specification | Example(s) |
| Signal generator | Power accuracy: $+/-1 \mathrm{~dB}$ | MI 2022 |
|  | (at 50 MHz$)$ | MI 2018A |
|  |  | MI 2019A |

## Test arrangement



TPA 5469
Fig. 3 : Arrangement for instrumentation accuracy test
Procedure (For power reading in Watts mode)
(1) Set signal generator RF level to 0 dBm ( -30 dBm for 6920 series), carrier frequency to 50 MHz .
(2) Use signal generator $R F$ on/off control to switch output off.
(3) Press [CAL FACTOR] on 6960 and enter REFERENCE CAL FACTOR (given on all sensors except the 6910 and 6913). For the 6910 and 6913 , the default CAL FACTOR of 100 is the correct value, and no entry is normally required.
(4) Press [AUTOZERO] and wait until complete.
(5) Switch signal generator RF output on.
(6) Press [LIN'FACTOR] and enter appropriate linearity factor for the sensor being used.
(7) Press [AUTOCAL] and wait until complete. This is indicated by 0 dBm (6910) or -30 dBm (6920) being displayed on the 6960 .

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Page 8
(8) Set [UNITS] to Watts, [AVERAGE] to 50.
(9) Set RF level on signal generator to -20 dBm (6910) or -60 dBm (6920).
(10) Set [RANGE] to 1.
(11) Wait 15 s for averaging to be completed.
(12) Note reading, Pa, in the results table below.
(13) Set [RANGE] to 2.
(14) Wait 15 s .
(15) Note reading, Pb , in the results table below.
(16) Percentage instrumentation error $=(\mathrm{Pb} / \mathrm{Pa}-1) \times 100 \%$
(17) Repeat (9) to (16) with the power and range settings shown in the results table.

## Results

| $\begin{gathered} \text { Initial/Final } \\ \text { range } \end{gathered}$ | Generator power setting |  | $\begin{gathered} \mathrm{Pa} \\ \text { (Watts) } \end{gathered}$ | $\begin{gathered} \mathrm{Pb} \\ \text { (Watts) } \end{gathered}$ | $\begin{gathered} \% \\ \text { error } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { Error } \\ & \text { limit } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1/2 | -20 dBm | -60 dBm |  | $\because$, $\because$ | $\because$ | NOTE (i) |
| 2/3 | $-10 \mathrm{dBm}$ | $-50 \mathrm{dBm}$ | $0 \pi$ |  | $\cdots$ | $\pm 0.5 \%$ |
| 3/4 | 0 dBm | -40 dBm | ¢0. ${ }^{\text {a }}$ |  | - | 0.5\% |
| 4/5 | $+10 \mathrm{dBm}$ | $-30 \mathrm{dBm}$ |  |  | ) | 0.5\% |

## NOTES:

(i) At low powers the range error is dominated by noise and zero set (each contributing a possible $+/-1 \%$ ). To accurately measure the range error for ranges 1 and 2 the zero set values for both ranges should be deducted. This, however, is time consuming and susceptible to errors. It is therefore suggested that the instrumentation error for range $1 / 2$ should be tested to $5 \%$ only, as a functional check.
(ii) A similar test can be performed to check the instrument accuracy in the dBm and dB REL modes. In this case the instrumentation error would be given by Pb - $\mathrm{Pa}(\mathrm{dB})$. The specified maximum error in the dB modes is 0.02 dB (but for ranges $1 / 2$, test for 0.2 dB only).

## Internal signal tests (TEST mode) (COVERS OFF)

27. To facilitate fault finding, the 6960 has a "TEST" mode which allows the outputs of the $D-A$ converters and the filter, and the functioning of the display and keyboard to be checked. To enter into TEST mode press RESET and any other key simultaneously. Keep the keys pressed until "tESt" appears on the display, then release. Table 2 shows the tests available. To select the required test, press the appropriate key. To exit from a test (and from TES'T mode) press RESET.

Table 2 : TEST mode functions

| Key | Test | Display | Test point |
| :---: | :---: | :---: | :---: |
| 0 | Display test and filter enable | All displays flash | TP6 wrt TP7 |
| 1 | Recorder D-A to 0.000 volts | - - - - | Recorder 0/P |
| 2 | Recorder D-A to 5.000 volts | - - - - | Recorder 0/P |
| 3 | Recorder D-A to 9.99756 volts | - - - - | Recorder 0/P |
| 4 | 14-bit D-A to Vref (voltage at TP8) | - - - - | TP10 wrt TP7 |
|  | 14-bit D-A to zero volts | - - - - | TP10 wrt TP7 |
| 6 | 14-bit D-A to -Vref x (8191/8192) volts | - - - - | TP10 wrt TP7 |
| 7 | Zero D-A to zero (no bits set) | - - - - | TP12 wrt TPI |
| 8 | Zero D-A to centre (MSB only set) | - - - - | TPl2 wrt TPl |
| 9 | Zero D-A to top (all bits set) | - - - - | TP12 wrt TPl |
| - | Auto-cal (gain) D-A to zero | - - - - - | TP13 wrt TPl |
| ENT | Auto-cal (gain) D-A to top | - - - - | TPl3 wrt TPl |
| - | Keyboard test | Display appropriate to key pressed | - |

## NOTES:

(1) The locations of the test points on AAOl board (together with the preset potentiometers used for adjustments), are shown in Fig. 4, below.
(2) Tests "0" to "6" and "-" give results which are fixed for all 6960"s. The other tests are dependent upon individual D-A characteristics and do not yield fixed numerical values. These tests are included as servicing aids.
(3) The expected filter waveform of test " 0 ", and the adjustment procedures required should any of tests "0" to "6" fail, are described in the ADJUSTMENT AND CALIBRATION SECTION
(4) "wrt" means "with respect to".
(5) IMPORTANT: Do not ground (earth) any test pins.
28.


## Test points

```
TP1 Analog ground
TP2 Master oscillator
TP3 Spike blanking pulse
TP4 Sample pulse
TP5 Timing control earth
TP6 Detector output
TP7 Chassis earth
```

Preset potentiometers

R16 Master oscillator frequency
R55 Spike blanking width
R56 Time to sample pulse
R57 Sample pulse width
R70 14-bit D-A gain
R72 14-bit D-A offset A

TP8 -6.2V reference
TP9 14-bit D-A set-up
TP10 14-bit D-A output
TP11 Time to sample pulse
TP12 Zero D-A output
TP13 Filter input

Fig. 4 : Locations of test points and preset potentiometers on AAOl

## ADJUSTMENT AND CALIBRATION

29. In this section measurements and adjustments for maintaining the 6960 at its optimum operating condition are described. Table 3 lists the test equipment required.

Table 3 : Test equipment for adjustment and calibration.

| Description | Minimum specification | Example |
| :---: | :---: | :---: |
| a Multimeter | Greater than $20 \mathrm{k} \Omega / \mathrm{V}$ | GEC Selectest |
| b Digital voltmeter | $\begin{aligned} & \text { DC volts : } 0.1 \text { to } 10 \mathrm{~V} \\ & \text { Accuracy } 0.001 \% \end{aligned}$ | Datron 1065 |
| c Counter/timer | Time: $1 \mu \mathrm{~s}$ to 1 ms Frequency: 50 MHz | MI 2437 |
| d RF sensor | MI 6910 sensor with calibration certificate | MI 6910 |
| e $50 \mathrm{MHz}, 1 \mathrm{~mW}$ power reference | Current calibration certificate | Available in MI 6960 or 6950 |
| f 50 MHz rejection filter | Better than 35 dB rejection at 50 MHz . Absorptive at 50 MHz | Specification TE 1031/817 available from MI |
| $g$ Spectrum analyzer | Coverage to greater than 300 MHz | MI 2382 |
| h Oscilloscope | $\begin{aligned} & \text { Bandwidth : } 2 \mathrm{MHz} \\ & \text { Volts/div. : } 10 \mu \mathrm{~V} \text { to } 5 \mathrm{~V} \end{aligned}$ | Tektronix 5110 with plug-ins 5B40 and 5A22N |
| i Oscilloscope probe | Differential type | Tektronix P6055 |
| j Oscilloscope | ```Bandwidth : 70 MHz Volts/div. : 1 V to 5 V``` | Tektronix 2445 |
| k Oscilloscope probe | To suit above scope | Tektronix P6131 |
| 1 Filter test jig | Special. | Specification TE 1031/816 available from MI |

## Voltage checks and adjustments

Test equipment : items b, Digital voltmeter

$$
h, i \text { Oscilloscope and probe }
$$

30. $210 \mathrm{~V}-250 \mathrm{~V}$ range setting. Ensure that the mains supply input voltage selector on the rear panel is set for the above range and that the correct fuses are fitted in FSl and FS2 ( 250 mA , time delay). Connect the 6960 to a mains supply of 230 V a.c.

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Page 12
(1) Switch on a.c. supply.
(2) -19 V supply. Locate D 32 on AAO , the main p.c.b. Measure the voltage between D32 anode and chassis using the digital voltmeter, (-ve to chassis). Adjust R 88 for a reading of -18.9 V to -19.1 V .
(3) Move the digital voltmeter (d.v.m.) positive lead to D35 cathode and check that the voltage lies between +20 V and +21 V .
(4) +5 V supply. Transfer the d.v.m. positive lead to PL6 pin 6. Adjust R97 for +4.95 V to 5.05 V . Remove the d.v.m.
(5) Ripple voltages. Check the ripple voltages on the plus and minus 15 V supply rails and the +5 V rail with respect to the chassis. ( +15 V at D35 anode, -15 V at D32 cathode and +5 V at PL6 pin 6). The ripple should be less than $100 \mathrm{mV} \mathrm{pk}-\mathrm{pk}$ on the +5 V rail and less than 20 mV pk-pk on the other two rails. Use the differential scope probe without connecting the oscilloscope earth to the 6960.
31. 105 V to 120 V range setting. Ensure that the mains supply input voltage selector on the rear panelis set to the above range and that the correct fuses are fitted in FSi and FS2 ( 500 mA , time delay). Connect the 6960 to a 115 V a.c. supply then carry out the checks detailed in the previous paragraph.

## Timing adjustments

Test equipment : item $c$, Counter timer
32. Set the counter timer to read time between positive-going edges. Connect the timer input between TP5 (ground) and TP2 (signal). Adjust R16 for a reading of $540 \mu \mathrm{~s} \pm 0.5 \mu \mathrm{~s}$.
33. Set the counter timer to measure between a positive-going transition and a negative-going transition. Connect to TP3. Adjust R55 for $180 \mu \mathrm{~s} \pm 5 \mu \mathrm{~s}$.
34. Connect the counter timer to TPll and adjust R56 for $400 \mu \mathrm{~s} \pm 10 \mu \mathrm{~s}$.
35. Connect the counter timer to $T P 4$ and adjust $R 57$ for $6.0 \mu s \pm 0.5 \mu s$.

## Filter balance adjustment (TEST mode 0)

Test equipment : item 1 , Filter test jig h,i, Oscilloscope and probe
36. This adjustment should not need to be carried out unless AA01 C49, C50 or R115 has been replaced.
37. Connect the special filter test jig as shown on the box. Connect the oscilloscope, a.c. coupled, to TP6 and chassis. Set the sensitivity to $1 \mathrm{mV} / \mathrm{div}$. and time base to $0.5 \mathrm{~ms} / \mathrm{div}$. Remove the link from PL7. Enter the 'TES'T' mode, see para. 27.
38. Adjust Rll5 for the waveform shown in Fig. 3.


The two "pedestals" (arrowed) should not differ in voltage by more than 1 mV

Fig. 5 : Filter adjustment

Remove the test jig and oscilloscope. Replace the link on PL7.

## 14-Bit D-A adjustment (TEST mode 5)

Test equipment : item b, digital voltmeter (d.v.m.)
39. Enter the "TEST' mode, see para. 27. Connect the d.v.m. negative to TP7 and the positive to TP9. Link together TP7 and TP8.
40. Select test $-5^{-}$and adjust $R 72$ for a d.v.m. reading of $0 \pm 3 \mu \mathrm{~V}$.
41. Connect the d.v.m. positive to TP10 and adjust R76 for $0 \pm 5 \mu \mathrm{~V}$.
42. Remove the link from TP8 and adjust R70 for $0 \pm 10 \mu \mathrm{~V}$.
43. Remove the d.v.m.

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## Recorder D-A adjustment (TEST mode 1)

Test equipment : item $b$, digital voltmeter
44. Enter the "TEST" mode. Select test " 1 . Connect the d.v.m. to the recorder output on the rear panel.
45. Adjust R82 for $0 \pm 10 \mu \mathrm{~V}$.
46. Select Test ${ }^{-2-}$ and adjust R81 for $5 \mathrm{~V} \pm 100 \mu \mathrm{~V}$.


Fig. 6 : AC04, Power reference calibration components

## Power reference adjustment

Test equipment : item b, Digital voltmeter
c, Counter timer
d, Sensor 6910
e, $50 \mathrm{MHz}, 1 \mathrm{~mW}$ power reference
f, High-pass filter
g, Spectrum analyzer
47. Before setting the power reference output level the 6960 should be powered up for at least 15 minutes. The power reference used as a standard should have calibration to a national standard. The tests should be carried out in the correct order. Components referred to are on the power reference assembly.
48. Frequency. Connect the counter timer, set to read frequency, to the power reference output. Adjust the frequency, using Ll, to $50 \mathrm{MHz} \pm 50 \mathrm{kHz}$. Remove the counter timer.
49. Output level (initial setting). Set the 6960 to read "Watts ${ }^{\circ}$. Zero the 6910 Sensor. With the sensor reading the power of the 1 mW power reference standard press 'AUTO CAL'. When the calibration is finished transfer the sensor to the 6960 POWER REFERENCE output and adjust AA05 R15 for 1.000 mW .
50. Harmonics. Harmonic adjustment should not be carried out unless components on the power reference p.c.b. have been changed.
51. Connect the power reference output to the spectrum analyzer via the high-pass filter. Set the analyzer to 175 MHz centre frequency, 20 MHz per division and 0 dBm reference level. Reduce the viewed harmonics to a minimum using Cll. No harmonic should be greater than -55 dBm in level. The high-pass filter is used so that the level of 50 MHz signal applied to the mixer in the spectrum analyzer is such that no harmonics are produced by the mixer.
52. Output level (final setting). Repeat "Output level (initial setting)". Ensure that the 6910 Sensor is zeroed correctly before applying any power.

## FAULT LOCATION

53. The following section consists of a fault finding table and other checks to aid fault location. To assist fault finding it is advisable to study the technical description in Chap. 4. Note that for AUTO ZERO and AUTO CAL faults the sensor should be tried first as this is the most likely cause.
54. If no other sensor is available, the following tests may be carried out to decide whether the sensor is faulty:-
(i) Enter the TEST mode (see para. 27). Connect a voltmeter to the LEVELLING output on the rear panel. Without the sensor being connected to the power reference output, press the decimal point key followed by the " 7 " key. The voltage from the levelling output should be between -250 mV and -550 mV for a 6910 series sensor (for a 6920 series sensor, note the voltage). Press the " 9 " key and check that the voltage is +250 mV to +550 mV for a 6910 series sensor (note the voltage for 6920 series). For a 6920 series sensor, add the two voltages obtained, ignoring the minus sign of the second. The result should be less than 1400 mV . Press the " 8 " key. The voltage should be less than $+/-50 \mathrm{mV}$ for 6910 series sensors, less than $+/-200 \mathrm{mV}$ for 6920 series.
(ii) Connect the sensor to the power reference (directly for 6910 series, via a 40 dB attenuator for 6920 series). Check that the voltage is greater than 1.2 V (either type).
(iii) If any of the above voltages are not obtained, the sensor or its cable is likely to be faulty.
55. When disconnecting the Conhex connector from the power reference assembly ensure that the metal clad connector cannot accidentally cause short circuits on the printed boards and create additional faults.
56. The checks given in this chapter are not exhaustive but are intended as a pointer to further investigation. It is emphasized that each fault should be studied having regard for other fault finding information, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

## Power supply faults

57. Symptoms of power supply faults are often confusing therefore it is recommended that the supplies are checked before commencing any other tests. See "Voltage checks and adjustments", above.
58. If the l.e.d. in the +5 V power supply regulator is lit this indicates that the overcurrent circuit has tripped the supply. This may be caused by excessive current being drawn by the processor p.c.b. AA02/1 or the over-voltage s.c.r. firing. To decide in which area the problem lies disconnect the processor p.c.b. and turn on. N.B. The supply to the +5 V regulator must completely disappear before the trip will reset so allow at least 15 seconds before turning on again.

## Signal channel faults

59. Before working on a possible signal channel fault it is best if a known good sensor is tried, as failure to AUTO ZERO or AUTOCAL are more likely to be due to the sensor. Various typical waveforms are shown in Fig. 7.
60. Listed below are some possible signal channel problems.
(1) Fault symptom : Sensor will not zero.

Possible faults : Sensor cable faulty, ZERO D-A faulty or loss of one chopper drive

Check : Cable by substitution. Voltage from Zero D-A goes positive and negative (use TEST mode). Outputs from chopper drivers.
(2) Fault symptom : Failure to AUTO CAL.

Possible faults : Incorrect sample timing. GAIN D-A failed. 14-bit D-A failed.

Check : All timing adjustments as per paras. 32-35. Gain $D-A$ changes the output of the fourth amplifier (ICllb, pin 7) by a factor of 3 when using TEST modes -.- (decimal point) and "ENT". 14-bit D-A set-up as per paras. 39-43.
(3) Fault symptom : No signal channel gain.

Possible fault : Faulty amplifier stage.
Check : Outputs of each amplifier stage are approximately equal to those shown in Fig. 7.
(4) Fault symptom : Noisy readings on range 1 .

Possible fault : (i) Filter not adjusted correctly.
(ii) Inadequate AVERAGE number with 6920 sensor.

Check : (i) Filter alignment as per paras. 36-38.
(ii) Increase AVERAGE number.

LC1 pin 6
Output first amplifier




Vertical $20 \mathrm{mV} / \mathrm{div}$. Horizontal $0.2 \mathrm{~ms} / \mathrm{div}^{2}$

Vertical $20 \mathrm{mV} / \mathrm{div}$ Horizontal $0.2 \mathrm{~ms} / \mathrm{div}^{2}$

Vertical 0.2 V/div. Horizontal $0.2 \mathrm{~ms} / \mathrm{div}^{2}$

IC11b pin 7 output fourth amplifier (TP13)

IC4b pin 7 Output spike blanking buffer

IC4a pin 1 output second amplifier

LClla pin 1 output third amplifier

Vertical $0.5 \mathrm{~V} / \mathrm{div}$. Horizontal $0.2 \mathrm{~ms} / \mathrm{div}$.

Vertical $0.2 \mathrm{~V} / \mathrm{div}$. Horizontal $0.2 \mathrm{~ms} / \mathrm{div}$.

N.B All waveforms taken with 6910 Sensor connected to 0 dBm and
6960 on range 3 .

Fig. 7 : Signal channel waveforms
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## Processor board faults

61. Two possible processor p.c.b. faults are indicated on power-up. If
-Er $1^{-}$is displayed on power-up or RESET this indicates that achecksum test on the non-volatile RAM contents has failed. This could be caused by an exhausted battery (B1). The battery voltage should be above 2.0 V to guarantee memory retention.
62. A flashing display on power-up or RESET indicates total failure of the RAM. The signals driving the RAM, IC9, should be checked before changing it.
63. Other processor board faults can show themselves in many different ways. If a fault is suspected on the board and another board (which is known to be working) is available, this should be tried before fault-finding the failing board.

## Chapter 6

## REPLACEABLE PARTS

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```
Para.
    Introduction
    Abbreviations
    Component values
    Ordering
Components
        AAO - RF power meter with GPIB
        AAO1 - Analogue p.c.b. assembly
        AA02/1-Processor p.c.b. assembly
        AA03 - Front panel assembly
        AA04 - Rear panel assembly
        AA06 - Ribbon cable 50-way
        AA07 - Ribbon cable 26-way
        AA10 - Power link socket
        AAll - GPIB interface module
        ABO1 - Keyboard and display assembly
        AB04 - Cable assembly 6-way
        ABO5 - Cable assembly 2-way
        AB06 - GPIB p.c.b. assembly
        AB07 - Switch p.c.b. assembly
        AB08 - Cable assembly
        AC03 - Power ref. cable assembly
        AC04 - Power reference assembly
        AF03 - Sensor input assembly
        AF04 - RF cable assembly
        AF08 - Sensor cable assembly
    Mechanical parts
```

Fig. Page
1 Miscellaneous mechanical parts ... ... ... ... ... 19/20

## INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. AAO1, ACO2 etc.
2. The complete component reference includes its reference designator as a prefix e.g. AAO1 Cl (capacitor C1 on printed circuit board AAO1) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However, when ordering replacements or in correspondence the complete component reference must be quoted.

## ABBREVIATIONS

3. Electrical components are 1 isted in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used :

| ADC | analogue-digital converter |
| :---: | :---: |
| AX | axial |
| CAP | capacitor |
| CARR | carrier |
| CARB | carbon |
| CC | carbon composition |
| CDE CNV | code converter |
| CER | ceramic |
| CERM | cermet |
| CF | carbon film |
| COAX | coaxial |
| CON | connector |
| CTR | counter |
| DAC | digital-analogue converter |
| DEC/DMX | decoder/demultiplexer |
| DECOD | decoder |
| DIL | dual in-1ine |
| DIV | divider |
| DRIV | driver |
| ELEC | electrolytic |
| ENCOD | encoder |
| FEM | female |
| FF | flip-flop (bistable) |
| FILTERCON | filtering capacitor |
| GER | germanium |
| GP | general purpose |
| ICA | integrated circuit, analogue |
| ICD | integrated circuit, digital |
| IND | inductor |
| INV | inverter |
| LD/T | 1ead through |
| MF | metal film |
| MG | metal glaze |
| MISC | miscellaneous |
| MO | metal oxide |
| MP | microprocessor |
| MP SUPP | microprocessor support |
| MUX | multiplexer |
| NET | network |
| PC | polycarbonate |
| PETP | (polyester) polyethelene terephthalate |
| PS | polystyrene |
| PLL | phase-locked loop |


| Q/ACT | quick acting |
| :---: | :---: |
| RECT | rectifier |
| RES | resistor |
| RV | resistor, variable |
| RX | receiver |
| SAPPH | sapphire |
| SEC | secondary |
| SCHM | Schmitt |
| SH REG | shift register |
| SIL | silicon |
| SW | switch |
| T/LAG | time lag |
| TANT | tantalum |
| TOG | toggle |
| TRANS | transistor |
| TX | transmitter |
| VAR | variable |
| VREG | voltage regulator |
| W | watts at $70^{\circ} \mathrm{C}$ |
| WW | wirewound |
| X | miscellaneous item |
| XL | crystal |
| ! | static sensitive component |
| \% + | asymmetric tolerance |
| $\neq$ | programmed EPROM |

## COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons :
(a) Components indicated by an * have their values selected during test to achieve particular performance limits.
(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.
(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.
5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment. While equivalent alternatives to some components may be included during manufacture, Marconi Instruments Ltd., Microwave Products Division, should be consulted before any other alternatives are fitted when the equipment is being serviced.

## ORDERING

6. When ordering replacements, address the order to our Technical Services Department (address on rear cover) or nearest agent and specify the following for each component required:-
(1) Type $\neq$ and serial number of equipment.
(2) Complete circuit reference.
(3) Description.
(4) Part number

As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number. Or contact your local Marconi Instruments, Microwave Products Division representative.
$\neq$ To order a replacement programmed EPROM, specify the serial number of the instrument, and the part number of the IC required. Also specify the EPROM version number, this is identified on the IC following the part number.
H 6960
Vol. 2
Part no.

 $U$
0
0
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1
1
0
0
0
0
0

0 | 4 |
| :--- |
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| 0 |
| 0 |
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| 1 |
| 1 |
| 0 |
| 0 |
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| 0 |
| 0 | さ60Z-98792





$\begin{array}{ll}0 & \\ 0 & 1 \\ 0 & 0 \\ 0 & 1 \\ 1 & 1 \\ m & 0 \\ 0 & \infty \\ 0 & 0 \\ 0 & 0 \\ N & 0\end{array}$ 26383-006C | M |
| :--- |
| 0 |
| 0 |
| 0 |
|  |


26486-209F 26538-770T
Chap. 6
Page 5
Circuit
ref.
COMPONENTS
7. Unit AAO - RF POWER METER WITH GPIB
$\begin{array}{llll}\text { FS1 } & \text { FUSE T/LAG } & 0.25 A & 20 \times 5 \\ \text { FS2 } & \text { FUSE }\end{array}$

37590-211G

CAP CER 10N 25V 20\% DISC
CAP TANT 1U0 35 V 20\% BEAD CAP CER 10N 25V 20\% DISC CAP TANT 1U0 35V 20\% BEAD
CAP CER 10N 25V 20\% DISC CAP TANT 1 U0 35v 20\% BEAD CAP PETP 220N 63V 10\% RAD
CAP CER 10 N 25V 20\% DISC
CAP TANT 1U0 35V 20\% BEAD
CAP PS 10NO 63V 2\% RAD CAP CER 100P 63V 2\% PLATE Circuit
ref. 8080 CAP TANT 100 35V 20\% BEAD CAP CER 10N 25V 20\% DISC CAP CER 10N 25v 20\% DISC CAP TANT 1UO 35v 20\% BEAD CAP CER 47N 25V 20\% DISC CAP CER 47 N 25 V 20\% DISC CAP PETP 220 N 63V 10\% RAD
CAP CER 1NO $100 \mathrm{~V} 5 \%$ CAP CER 1ON 25V 20\% DISC机 Description

$\because \stackrel{m}{u} \vec{u} \mathbb{J}_{u}^{u}$

 $\stackrel{N}{U}^{N}{ }_{U}^{\infty}$

$2 \cdot 10 \Lambda$
0969 н


| Circuit ref． |  | Description | Port no． |
| :---: | :---: | :---: | :---: |
| C80 | CAP | CER 10N 25v 20\％DISC | 26383－006C |
| C81 | CAP | CER 10N 50V 20\％X7R MON AX | 26346－120Y |
| C82 | CAP | ELEC 4700U 40v 10\％＋PCB | 26422－321W |
| C83 | CAP | CER 1NO 63V 10\％PLATE | 26383－585m |
| C84 | CAP | ELEC 470U 25V 20\％＋PCB | 26421－129T |
| C85 | CAP | ELEC 470U 63v 20\％＋PCB | 26421－136C |
| C86 | CAP | ELEC 470U 25v 20\％＋PCB | 26421－129T |
| C87 | CAP | TANT 22U 35v 20\％ | 26486－231K |
| C88 | CAP | TANT 22v 35v 20\％ | 26486－231K |
| C89 | CAP | TANT 22U 16V 20\％BEAD | 26486－230B |
| C90 | CAP | TANT 22U 16V 20\％BEAD | 26486－230B |
| C91 | CAP | TANT 22U 16V 20\％BEAD | 26486－230в |
| C92 | CAP | TANT 10 U 35V 20\％BEAD | 26486－225C |
| C93 | CAP | TANT 10U 35v 20\％BEAD | 26486－225C |
| C94 | CAP | CER 56P 63V 2\％PLATE | 26343－474J |
| C95 | CAP | CER 47N 25v 20\％DISC | 26383－017U |
| C96 | CAP | CER 1NO 63v 10\％PLatte | 26383－585M |
| C97 | CAP | ELEC 470U 25V 20\％＋PCB | 26421－129T |
| C98 | CAP | ELEC 470u 16v 20\％＋PCB | 26421－127w |
| c99 | CAP | ELEC 470U $20 \%+$ PCB | 26421－127w |
| C100 | CAP 7 | tant 1u0 35v 20\％bead | 26486－209F |
| C101 | CAP | CER 1NO 63V 10\％PLATE | 26383－585M |
| C102 | CAP | TANT 6u8 6v 20\％BEAD | 26486－221T |
| C103 | CAP | CER 100N 50V 20\％M／LAYER | 26383－534Y |
| C104 | CAP | TANT 1U0 35V 20\％BEAD | 26486－209F |
| $\begin{aligned} & \text { C105 to } \\ & \text { C109 } \end{aligned}$ |  | CER 100P 100V 10\％EM | 100RD 101K |



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y8zo－LS88z
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$\begin{gathered}\text { Circuit } \\ \text { ref．}\end{gathered}$
C110 to
C113
C114
C115
C116 $\begin{array}{lll}\text { C116 CAP CHIP } & \text { 100P } & \text { 100V 10\％} \\ \text { C117 CAP CHIP } & 100 \mathrm{P} & 100 \mathrm{~V} \\ \text { 10\％}\end{array}$
 di Rect 1N5401 100 V כNAf AGL 8もItNt TIS Ia DI SIL 1 N 414875 V JUNC
DI SIL 1 N 414875 V JUNC I ZEN BZX79C 4．7v 5\％ $\begin{array}{ll}\text { DI ZEN BZX79C } & 5.1 \mathrm{~V} \\ \text { 2\％} \\ \text { ZEN }\end{array}$ DI SIL 1 N 414875 v JUNC
DI SIL 1 N 4148 75v JUNC DI SIL $1 N 414875 \mathrm{~V}$ JUNC DI ZEN $1 \mathrm{~N} 825 / \mathrm{A} 6.2 \mathrm{~V} 5 \%$ DI ZEN BZX79C $5.6 \mathrm{~V} 5 \%$ 808 b 0 V BRIDGE KBP608 800V 6A
RECT MR810 50v 1A 100NS RECT MR810 50V 1A 100NS DI RECT MR810 50v 1A 100NS DI ZEN BZX79C 5．1V 5\％ DI ZEN BZX79C4V7 4．7v 5\％
DI SIL $1 N 414875 \mathrm{~V}$ JUNC D1
D2
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26383－006C
Chap． 6
Page 6

| Part no． | Circuit ref． | Description |
| :---: | :---: | :---: |
| 26343－477v | C54 | CAP TANT 1U0 35V 20\％BEAD |
| 26538－770T | C55 | CAP CER 100N 50V 20\％M／LAYER |
| 26343－581G | C56 | CAP CER 10N 25V 20\％DISC |
| 26343－477v | C57 | CAP CER 10N 25V 20\％DISC |
| 26343－477v | C58 | CAP CER 100N 50V 20\％M／LAYER |
|  | C59 | CAP CER 100N 50V 20\％M／LAYER |
| 26486－230B | C60 | CAP CER 100N 50V 20\％M／LAYER |
| 26343－583S | C61 | CAP CER 100P 63V 2\％PLATE |
| 26582－406T | C62 | CAP TANT 10035 V 20\％BEAD |
| 26383－534Y | C63 | CAP CER 100P 63 V 2\％PLATE |
| 26343－583S | C64 | CAP TANT 1U0 35V 20\％BEAD |
| 26582－406T | C65 | CAP TANT 1U0 35V 20\％BEAD |
| 26383－006C | C66 | CAP CER 10N 25V 20\％DISC |
| 26486－209F | C67 | CAP TANT 1U0 35V 20\％BEAD |
| 26383－006C | C68 | CAP CER 10N 25V 20\％DISC |
| 26486－209F | C69 | CAP CER 10N 25V 20\％DISC |
| 26383－006C | C70 | CAP CER 100P 63v 2\％PLATE |
| 26486－209F | C71 | CAP CER 100N 50V 20\％M／LAYER |
| 26383－006C | C72 | CAP CER 100N 50V 20\％M／LAYER |
| 26486－209F | C73 | CAP CER 100N 50V 20\％M／LAYER |
| 26343－582v | C74 | CAP CER 100N 50V 20\％M／LAYER |
| 26582－428J | C75 | CAP TANT 1U0 35V 20\％BEAD |
| 26582－428J | C76 | CAP CER 10N 25V 20\％DISC |
| 26383－006C | C77 | CAP CER 10N 25V 20\％DISC |
| 26486－209F | C78 | CAP CER 100P 63v 2\％PLATE |
| 26383－006C | C79 | CAP CER 10N 25V 20\％DISC |


| Circuit ref． | Description |
| :---: | :---: |
| C29 | CAP CER 100P 63V 2\％PLATE |
| C30 | CAP PS 10NO 63V 2\％RAD |
| C31 | CAP CER 330P 100V 5\％ |
| C32 | CAP CER 100P 63V 2\％PLATE |
| C33 | CAP CER 100P 63V 2\％PLATE |
| C34 | CAP TANT 22U 16V 20\％BEAD |
| C35 | CAP CER 1NO 100V 5\％ |
| C36 | CAP PETP 220N 63V 10\％RAD |
| C37 | CAP CER 100N 50V 20\％M／LAYER |
| C38 | CAP CER 1NO 100V 5\％ |
| C39 | CAP PETP 220N 63V 10\％RAD |
| C40 | CAP CER 10N 25V 20\％DISC |
| C41 | CAP TANT 1U0 35v 20\％BEAD |
| C42 | CAP CER 10N 25V 20\％DISC |
| C43 | CAP TANT 1U0 35V 20\％BEAD |
| C44 | CAP CER 10N 25V 20\％DISC |
| C45 | CAP TANT 1U0 35V 20\％BEAD |
| C46 | CAP CER 10N 25V 20\％DISC |
| C47 | CAP TANT 1U0 35V 20\％BEAD |
| C48 | CAP CER 470P 100V 5\％ |
| C49 | CAP PETP 47N 63V 10\％RAD MIN |
| C50 | CAP PETP 47N 63V 10\％RAD MIN |
| C51 | CAP CER 10N 25V 20\％DISC |
| C52 | CAP TANT 1U0 35V 20\％BEAD |
| C53 | CAP CER 10N 25V 20\％DISC |


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| Part no． | Circuit ref． | Description |
| :---: | :---: | :---: |
| 28355－169N | IC13 | ICA AMP TLO72CP DUAL FET I／P |
| 28336－676J | IC14 | ICA SW HI3－201－5 QUAD |
| 28336－676J | IC15 | ICA AMP TLO72CP DUAL FET I／P |
| 28385－711A | IC16 | ICA SW HI3－201－5 QUAD |
| 28336－676J | IC17 | ICA COMP LM311N DIL8 |
| 28624－116K | IC18 | AMP TLO72CP DUAL FET I／P |
| 28371－417X | IC19 | ICA DAC AD7543JN 12BIT MULT |
| 28385－713H | IC20 | ICA AMP TLO72CP DUAL FET I／P |
| 28357－028K | IC21 | ICA DAC HS3140C－4 14BIT MULT ！ |
| 28357－028K | IC22 | ICA AMP OP27GZ ULTRA LOW NOISE |
| 28357－028K | IC23 | ICA AMP OP27GZ ULTRA LOW NOISE |
| 28357－028K | IC24 | ICA DAC AD7543JN 12BIT MULT ： |
| 28357－028K | IC25 | ICA AMP TL071CP FET I／P DIL8 |
| 28336－676J | IC26 | ICA VREG 78540 SMPS CTRL DIL16 |
|  | IC27 | ICA VREG＋ 7815 15V 1A TO220 |
| 28461－368T | IC28 | ICA VREG－ 7915 15v 1A TO220 |
| 28461－368T | IC29 | ICA VREG UA723C PROG DIL14 |
| 28461－934z |  |  |
| 28461－367D | L1 | IND CHOKE S．M．P．S． |
| 28468－307C | L6 | IND CHOKE 1UH 10\％MINIATURE |
| 28468－307C |  |  |
| 28468－313K |  |  |
| 28466－340R | PL1 | CON PCB HDR 50WAY FXD STRT |
| 28462－608A | PL2 | CON PCB MALE 6WAY FXD FR LOCK |
| 28461－934Z | PL3 | CON PART M／W made 2W Housg 12A |
| TEXAS | PL4 | CON PCB MALE 6WAY FXD FR LOCK |
| 28461－931B | PL5 | CON PCB MALE 8WAY FXD FR LOCK |


| Circuit ref． | Description |
| :---: | :---: |
| D23 | DI RECT 31DQ03 30v Schoirt |
| D25 | DI SIL 1N4148 75v Junc |
| D26 | DI SIL 1N4148 75 V JUNC |
| D27 | DI SCR BRY55－3 50V 0．8A |
| D28 | DI SIL 1 N 414875 V JUNC |
| D29 | LAMP LED YL4484 3V YELLOW |
| D30 | DI ZEN BZX79C 5．6V 5\％ |
| D31 | DI SCR 2N4441 50V 8A |
| D32 | DI RECT 1N4004 400V |
| D33 | DI RECT 1N4004 400V |
| D34 | DI RECT 1N4004 400V |
| D35 | DI RECT 1N4004 400V |
| D36 | DI RECT 1N4004 400V |
| D37 | DI SIL 1N4148 75v JUNC |
| IC1 | ICA AMP OP27GZ ULTRA LOW NOISE |
| IC2 | ICA AMP OP27GZ ULTRA LOW NOISE |
| IC3 | ICA SW HI3－201－5 QUAD |
| IC4 | ICA AMP OP14CP DUAL MATCHED |
| IC5 | ICD MONO 4047 AST MULTI BI |
| IC6 | ICD MONO 4047 AST MULTI BI |
| IC7 | ICD MONO 4538 DUAL RETR PREC |
| IC8 | ICD NAND 4011 QUAD 2INP BI |
| IC9 | ICD FF D 4013 DUAL BI |
| IC10 | ICA SW HI3－201－5 QUAD |
| IC11 | ICA AMP TL072CP DUAL FET I／P |
| IC12 | ICA DAC AD7543JN 12BIT MULT |
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RES MF 10K 1／4W 2\％100PPM RES MF 20K．6W 01\％6PPM RES MF 22K 1／4W 2\％100PPM



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23435－520K


24753－484H
24773－315U
24773－311A
24753－349U 24773－249J


24773－265M
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 24722－006S 24722－001L 25748－563F 24773－305R 24773－317N 24773－3097 24773－289W 24773－297M

CON PART M／W FEM 9W HOUSG 9A CON PART M／W FEM MALE 36 FXD STRAIGHT

RV CERM 5KO LIN 1／2W 10\％ RES MF 22K 1／4W $2 \%$ 100PPM $\begin{array}{lllll}\text { RES MF } & 68 \mathrm{~K} & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM} \\ \text { RES MF } & 33 \mathrm{~K} & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM}\end{array}$ $\begin{array}{llllll}\text { RES MF } & 33 \mathrm{~K} & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM} \\ \text { RES } & \text { MF } & 4 \mathrm{~K} 7 & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM}\end{array}$ RES MF 10K 1／4W 2\％100PPM

$\underset{\text { PLi }}{\text { PL } 7}$ $R 1$
$R 2$
$R 3$
$R 4$
$R 5$ R6 R6
R7
R8
R9
R10


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 $24773-273 A$
$24773-273 A$

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 WL6て－モLLもて


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 R97 or $\stackrel{8}{a}$


24773－249J
24773－249J


25711－643S 25711－640F 24773－344z 24773－289W $\pm 09 \varepsilon-\varepsilon 与 \angle ฤ て$
$\forall \varepsilon \angle Z-\varepsilon \angle L も 乙$ 24773－297M $24773-304 \mathrm{C}$
$24773-297 \mathrm{M}$ ヘレ8て－モLLもて 24773－261D 24773－304C $24753-567 \mathrm{~S}$
$25748-567 \mathrm{~W}$ 24753－627Y 247548－566S 24681－508P 24753－361G

## Description

 RES MF $100 \mathrm{R} 1 / 4 \mathrm{~W}$ 2\％100PPM RES MF 100R $1 / 4 \mathrm{~W} 2 \% 100 \mathrm{PPM}$ RES MF 100R 1／4W 2\％100PPM RES MF 10K 1／4W 2\％100PPM

RES MF 6K8 1／4W 2\％100PPM $\begin{array}{llllll}\text { RV CERM } & 10 \mathrm{~K} & \text { LIN } & .5 \mathrm{~W} & 10 \% \text { HORZ } \\ \text { RV CERM } & 50 \mathrm{~K} & \text { LIN } & .5 \mathrm{~W} & 10 \% \text { HORZ } \\ \text { RV CERM } & 5 \mathrm{KO} & \text { LIN } & .5 \mathrm{~W} & 10 \% \text { HORZ } \\ \text { RES MF } & 820 \mathrm{~K} & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM} \\ \text { RES MF } & 4 \mathrm{~K} 7 & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM} \\ \text { RES MF } & 4 \mathrm{~K} 3 & 1 / 4 \mathrm{~W} & 2 \% & 100 \mathrm{PPM}\end{array}$
 $\begin{array}{llll}\text { RES MF } & 1 \mathrm{KO} \\ \text { RES MF } & 1 \mathrm{~K} 05 & 1 / 4 \mathrm{~W} & .5 \% \\ \text { SOPPM }\end{array}$ RES MF 10K 1／4W 2：100PPM RES MF 20K 1／4W 2\％100PPM RES MF 3K9 1／4W 2\％100PPM RES MF 330R 1／4W 2\％100PPM RES MF 20K 1／4W 2\％100PPM RES MF 3K92 1／4W 0．5\％50PPM RV CERM 200R LIN 1／2W 10\％ WddOS \％S． 0 Mb／L ZOXt ज्ञाW STy RES MF $4 \mathrm{KO} 21 / 4 \mathrm{~W} 0.5 \%$
RV CERM 10 K LIN $1 / 2 \mathrm{~W} 10 \%$
RES NET $100 \mathrm{~K} 5 \% 15 \mathrm{DIL}$ RES MF 665R 1／4W ． $5 \%$ 50PPM （Am．2）
H 6960
Vol. 2





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Circuit
ref． $\quad$ Description

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DI SIL 1N4148 75V JUNC DI SIL 1N414875V JUNC $\begin{array}{llll}\text { DI SIL } & 1 N 4148 & 75 \mathrm{~V} & \text { JUNC } \\ \text { DI } & \text { SIL } & 1 N 4148 & 75 \mathrm{~V} \\ \text { JUNC }\end{array}$ DI SIL $1 N 4148$ 75V JUNC
DI SIL $1 N 3595$ 150V JUNC DI

CAP TANT 1U0 35V 20\％BEAD CAP CER 100N 50V 20\％M／LAYER CAP CER 100N 50V 20\％M／LAYER
CAP CER 100N 50V 20\％M／LAYER CAP CER 100N 50V 20\％M／LAYER㘶 CAP TANT 22U 16V 20\％BEAD
 DI ZEN BZX79C4V7 4．7V 5\％ DI ZEN BI SIL $1 \mathrm{~N} 4148 \quad 75 \mathrm{v}$ JUNC
DI SIL $1 \mathrm{~N} 4148 \quad 75 \mathrm{~V}$ JUNC
DI RECT $1 \mathrm{~N} 4004 \quad 400 \mathrm{~V}$
DI SIL $\infty$
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| Circuit ref. | Description |
| :---: | :---: |
| R7 | RES MF 100K 1/4W 2\% 100PPM |
| R8 | RES MF 100R 1/4W $2 \% 100 \mathrm{PPM}$ |
| R9 | RES MF 10K 1/4W 2\% 100PPM |
| R10 | RES MF $22 \mathrm{~K} 1 / 4 \mathrm{~W}$ 2\% 100PPM |
| R11 | RES MF $22 \mathrm{~K} 1 / 4 \mathrm{~W}$ 2\% 100PPM |
| R12 | RES MF 47K 1/4W 2\% 100PPM |
| R13 | RES MF 10K 1/4W 2\% 100PPM |
| R14 | RES MF 10K 1/4W 2\% 100PPM |
| R15 | RES MF 10K 1/4W 2\% 100PPM |
| R16 | RES MF 10K 1/4W 2\% 100PPM |
| R17 | RES MF 6K8 1/4W 2\% 100PPM |
| R18 | RES MF 4K7 1/4W 2\% 100PPM |
| R19 | RES MF 1K0 1/4W 2\% 100PPM |
| R20 | RES MF 4K7 1/4W 2\% 100PPM |
| R21 | RES MF $100 \mathrm{~K} 1 / 4 \mathrm{~W} 2 \% 100 \mathrm{PPM}$ |
| R22 | RES MF 33K 1/4W 2\% 100PPM |
| R23 | RES MF 22K 1/4W 2\% 100PPM |
| S1 | SW PUSH 1P1W MOM LIPA D6 |
| S2 | SW SLIDE $4 \times 2 \mathrm{~W}$ 28V DIL QUAD |
| TR1 | TR NSI 2N2369 15V 500M - SW |
| TR2 | TR NSI 2N2369 15V 500M - SW |
| X10 | S/C ACC SKT dil2 |
| X11 | S/C ACC PAD TO18, ETC TO .1" GRD |

H 6960
Vol. 2




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H 6960
Vol. 2



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| Description |
| :---: |
| CAP CER 100N 100V 20\％＋M／LAYER |
| CAP CER 33P 63V 5\％PLATE |
| CAP CER 18P 63V 5\％PLATE |
| CAP CER 18P 63V 5\％PLATE |
| CAP CER 100P 63V 2\％PLATE |
| CAP CER 1NO 63V 10\％PLATE |
| CAP CER 100N 100V 20\％＋M／LAYER |
| CAP CER 1NO 63V 10\％PLATE |
| CAP CER 100N 100V 20\％＋M／LAYER |
| CAP CER 18P 63V 5\％PLATE |
| CAP VAR PLAS 22P 2P TRIM |
| CAP CER 100P 63v 2\％PLATE |
| CAP CER 1NO 63V 10\％PLATE |
| CAP TANT 1U0 35v 20\％BEAD |
| CAP TANT 1U0 35V 20\％BEAD |
| CAP CER 47N 25V 20\％DISC |
| CAP CER 100N 100V 20\％＋M／LAYER |
| CAP CER 100N 100V 20\％＋M／LAYER |
| DI SIL 1N4148 75v Junc |
| DI H／CARR 1N5711 |
| DI H／CARR 1N5711 |
| DI SIL 1N4148 75v JUNC |
| ICA AMP Op14CP DUAL MATCHED |

H 6960



Fig. 1 Miscellaneous mechanical parts

## SERVICING DIAGRAMS

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## CIRCUIT NOTES

Component values

1. Resistors : Code letter $R=$ ohms, $k=\operatorname{kilohms}\left(10^{3}\right), M=\operatorname{megohms}\left(10^{6}\right)$.

Capacitors: Code letter $\begin{aligned} \mathrm{m} & =\text { millifarads }\left(10^{-3}\right), \mu \\ \mathrm{n} & =\text { manofarads }\left(10^{-9}\right), \mathrm{p}\end{aligned}$ = picofarads $\left(10^{-6}\right)$,
Inductors : Code letter $H=$ henrys, $m=$ millihenrys $\left(10^{-3}\right)$, $\mu=$ microhenrys $\left(10^{-6}\right), \mathrm{n}=$ nanohenrys $\left(10^{-9}\right)$.

SIC : Value selected during test, nominal value shown.
2. Components are marked normally with two, three or four figures according to the accuracy limit $\pm 10 \%, \pm 1 \%$ or $\pm 0.1 \%$. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4 m 7 could be interpreted as milliohms, millifarads or millihenrys, all values are placed near to its related symbol.



Drg. No. 6960/900 Sht. 1 of 4, Iss. 2
AA01 : Analogue p.c.b. assembly



Fig. 2



AAO1 : AnaTogue p.c.b. assembly



AA02/1 : Processor p.c.b. assembly
Drg. No. 6960/903 Sht. 1 of 2, Iss. 1


Board detail: AA02/1

^1 INDICATES STATIC SENSITIVE COMPONENTS

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Drg. No. 6960/902 Sht. 1 of 1, Iss. 1
AB01 : Power meter keyboard and display assembly


Component layout and board detail : ACO4


NOTE.
$\triangle$ indicates static sensitive component.


Component layout and board detail


Drg. No. 3964/921, Sht. 1 of 1, Iss. 1

