HITACHI

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the "Safety Precautions" and "Product Safety Notices" in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise" und „Hinweise zur Produktsicherheit" in diesem Wartungshandbuch zu lesen.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Colour Television
August 2005

TABLE OF CONTENTS

1. INTRODUCTION

32" TFT TV is a progressive TV control system with built-in **de-interlacer** and **scaler**. It uses a 1366*768 panel with 16:9 aspect ratio. The TV is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Sound system output is supplying 2x8W (10%THD) for stereo 8Ω speakers. The chassis is equipped with many inputs and outputs allowing it to be used as a center of a media system.

It supports following peripherals:
2 SCART sockets
1 AV input (CVBS + Stereo Audio)
1 SVHS input
1 Stereo Headphone input
1 Component input (YPbPr + Stereo Audio)
1 D-Sub 15 PC input
1 HDMI input
1 Stereo audio input for PC
Audio line out is taken from the scart with given scart-to-line out connector

2. TUNER

The tuners used in the design are combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L', I/I', and D/K. The tuning is available through the digitally controlled I^2C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

Features of UV1316:
1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
3. Digitally controlled (PLL) tuning via I^2C-bus
4. Off-air channels, S-cable channels and Hyper band
5. World standardised mechanical dimensions and world standard pinning
6. Compact size
7. Complies to "CENELEC EN55020" and "EN55013"

Pinning:
1.	Gain control voltage (AGC)	:	4.0V, Max: 4.5V
2.	Tuning voltage		
3.	I²C-bus address select	:	Max: 5.5V
4.	I²C-bus serial clock	:	Min:-0.3V, Max: 5.5V
5.	I²C-bus serial data	:	Min:-0.3V, Max: 5.5V
6.	Not connected		
7.	PLL supply voltage	:	5.0V, Min: 4.75V, Max: 5.5V
8.	ADC input		
9.	Tuner supply voltage	:	33V, Min: 30V, Max: 35V
10.	Symmetrical IF output 1		
11.	Symmetrical IF output 2		

3. IF PART (TDA9886)

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL. The following figure shows the simplified block diagram of the integrated circuit.
The integrated circuit comprises the following functional blocks:
VIF amplifier, Tuner and VIF-AGC, VIF-AGC detector, Frequency Phase-Locked Loop (FPLL) detector, VCO and divider, Digital acquisition help and AFC, Video demodulator and amplifier, Sound carrier trap, SIF amplifier, SIF-AGC detector, Single reference QSS mixer, AM demodulator, FM demodulator and

acquisition help, Audio amplifier and mute time constant, I²C-bus transceivers and MAD (module address), Internal voltage stabilizer.
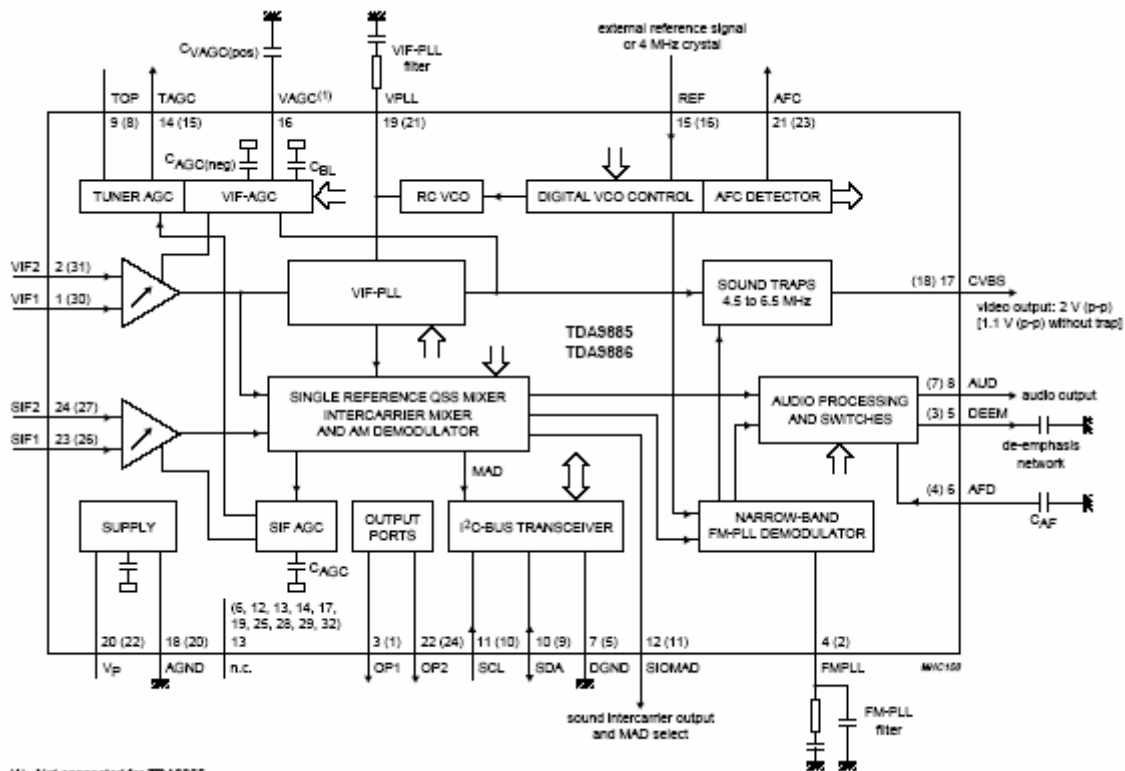
(1) Not connected for TDA9885.

4. MULTI STANDARD SOUND PROCESSOR

The MSP34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP34x1G has optimum stereo performance without any adjustments.

5. VIDEO SWITCH TEA6415

In case of three or more external sources are used, the video switch IC TEA6415 is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS. Driving 75ohm load needs an external resistor. It is possible to have the same input connected to several outputs.

6. AUDIO AMPLIFIER STAGE WITH TPA3002D2

The TPA3004D2 is a 9-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3004D2 can drive stereo speakers as low as 8 Ω. The high efficiency of the TPA3004D2 eliminates the need for external heatsinks when playing music.

Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from –40 dB to 36 dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from –56 dB to 20 dB.

An integrated 5-V regulated supply is provided for powering an external headphone amplifier.

7. MICROCONTROLLER

The Micronas SDA 55xx TV microcontroller is dedicated to 8 bit applications for TV control and provides dedicated graphic features designed for modern low class to mid range TV sets. The SDA 55xx provides also an integrated general purposefully 8051-compatible microcontroller with specific hardware features especially suitable in TV sets. The microcontroller core has been enhanced to provide powerful features such as memory banking, data pointers and additional interrupts, etc. The internal XRAM consists of up to 16 kBytes. The microcontroller provides an internal ROM of up to 128 kBytes. ROMless versions can access up to 1 MByte of external RAM and ROM. The 8-bit microcontroller runs at 33.33 MHz internal clock. SDA 55xx is realized in 0.25 micron technology with 2.5 V supply voltage for the core and 3.3 V for the I/O port pins to make them TTL compatible. Based on the SDA 55xx microcontroller the MINTS software package was developed and provides dedicated device drivers for many Micronas video & audio products and includes a full blown TV control SW for the PEPER application chassis. The SDA 55xx is also supported with powerful design tools like emulators from Hitex, Kleinhenz, iSystems, the Keil C51 Compiler and TEDIpro OSD development SW by Tara Systems.

8. EEPROM 24C32

The Microchip Technology Inc. 24C32 is a 4Kx8 (32 Kbit) Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications.

9. CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

10. SAW FILTERS
K9656M:
Standard:
• B/G
• D/K
• I
• L/L'

Features
• TV IF audio filter with two channels
• Channel 1 (L') with one pass band for sound carriers at 40.40 MHz (L') and 39.75 MHz (L'- NICAM)
• Channel 2 (B/G, D/K, L, I) with one pass band for sound carriers between 32.35 MHz and 33.40 MHz

Terminals
• Tinned CuFe alloy

Pin configuration
1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

K3958M:
Standard:
• B/G
• D/K
• I
• L/L'

Features
• TV IF video filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
• Constant group delay

Terminals
Tinned CuFe alloy

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

11. IC DESCRIPTIONS
TEA6415C
24LC02
4MX32 DDR SDRAM (128M)
MAD4868A
TCET1102G OPTOCOUPLER
SVP-EX 59B
TL431
24C32
74LVC14A
TEA6420D
CS4334
GAL16LV8
K6R4008V1
L6562D
LM1086
LM1117
LM317T
LM809
MSP3411G
M29W040B
MC33202
PCF8574
PI5V330
SDA5550
SG3525
SII9993
NCP1014
SN74CB3Q3305
ST24LC21
LM2576
MC34063
TDA1308
TDA9886T
TPA3002D2
µPA672T
VPC3230D

11.1. TEA6415C

11.1.1. General Description

The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V$_{DC}$ on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75Ω load needs an external transistor. It is possible to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

11.1.2. Features

• 20MHz Bandwidth
• Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
• 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
• 6 Outputs
• Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
• Bus controlled
• 6.5dB gain between any input and output
• 55dB crosstalk at 5mHz
• Fully ESD protected

11.1.3. Pinning

1.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
2.	Data	:	Low level	: -0.3V Max: 1.5V,
			High level	: 3.0V Max : Vcc+0.5V
3.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
4.	Clock	:	Low level	: -0.3V Max: 1.5V,
			High level	: 3.0V Max : Vcc+0.5V
5.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
6.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
7.	Prog			
8.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
9.	Vcc	:	12V	
10.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
11.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
12.	Ground			
13.	Output	:	5.5Vpp,	Min : 4.5Vpp
14.	Output	:	5.5Vpp,	Min : 4.5Vpp
15.	Output	:	5.5Vpp,	Min : 4.5Vpp
16.	Output	:	5.5Vpp,	Min : 4.5Vpp
17.	Output	:	5.5Vpp,	Min : 4.5Vpp
18.	Output	:	5.5Vpp,	Min : 4.5Vpp
19.	Ground			
20.	Input	:		Max : 2Vpp, Input Current : 1mA, Max : 3mA

11.2. 24LC02

11.2.1. Description

The Microchip Technology Inc. 24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1µA and 1mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data.

11.2.2. Features

• Single supply with operation down to 1.8V
• Low-power CMOS technology
     -1mA active current typical
     -1µA standby current typical (I-temp)
• Organized as 1 block of 256 bytes (1 x 256 x 8)
• 2-wire serial interface bus, I^2C™ compatible
• Schmitt Trigger inputs for noise suppression
• Output slope control to eliminate ground bounce
• 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
• Self-timed write cycle (including auto-erase)
• Page write buffer for up to 8 bytes
• 2ms typical write cycle time for page write
• Hardware write-protect for entire memory
• Can be operated as a serial ROM
• Factory programming (QTP) available
• ESD protection > 4,000V
• 1,000,000 erase/write cycles
• Data retention > 200 years
• 8-lead PDIP, SOIC, TSSOP and MSOP packages
• 5-lead SOT-23 package
• Pb-free finish available
• Available for extended temperature ranges:
     -Industrial (I): -40°C to +85°C
     -Automotive (E): -40°C to +125°C

11.2.3. Pinning

PDIP/SOIC/TSSOP/MSOP

A0 1 — 8 Vcc
A1 2 — 7 WP
A2 3 — 6 SCL
Vss 4 — 5 SDA
24XX02

SOT-23-5

SCL 1 — 5 WP
Vss 2
SDA 3 — 4 Vcc
24XX02

Note: Pins A0, A1 and A2 are not used by the 24XX02. (No internal connections).
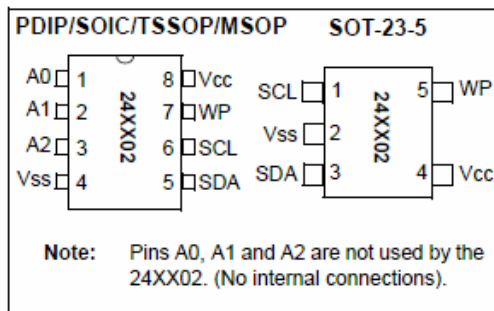
Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
Vss	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write-Protect Input
Vcc	8	8	8	8	4	+1.8V to 5.5V Power Supply

11.3. MAD4868A

11.3.1. General Description

The Micronas Audio Delay IC MAD 4868A acts as a delay line for TV audio and consumer audio applications. The IC is designed for synchronizing audio and video signals ensuring "Lip Sync" by delaying the audio signal with the same amount of time as the video signal is delayed in a TV's video processing.

For TV designs, independent signals for loudspeakers, headphones, and line-out or S/PDIF out must be provided, resulting in the need to delay six independent audio channels.

11.3.2. Features

- 32 k audio samples RAM:
- Total delay time of 680 ms at 48 kHz or 1020 ms at 32 kHz sampling rate
- 32/18-bit word width:
- 32-bit High-Resolution mode or 18-bit Standard mode
- Sampling rates from 32 kHz to 48 kHz for serial 8-channel mode are supported
- Sampling rates from 4 kHz to 192 kHz for parallel 2-channel mode are supported
- Memory allocation:
- MAD 4868A's memory can be allocated for 1... 8 audio channels. Delay time can be programmed for each channel individually.

11.3.3. Interfaces

- 8-channel Micronas I^{2}S input and output:
- In combination with Micronas ICs (serial mode) (e.g. MSP 44/46xyK, MAS 35xyH), eight audio channels can be routed through MAD 4868A by using four lines only.
- 4x2-channel standard I^{2}S inputs and outputs (parallel mode) allow routing eight audio channels with sampling rates of 4... 192 kHz through MAD 4868A
- I^{2}C control for delay time programming
- Address select to set one out of two available I^{2}C addresses

11.3.4. Pinning
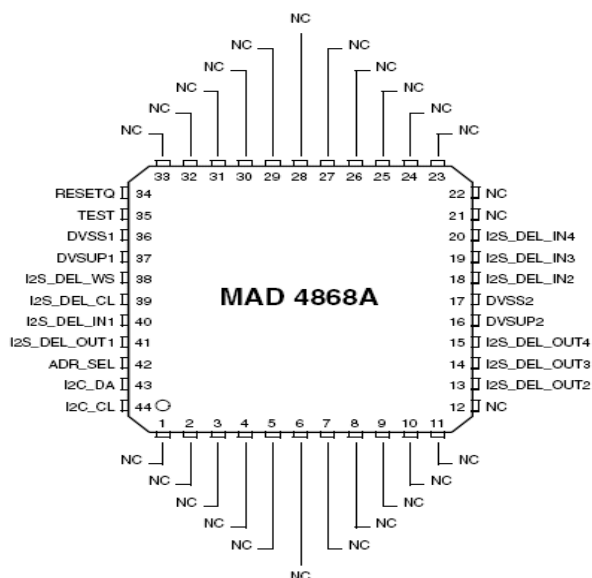
Pin No. PMQFP44-1	Pin Name	Type	Connection (If not used)	Short Description
1...12	NC		LV	Not Connected
13	I2S_DEL_OUT2	OUT	OBL	I²S data output channel 3 + 4
14	I2S_DEL_OUT3	OUT	OBL	I²S data output channel 5 + 6
15	I2S_DEL_OUT4	OUT	OBL	I²S data output channel 7 + 8
16	DVSUP2	SUP	DVSUP	Digital Power Supply
17	DVSS2	SUP	DVSS	Digital Ground
18	I2S_DEL_IN2	IN	OBL	I²S data input channel 3 + 4
19	I2S_DEL_IN3	IN	OBL	I²S data input channel 5 + 6
20	I2S_DEL_IN4	IN	OBL	I²S data input channel 7 + 8
21...33	NC		LV	Not Connected
34	RESETQ	IN	OBL	Power-On Reset (active low)
35	TEST	IN	DVSS	Test pin
36	DVSS1	SUP	DVSS	Digital Ground
37	DVSUP1	SUP	DVSUP	Digital Power Supply
38	I2S_DEL_WS	IN	OBL	I²S word strobe input
39	I2S_DEL_CL	IN	OBL	I²S clock input
40	I2S_DEL_IN1	IN	OBL	I²S data input channel 1 + 2 or 1..8
41	I2S_DEL_OUT1	OUT	OBL	I²S data output channel 1 + 2 or 1..8
42	ADR_SEL	IN	OBL	I²C bus address select
43	I2C_DA	IN/OUT	OBL	I²C Data
44	I2C_CL	IN/OUT	OBL	I²C Clock

11.4. TCET1102G Optocoupler

11.4.1. General Description

The TCET110. / TCET2100/ TCET4100 consist of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 4-lead up to 16-lead plastic dual inline package.

The elements are mounted on one lead frame using a **coplanar technique,** providing a fixed distance between input and output for highest safety requirements.

11.4.2. General Features

- CTR offered in 9 groups
- Isolation materials according to UL94-VO
- Pollution   degree   2
(DIN/VDE 0110 / resp. IEC 664)
- Climatic classification 55/100/21 (IEC 68 part 1)
- Special construction:
- Therefore, extra low coupling capacity of typical 0.2 pF, high Common Mode Rejection
- Low temperature coefficient of CTR
- G=Leadform10.16mm;   provides   creepage   distance   >   8   mm,
for TCET2100/ TCET4100 optional;
- suffix letter 'G' is not marked on the optocoupler
- Coupling System U

11.4.3. Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):

For appl. class I – IV at mains voltage ≤300 V
For appl. class I – III at mains voltage ≤600 V
According to VDE 0884, table 2, suitable for: **Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interface.**

11.5. SVP-EX 59B

11.5.1. General Description

To improve the video quality of the PAL CVBS and HD video input, the all layer changed EX59 improve video sharpness function in HD channel and enhance the 3D PAL quality compared to EX52 Rev. D chips.

11.6. TL431

11.6.1. General Description

The TL431/TL431Aare three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between Vref (approximately 2.5 volts) and 36 volts with two external resistors These devices have a typical dynamic output impedance of 0.2W Active output circuitry provides a very sharp turn-on characteristic, making these devices excel lent replacement for zener diodes in many applications.

11.6.2. Features

- Programmable Output Voltage to 36 Volts
- Low Dynamic Output Impedance 0.20 Typical
- Sink Current Capability of 1.0 to 100mA
- Equivalent Full-Range Temperature Coefficient of 50ppm/°C Typical
- Temperature Compensated For Operation Over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Fast Turn-on Response

11.7. 24C32

11.7.1. General Description

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications.

11.7.2. Features

• Voltage operating range: 4.5V to 5.5V
- Peak write current 3 mA at 5.5V
- Maximum read current 150µA at 5.5V
- Standby current 1µA typical
• Industry standard two-wire bus protocol, I^{2}C™ compatible
-Including 100 kHz and 400 kHz modes
• Self-timed write cycle (including auto-erase)
• Power on/off data protection circuitry
• Endurance:
- 10,000,000 Erase/Write cycles guaranteed for High Endurance Block
- 10,000,000 E/W cycles guaranteed for Standard Endurance Block
• 8 byte page, or byte modes available

• 1 page x 8 line input cache (64 bytes) for fast write
loads
• Schmitt trigger, filtered inputs for noise suppression
• Output slope control to eliminate ground bounce
• 2 ms typical write cycle time, byte or page
• Up to 8 chips may be connected to the same bus for up to 256K bits total memory
• Electrostatic discharge protection > 4000V
• Data retention > 200 years
• Temperature ranges:
       -Commercial (C): 0°C to +70°C
       -Industrial (I): -40°C to +85°C

11.7.3. Pinning

PDIP

```
      A0 ▯ 1        8 ▯ Vcc
      A1 ▯ 2        7 ▯ NC
           24C32
      A2 ▯ 3        6 ▯ SCL
     Vss ▯ 4        5 ▯ SDA
```

SOIC

```
      A0 ▯ 1        8 ▯ Vcc
      A1 ▯ 2        7 ▯ NC
           24C32
      A2 ▯ 3        6 ▯ SCL
     Vss ▯ 4        5 ▯ SDA
```
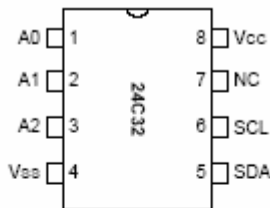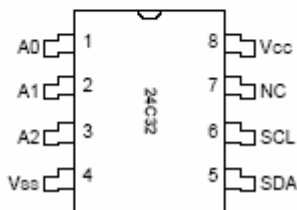
PIN Function Table

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

PIN DESCRIPTIONS
A0, A1, A2 Chip Address Inputs
The A0...A2 inputs are used by the 24C32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, and A0) in the control byte.
SDA Serial Address/Data Input/Output
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal; therefore the SDA bus requires a pull-up resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).
For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.
SCL Serial Clock
This input is used to synchronize the data transfer from and to the device.

11.8. 74LVC14A

11.8.1. Description

The 74LVC14A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5V environment. The 74LVC14A provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

11.8.2. Features

• Wide supply voltage range from 1.2 to 3.6 V
• CMOS low power consumption
• Direct interface with TTL levels
• Inputs accept voltages up to 5.5 V
• Complies with JEDEC standard no.8-1A
• ESD protection:
        HBM EIA/JESD22-A114-A exceeds 2000V
        MM EIA/JESD22-A115-A exceeds 200V.
• Specified from -40 to +85C and -40 to +125C.

11.8.3. Pinning
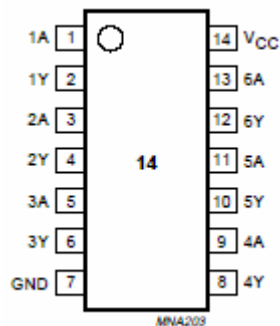
PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V_{CC}	supply voltage

11.9. TEA6420

11.9.1. Features

• 5 Stereo Inputs
• 4 Stereo Outputs
• Gain Control 0/2/4/6dB/Mute for each Output
• Cascadable (2 different addresses)
• Serial Bus Controlled
• Very low Noise
• Very low Distortion

11.9.2. Description

The TEA6420 switches 5 stereo audio inputs on4stereo outputs. All the switching possibilities are changed through the I^{2}C bus.

11.9.3. Pin Connections
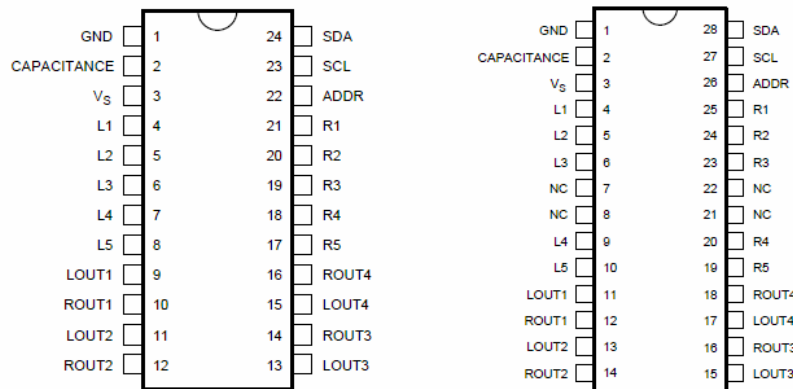
11.10. CS4334

11.10.1. Features

• Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
• 24-Bit Conversion
• 96 dB Dynamic Range
• -88 dB THD+N
• Low Clock Jitter Sensitivity
• Single +5V Power Supply
• Filtered Line Level Outputs
• On-Chip Digital De-emphasis
• Popgaurd® Technology
• Functionally Compatible with CS4330/31/33

11.10.2. General Description

The CS4334 family members are complete, stereo digital-to-analog output systems including interpolation, 1-bitD/A conversion and output analog filtering in an 8-pinpackage. The CS4334/5/6/7/8/9 support all major audio data interface formats, and the individual devices differ only in the supported interface format. The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency. The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support circuitry. These features are ideal for set-top boxes, DVD players, SVCD players, and A/V receivers.

11.10.3. Pin Descriptions

SERIAL DATA INPUT	**SDATA**	1 ● ⎵ 8	**AOUTL** ANALOG LEFT CHANNEL OUTPUT
DE-EMPHASIS / SCLK	**DEM/SCLK**	2 · 7	**VA** ANALOG POWER
LEFT / RIGHT CLOCK	**LRCK**	3 · 6	**AGND** ANALOG GROUND
MASTER CLOCK	**MCLK**	4 · 5	**AOUTR** ANALOG RIGHT CHANNEL OUTPUT

No.	Pin Name	I/O	Pin Function and Description
1	SDATA	I	*Serial Audio Data Input* - two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4334/5/6/7/8/9 via internal or external SCLK, and the channel is determined by LRCK.
2	DEM/SCLK	I	*De-Emphasis/External Serial Clock Input* - used for de-emphasis filter control or external serial clock input.
3	LRCK	I	*Left/Right Clock* - determines which channel is currently being input on the Audio Serial Data Input pin, SDATA.
4	MCLK	I	*Master Clock* - frequency must be 256x, 384x, or 512x the input sample rate in BRM and either 128x or 192x the input sample rate in HRM.
5	AOUTR	O	*Analog Right Channel Output* - typically 3.5 Vp-p for a full-scale input signal.
6	AGND	I	*Analog Ground* - analog ground reference is 0V.
7	VA	I	*Analog Power* - analog power supply is nominally +5V.
8	AOUTL	O	*Analog Left Channel Output* - typically 3.5 Vp-p for a full-scale input signal.

11.11. GAL16LV8

11.11.1. Description

The GAL16LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL16LV8C can interface with both 3.3V and 5Vsignal levels. The GAL16LV8 is manufactured using Lattice Semiconductor's advanced 3.3V E^2CMOS process, which combines CMOS with Electrically Erasable (E^2) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The 3.3V GAL16LV8 uses the same industry standard 16V8 architecture as its 5V counterpart and supports all architectural features such as combinatorial or registered macrocell operations.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

11.11.2. Features

• HIGH PERFORMANCE E2CMOS® TECHNOLOGY
   - 3.5 ns Maximum Propagation Delay
   - Fmax = 250 MHz
   - 2.5 ns Maximum from Clock Input to Data Output
   - UltraMOS® Advanced CMOS Technology
• 3.3V LOW VOLTAGE 16V8 ARCHITECTURE
   - JEDEC-Compatible 3.3V Interface Standard
   - 5V Compatible Inputs
   - I/O Interfaces with Standard 5V TTL Devices (GAL16LV8C)
• ACTIVE PULL-UPS ON ALL PINS (GAL16LV8D Only)
• E2 CELL TECHNOLOGY
   - Reconfigurable Logic
   - Reprogrammable Cells
   - 100% Tested/100% Yields
   - High Speed Electrical Erasure (<100ms)
   - 20 Year Data Retention
• EIGHT OUTPUT LOGIC MACROCELLS
   - Maximum Flexibility for Complex Logic Designs
   - Programmable Output Polarity

- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
    - 100% Functional Testability
- APPLICATIONS INCLUDE:
    - Glue Logic for 3.3V Systems
    - DMA Control
    - State Machine Control
    - High Speed Graphics Processing
    - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

11.11.3. Pin connections
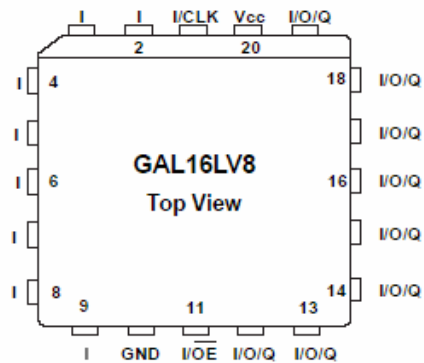
11.12. K6R4008V1D

11.12.1. Description

The K6R4008V1D is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. TheK6R4008V1D uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG′s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4008V1D is packaged in a 400 mil 36-pin plastic SOJ and 44-pin plastic TSOP type II.

11.12.2. Features

- Fast Access Time 8, 10ns(Max.)
- Low Power Dissipation
    - Standby (TTL) : 20mA(Max.)
            (CMOS) : 5mA(Max.)
    - Operating K6R4008V1D-08 : 80mA(Max.)
            K6R4008V1D-10 : 65mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
    - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
    K6R4008V1D-J : 36-SOJ-400
    K6R4008V1D-K : 36-SOJ-400(Lead-Free)
    K6R4008V1D-T : 44-TSOP2-400BF
    K6R4008V1D-U : 44-TSOP2-400BF(Lead-Free)
- Operating in Commercial and Industrial Temperature range.

11.12.3. Pin Description
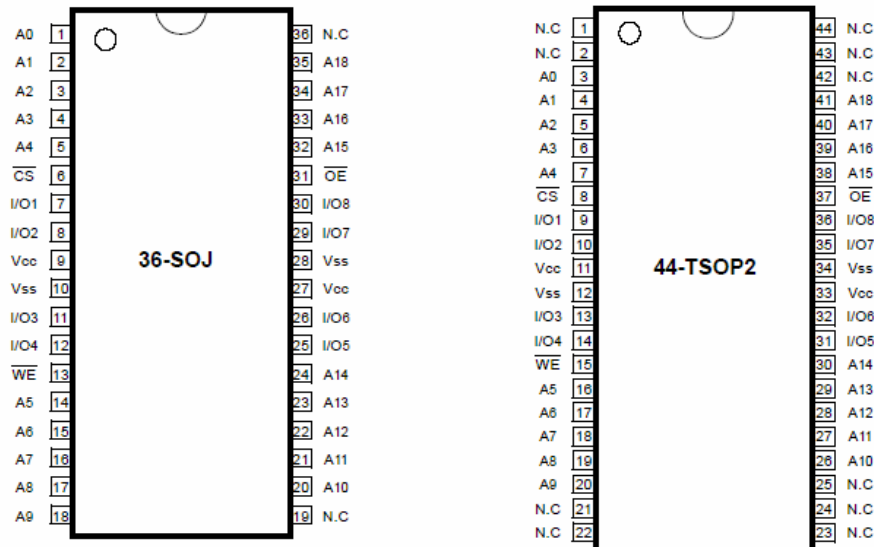
Pin Name	Pin Function
A0 - A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

11.13. L6562

11.13.1. Features

• TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
• PROPRIETARY MULTIPLIER DESIGN FOR MINIMUM THD OF AC INPUT CURRENT
• VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
• ULTRA-LOW (≤70µA) START-UP CURRENT
• LOW (≤4 mA) QUIESCENT CURRENT
• EXTENDED IC SUPPLY VOLTAGE RANGE
• ON-CHIP FILTER ON CURRENT SENSE
• DISABLE FUNCTION
• 1% (@ Tj = 25 °C) INTERNAL REFERENCE VOLTAGE

11.13.2. Description

The L6562 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor L6561, it offers improved performance. The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

11.13.3. Pin Connections and Descriptions
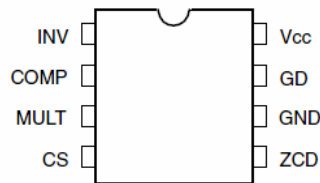
N°	Pin	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

11.14. LM1117

11.14.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

11.14.2. Features

• Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
• Space Saving SOT-223 Package
• Current Limiting and Thermal Protection
• Output Current 800mA
• Line Regulation 0.2% (Max)
• Load Regulation 0.4% (Max)
• Temperature Range
— LM1117 0°C to 125°C
— LM1117I -40°C to 125°C

11.14.3. Applications

• 2.85V Model for SCSI-2 Active Termination
• Post Regulator for Switching DC/DC Converter
• High Efficiency Linear Regulators
• Battery Charger
• Battery Powered Instrumentation

11.14.4. Connection Diagrams

SOT-223
Top View
TO-220
Top View
TO-252
Top View
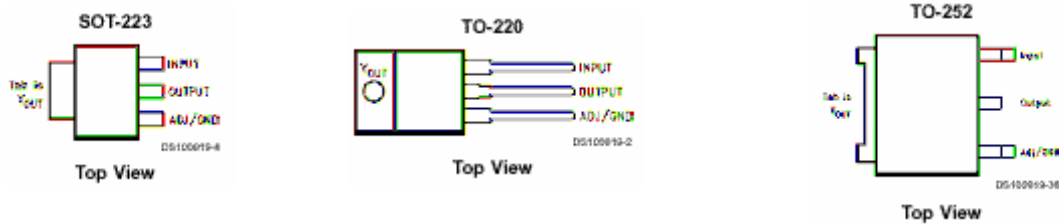
11.15. LM317

11.15.1. General Description

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V. It employs internal current limiting, thermal shut-down and safe area compensation.

11.15.2. Features

• Output Current In Excess of 1.5A
• Output Adjustable Between 1.2V and 37V
• Internal Thermal Overload Protection
• Internal Short Circuit Current Limiting
• Output Transistor Safe Operating Area Compensation
• TO-220 Package

11.15.3. Pin Description

TO-220

1. Adj 2. Output 3. Input

11.16. LM809

11.16.1. General Description

The LM809/810 microprocessor supervisory circuits can be used to monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down and brown-out conditions. The function of the LM809/810 is to monitor the VCC supply voltage, and assert a reset signal whenever this voltage declines below the factory-programmed reset threshold. The reset signal remains asserted for 240 ms after VCC rises above the threshold. The LM809 has an active-low RESET output, while the LM810 has an active-high RESET output. Seven standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 3V supply voltages. With a low supply current of only 15μA, the LM809/810 are ideal for use in portable equipment.

11.16.2. Features

• Precise monitoring of 3V, 3.3V, and 5V supply voltages
• Superior upgrade to MAX809/810
• Fully specified overtemperature
• 140 ms min. Power-On Reset pulse width, 240 ms typical
      Active-low RESET Output(LM809)
      Active-high RESET Output(LM810)

• Guaranteed RESET Output valid for VCC≥1V
• Low Supply Current, 15µAtyp
• Power supply transient immunity

11.16.3.   Pinning

( ) are for LM810
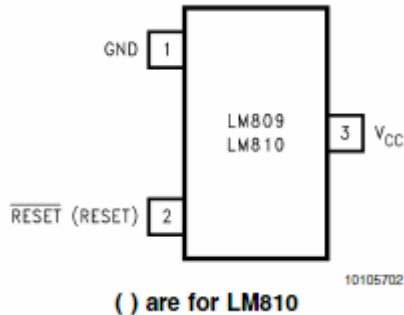
PIN		NAME	FUNCTION
(LLP)	SOT-23		
1	1	GND	Ground reference
3	2	$\overline{\text{RESET}}$ (LM809)	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
		RESET (LM810)	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
5	3	V_{CC}	Supply Voltage (+5V, +3.3V, or +3.0V)

11.17. MSP34X1G
Multistandard Sound Processor Family

11.17.1.   Introduction

The MSP 34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP 34x1G.

The MSP 34x1G has all functions of the MSP 34x0G with the addition of a virtual surround sound feature.

Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP 34x1G includes the Micronas virtualizer algorithm "3D-PANORAMA" which has been approved by the Dolby 1) Laboratories for with the "Virtual Dolby Surround" technology. In addition, the MSP 34x1G includes the "PAN-ORAMA" algorithm.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments.

The MSP 34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automat-ically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I 2 C interaction is necessary (Automatic Sound Selection).
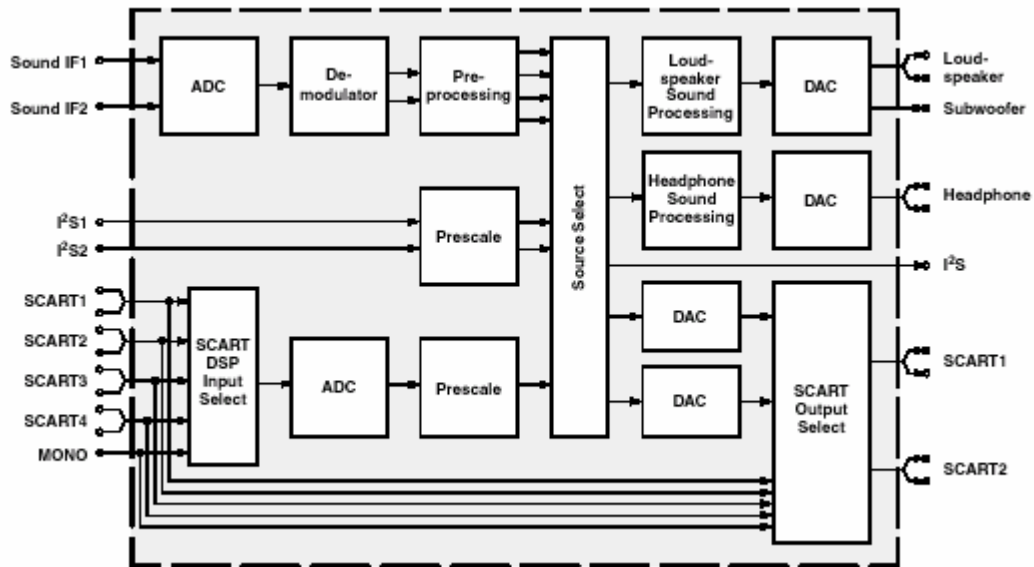
Source Select

I^2S bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2: For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT: For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL: Gives the timing for the transmission of I^2S serial data (1.024 MHz).
4. I2S_WS: The I2S_WS word strobe line defines the left and right sample.

11.17.2.　　　　Features

• Standard Selection with single I^2C transmission
• Automatic Standard Detection of terrestrial TV standards
• Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
• Two selectable sound IF (SIF) inputs
• Automatic Carrier Mute function
• Interrupt output programmable (indicating status change)
• Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
• AVC: Automatic Volume Correction
• Subwoofer output with programmable low-pass and complementary high-pass filter
• 5-band graphic equalizer for loudspeaker channel
• Spatial effect for loudspeaker channel
• Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
• Complete SCART in/out switching matrix
• Two I^2S inputs; one I^2S output
• Dolby Pro Logic with DPL 351xA coprocessor
• All analog FM-Stereo A2 and satellite standards; AM-SECAM L standard
• Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
• Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
• ASTRA Digital Radio (ADR) together with DRP 3510A
• All NICAM standards
• Korean FM-Stereo A2 standard

11.17.3.　　　　Pin connections

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	-	-	-	-	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR Data Output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I^{2}S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I^{2}S data output
6	12	10	5	4	I2S_WS	IN/OUT	LV	I^{2}S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I^{2}S clock
8	10	8	3	2	I2C_DA	IN/OUT	OBL	I^{2}C data
9	9	7	2	1	I2C_CL	IN/OUT	OBL	I^{2}C clock
10	8	-	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	OBL	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	OBL	I^{2}C bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	-	76	59	NC		LV	Not connected
16	2	-	75	58	NC		LV	Not connected
17	-	-	-	-	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	OBL	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	OBL	Crystal oscillator
22	61	50	70	53	TESTEN	IN	OBL	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF/LV	IF Input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN-	IN	AVSS via 56 pF/LV	IF common (can be left vacant, only if IF input 1 is also not in use)
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	49	AVSUP		OBL	Analog power supply 5V
-	-	-	65	-	AVSUP		OBL	Analog power supply 5V
-	-	-	64	-	NC		LV	Not connected
-	-	-	63	-	NC		LV	Not connected
27	56	45	62	48	AVSS		OBL	Analog ground
-	-	-	61	-	AVSS		OBL	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
-	-	-	59	-	NC		LV	Not connected
29	54	43	58	46	VREFTOP		OBL	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	-	55	43	ASG1		AHVSS	Analog Shield Ground 1
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	-	52	40	ASG2		AHVSS	Analog Shield Ground 2
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right
37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	-	49	37	ASG4		AHVSS	Analog Shield Ground 4
39	44	-	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	-	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	-	-	46	-	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		OBL	Analog reference voltage
43	41	35	44	33	AHVSS		OBL	Analog ground
-	-	-	43	-	AHVSS		OBL	Analog ground
-	-	-	42	-	NC		LV	Not connected
-	-	-	41	-	NC		LV	Not connected
44	40	34	40	32	CAPL_M		OBL	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		OBL	Analog power supply 8V
46	38	32	38	30	CAPL_A		OBL	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF1		OBL	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	-	-	32	-	NC		LV	Not connected
53	32	-	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output

| 55	30	-	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		OBL	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
-	-	-	23	-	NC		LV	Not connected
-	-	-	22	-	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	OBL	Power-on-reset
62	23	-	20	15	NC		LV	Not connected
63	22	-	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I^{2}S2-data input
66	19	17	16	11	DVSS		OBL	Digital ground
-	-	-	15	-	DVSS		OBL	Digital ground
-	-	-	14	-	DVSS		OBL	Digital ground
67	18	16	13	10	DVSUP		OBL	Digital power supply 5V
-	-	-	12	-	DVSUP		OBL	Digital power supply 5V
-	-	-	11	-	DVSUP		OBL	Digital power supply 5V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

11.18. M29W040B

11.18.1. Description

The M29W040B is a 4 Mbit (512Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM. The M29W040B is fully backward compatible with the M29W040.The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are writ-ten to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards. Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

11.18.2. Features

• SINGLE 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
• ACCESS TIME: 55ns
• PROGRAMMING TIME
      - 10µs per Byte typical8
• UNIFORM 64 Kbytes MEMORY BLOCKS
• PROGRAM/ERASE CONTROLLER
      - Embedded Byte Program algorithm
      - Embedded Multi-Block/Chip Erase algorithm
      - Status Register Polling and Toggle Bits
• ERASE SUSPEND and RESUME MODES
      - Read and Program another Block during Erase Suspend
• UNLOCK BYPASS PROGRAM COMMAND
      - Faster Production/Batch Programming
• LOW POWER CONSUMPTION
      - Standby and Automatic Standby
• 100,000 PROGRAM/ERASE CYCLES per BLOCK
• 20 YEARS DATA RETENTION
      - Defectivity below 1 ppm/year
• ELECTRONIC SIGNATURE
      - Manufacturer Code: 20h
      - Device Code: E3h

11.18.3.   Pin Descriptions
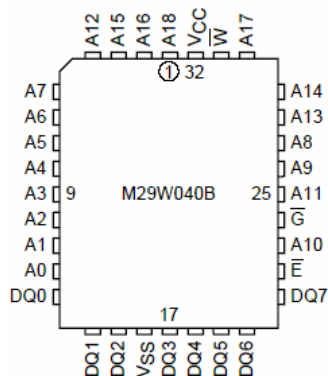
| A0-A18	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

11.19. MC33202

11.19.1.   General Description

The MC33201/2/4 family of operational amplifiers provide rail−to−rail operation on both the input and output. The inputs can be driven as high as 200mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail−to−rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (±0.9 V) yet can operate with a supply of up to +12V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

11.19.2.   Features

• Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
• Input Voltage Range Includes both Supply Rails
• Output Voltage Swings within 50 mV of both Rails
• No Phase Reversal on the Output for Over−driven Input Signals
• High Output Current (ISC = 80 mA, Typ)
• Low Supply Current (ID = 0.9 mA, Typ)
• 600 Ω Output Drive Capability
• Extended Operating Temperature Ranges (−40° to +105°C and −55° to +125°C)
• Typical Gain Bandwidth Product = 2.2 MHz
• Pb−Free Packages are Available

11.19.3.   Pin Connections
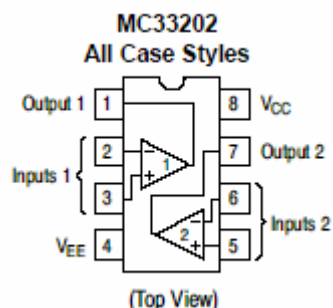
11.20. PCF8574

11.20.1.   General Description

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I^2C).The device consists of an 8-bit quasi-bidirectional port and an I^2C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

11.20.2.   Features

• Operating supply voltage 2.5 to 6V
• Low standby current consumption of 10 µA maximum
• I^2C to parallel port expander
• Open-drain interrupt output
• 8-bit remote I/O port for the I^2C-bus
• Compatible with most microcontrollers
• Latched outputs with high current drive capability for directly driving LEDs
• Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
• DIP16, or space-saving SO16 or SSOP20 packages.

11.20.3.   Pinning
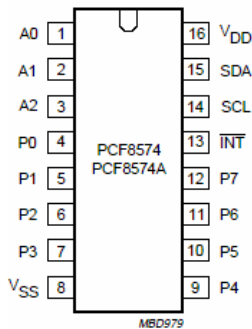
SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

11.21. PI5V330

11.21.1. General Description

The PI5V330 is well suited for video applications when switching composite or RGB analogue. A picture-in-picture application will be described in this brief. The pixel-rate creates video overlays so two or more pictures can be viewed at the same time. An inexpensive NTSC titler can be implemented by superimposing the output of a character generator on a standard composite video background.

11.22. SDA55XX (SDA5550)

11.22.1. General description

The SDA55XX is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device also supports Closed caption acquisition and decoding. The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to16 Kbytes. Device has an internal ROM of up to 128 KBytes. ROMless versions can access up to 1 MByte of external RAM and ROM. The SDA 55XX supports a wide range of standards including PAL, NTSC and contains a digital slicer for VPS, WSS, PDC, TTX and Closed Caption, an accelerating acquisition hardware module, a display generator for Level 1.5 TTX data and powerful On screen Display capabilities based on parallel attributes, and Pixel oriented characters (DRCS).
The 8-bit Microcontroller runs at 360 ns. cycle time (min.). Controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface and receives/ transmits data via I^{2}C-firmware user-interface. The slicer combined with dedicated hardware stores TTX data in a VBI buffer of 1 Kilobyte. The Microcontroller firmware performs all the acquisition tasks (hamming and parity-checks, page search and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26-handling, FLOF, TOP and list-pages. The interface to user software is optimized for minimal overhead. SDA 55XX is realized in 0.25 micron technology with 2.5 V supply voltage and 3.3 V I/O (TTL compatible). The software and hardware development environment (TEAM) is available to simplify and speed up the development of the software and On Screen Display. TEAM stands for TVT Expert Application Maker. It improves the TV controller software quality in following aspects:
– Shorter time to market
– Re-usability
– Target independent development
– Verification and validation before targeting
– General test concept
– Graphical interface design requiring minimum programming and controller know how.
– Modular and open tool chain, configurable by customer.

11.23. Sil 9993

11.23.1. General Description

The Sil 9993 is the first generation of PanelLink receivers that are designed for the HDMI 1.0 (High Definition Multimedia Interface) specification. DTVs, plasma displays, LCD TVs and projectors can now provide the purest level of protected digital audio/video over a simple, low cost cable. Backwards compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 host (DVD players, HD set top boxes, D-VHS players and receivers, PC). The Sil 9993 incorporates a flexible audio and video interface. The receiver can connect to RGB input and output YCbCr using an integrated color space converter. This allows full backward compatibility to DVI, and interfaces to all major video processors. A S/PDIF port can output PCM encoded data as well as Dolby Digital, DTS and all other formats capable of being sent over S/PDIF. A 2-channel I2S port outputs data converted from S/PDIF. The Sil 9993 comes pre-programmed with HDCP keys, greatly simplifying the manufacturing process, lowering costs, all the while providing the highest level of HDCP key security. Silicon Image's PanelLink

receivers use the latest generation of PanelLink TMDS core technology. These PanelLink cores pass all HDMI compliancy tests.

11.23.2. Features

• HDMI 1.0 and DVI 1.0 compliant receiver
• Integrated PanelLink core supports DTV resolutions (480i/576i/480p/576p/720p/1080i)
• Digital video interface supports video processors:
  o 24-bit RGB 4:4:4
  o 24-bit YCbCr 4:4:4
  o 16/20/24-bit YCbCr 4:2:2
  o 8/10/12-bit YCbCr 4:2:2 embedded syncs
• Analog RGB and YPbPr output:
  o 10-bit DAC
  o Separate or Composite Syncs (Sync on G)
• S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-48kHz Fs) using IEC 60958 and IEC 61937.
• Programmable I^2S interface for connection to low-cost audio DACs.
• Integrated HDCP decryption engine for receiving protected audio and video content
• Pre-programmed HDCP keys provide highest level of key security, simplifies manufacturing
• Programmable registers via slave I^2C interface
• 3.3V operation in 100-pin TQFP package
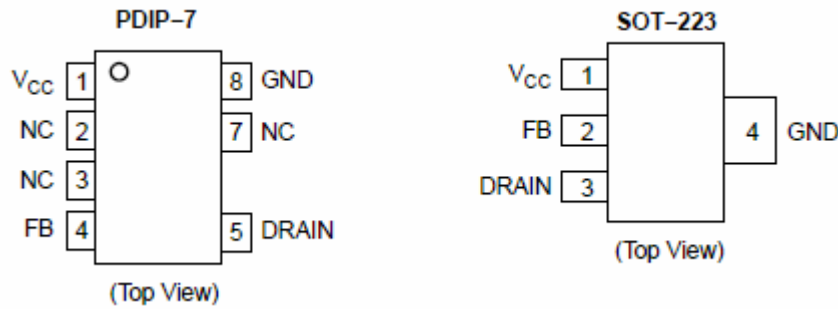• Flexible power management

11.24. NCP1014

11.24.1. General Description

The NCP101X series integrates a fixed−frequency current−modecontroller and a 700 V MOSFET. Housed in a PDIP−7 or SOT−223package, the NCP101X offers everything needed to build a rugged and low−cost power supply, including soft−start, frequency jittering, short−circuit protection, skip−cycle, a maximum peak current setpoint and a Dynamic Self−Supply (no need for an auxiliary winding). Unlike other monolithic solutions, the NCP101X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65−100−130 kHz). When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at typically 1/4 of the maximum peak value, no acoustic noise takes place. As a result, standby power is reduced to the minimum without acoustic noise generation. Short−circuit detection takes place when the feedback signal fades away, e.g. in true short−circuit conditions or in broken Optocoupler cases. External disabling is easily done either simply by pulling the feedback pin down or latching it to ground through an inexpensive SCR for complete latched−off. Finally soft−start and frequency jittering further ease the designer task to quickly develop low−cost and robust offline power supplies. For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to consume less than100 mW at high line. In this mode, a built−in latched overvoltage protection prevents from lethal voltage runaways in case the Optocoupler would brake.

11.24.2. Features

• Built−in 700 V MOSFET with Typical R_{DSon} of 11 Ω and 22 Ω
• Large Creepage Distance Between High−Voltage Pins
• Current−Mode Fixed Frequency Operation: 65 kHz–100 kHz−130 kHz
• Skip−Cycle Operation at Low Peak Currents Only: No Acoustic Noise!
• Dynamic Self−Supply, No Need for an Auxiliary Winding
• Internal 1.0 ms Soft−Start
• Latched Overvoltage Protection with Auxiliary Winding Operation
• Frequency Jittering for Better EMI Signature
• Auto−Recovery Internal Output Short−Circuit Protection
• Below 100 mW Standby Power if Auxiliary Winding is Used
• Internal Temperature Shutdown
• Direct Optocoupler Connection
• SPICE Models Available for TRANsient Analysis

11.24.3. Pin Connections and Descriptions

Pin No. (SOT−223)	Pin No. (PDIP−7)	Pin Name	Function	Description
1	1	V_{CC}	Powers the Internal Circuitry	This pin is connected to an external capacitor of typically 10 μF. The natural ripple superimposed on the V_{CC} participates to the frequency jittering. For improved standby performance, an auxiliary V_{CC} can be connected to Pin 1. The V_{CC} also includes an active shunt which serves as an opto−fail−safe protection.
−	2	NC	−	−
−	3	NC	−	−
2	4	FB	Feedback Signal Input	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	5	Drain	Drain Connection	The internal drain MOSFET connection.
−	−	−	−	−
−	7	NC	−	This unconnected pin ensures adequate creepage distance.
4	8	GND	The IC Ground	−

11.25. SN74CB3Q3305

11.25.1. General Description

The SN74CB3Q3305 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

11.25.2. Features

• High-Bandwidth Data Path (Up To 500 MHz)
• 5-V Tolerant I/Os with Device Powered-Up or Powered-Down
• Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typical)
• Rail-to-Rail Switching on Data I/O Ports
    − 0- to 5-V Switching With 3.3-V VCC
    − 0- to 3.3-V Switching With 2.5-V VCC
• Bidirectional Data Flow, With Near-Zero Propagation Delay
• Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)
• Fast Switching Frequency (f_{OE} = 20 MHz Max)
• Data and Control Inputs Provide Undershoot Clamp Diodes
• Low Power Consumption (ICC = 0.25 mA Typical)
• VCC Operating Range From 2.3 V to 3.6 V
• Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
• Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
• I_{off} Supports Partial-Power-Down Mode Operation
• Latch-Up Performance Exceeds 100 mA PerJESD 78, Class II
• ESD Performance Tested Per JESD 22
    − 2000-V Human-Body Model (A114-B, Class II)

− 1000-V Charged-Device Model (C101)

• Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

11.25.3. Pin Connections

PW PACKAGE
(TOP VIEW)

1OE 1 — 8 V$_{CC}$
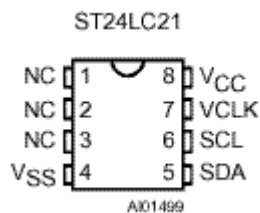1A 2 — 7 2OE
1B 3 — 6 2B
GND 4 — 5 2A
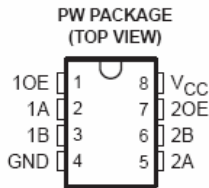
11.26. ST24LC21

11.26.1. Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I^{2}C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I^{2}C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 can not switch from the I^{2}C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.
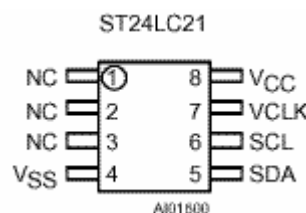
11.26.2. Features

• 1 million Erase/Write cycles
• 40 years data retention
• 2.5V to 5.5V single supply voltage
• 400k Hz compatibility over the full range of supply voltage
• Two wire serial interface I^{2}C bus compatible
• Page Write (Up To 8 Bytes)
• Byte, random and sequential read modes
• Self timed programming cycle
• Automatic address incrementing
• Enhanced ESD/Latch up
• Performances

11.26.3. Pin connections

ST24LC21

NC 1 — 8 V$_{CC}$
NC 2 — 7 VCLK
NC 3 — 6 SCL
V$_{SS}$ 4 — 5 SDA

AI01499

ST24LC21

NC 1 — 8 V$_{CC}$
NC 2 — 7 VCLK
NC 3 — 6 SCL
V$_{SS}$ 4 — 5 SDA

AI01800

DIP Pin connections   CO Pin connections

NC: Not connected

Signal names

SDA	Serial data Address Input/Output
SCL	Serial Clock (I^{2}C mode)
V$_{cc}$	Supply voltage
V$_{ss}$	Ground
VCLK	Clock transmit only mode

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11.27. LM2576

11.27.1. General Description

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step–down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0 A load with excellent line and load regulation.

These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version. These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2576 are offered by several different inductor manufacturers.

Since the LM2576 converter is a switch–mode power supply, its efficiency is significantly higher in comparison with popular three–terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated is so low that no heatsink is required or its size could be reduced dramatically.
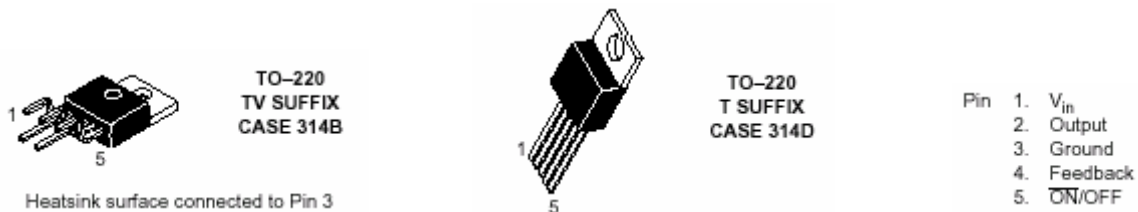
A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch–mode power supplies.

The LM2576 features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency (±2% over 0°C to 125°C). External shutdown is included, featuring 80 mA (typical) standby current. The output switch includes cycle–by–cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

11.27.2. Features

• 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
• Adjustable Version Output Voltage Range, 1.23 to 37 V ±4% Maximum Over Line and Load Conditions
• Guaranteed 3.0 A Output Current
• Wide Input Voltage Range
• Requires Only 4 External Components
• 52 kHz Fixed Frequency Internal Oscillator
• TTL Shutdown Capability, Low Power Standby Mode
• High Efficiency
• Uses Readily Available Standard Inductors
• Thermal Shutdown and Current Limit Protection
• Moisture Sensitivity Level (MSL) Equals 1

11.27.3. Pin description

TO–220
TV SUFFIX
CASE 314B

Heatsink surface connected to Pin 3

TO–220
T SUFFIX
CASE 314D

Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. $\overline{ON}$/OFF

11.28. TDA1308

11.28.1. General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

11.28.2. Features

• Wide temperature range
• No switch ON/OFF clicks
• Excellent power supply ripple rejection
• Low power consumption

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- Short-circuit resistant
- High performance
- high signal-to-noise ratio
- High slew rate
- Low distortion
- Large output voltage swing.

11.28.3. Pinning

SYMBOL	PIN	DESCRIPTION	PIN VALUE
OUTA	1	Output A (Voltage swing)	Min : 0.75V, Max : 4.25V
INA(neg)	2	Inverting input A	Vo(clip) : Min : 1400mVrms
INA(pos)	3	Non-inverting input A	2.5V
V_{SS}	4	Negative supply	0V
INB(pos)	5	Non-inverting input B	2.5V
INB(neg)	6	Inverting input B	Vo(clip) : Min : 1400mVrms
OUTB	7	Output B (Voltage swing)	Min : 0.75V, Max : 4.25V
V_{DD}	8	Positive supply	5V, Min : 3.0V, Max : 7.0V

11.29. TDA9886

11.29.1. General Description

The TDA9886 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL.

11.29.2. Features

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
- Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L/L accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I^2C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analogue converter; AFC bits via I^2C -bus readable
- TakeOver Point (TOP) adjustable via I^2C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)
- SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I^2C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- I^2C-bus control for all functions
- I^2C-bus transceiver with pin programmable Module Address (MAD).

11.29.3. Pinning

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
OP1	3	output 1 (open-collector)
FMPLL	4	FM-PLL for loop filter

DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP)
SDA	10	I²C-bus data input/output
SCL	11	I²C-bus clock input
SIOMA	12	sound intercarrier output and MAD select
n.c.	13	not connected
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
VAGC	16	VIF-AGC for capacitor; note 1
CVBS	17	video output
AGND	18	analog ground
VPLL	19	VIF-PLL for loop filter
V_P	20	supply voltage (+5 V)
AFC	21	AFC output
OP2	22	output 2 (open-collector)
SIF1	23	SIF differential input 1
SIF2	24	SIF differential input 2

11.30. TPA3002D2

11.30.1. General Description

The TPA3002D2 is a 9-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3002D2 can drive stereo speakers as low as 8 O. The high efficiency of the TPA3002D2 eliminates the need for external heatsinks when playing music.

Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from -40 dB to 36 dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from -56 dB to 20 dB.

An integrated 5-V regulated supply is provided for powering an external headphone amplifier.

11.30.2. Features

- 9-W/Ch into an 8-Q Load from 12-V Supply
- Efficient, Class-D Operation Eliminates Heatsinks and Reduces Power Supply Requirements
- 32-Step DC Volume Control From -40 dB to 36 dB
- Line Outputs for External Headphone Amplifier with Volume Control
- Regulated 5-V Supply Output for Powering TPA6110A2
- Space-Saving, Thermally-Enhanced PowerPAD™ Packaging
- Thermal and Short-Circuit Protection

Applications
- LCD Monitors and TVs
- Powered Speakers

11.30.3.   Pinning
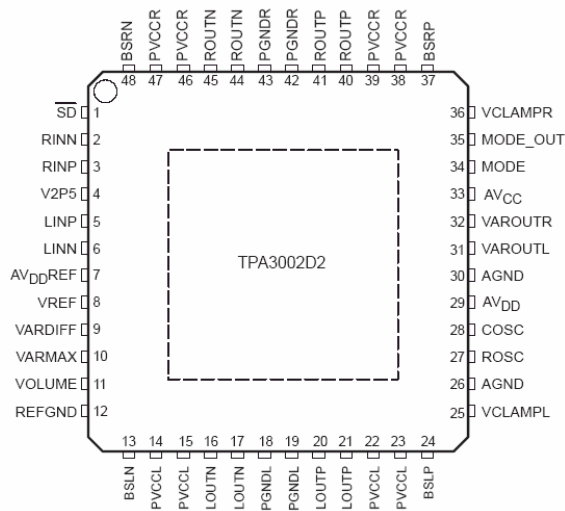
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
AGND	26, 30	-	Analog ground for digital/analog cells in core
AV$_{CC}$	33	-	High-voltage analog power supply (8.5 V to 14 V)
AV$_{DD}$	29	O	5-V Regulated output capable of 100-mA output
AV$_{DD}$REF	7	O	5-V Reference output—provided for connection to adjacent VREF terminal.
BSLN	13	I/O	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	I/O	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	I/O	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	I/O	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
LINN	6	I	Negative differential audio input for left channel
LINP	5	I	Positive differential audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
MODE	34	I	Input for MODE control. A logic high on this pin places the amplifier in the variable output mode and the Class-D outputs are disabled. A logic low on this pin places the amplifier in the Class-D mode and Class-D stereo outputs are enabled. Variable outputs (VAROUTL and VAROUTR) are still enabled in Class-D mode to be used as line-level outputs for external amplifiers.
MODE_OUT	35	O	Output for control of the variable output amplifiers. When the MODE pin (34) is a logic high, the MODE_OUT pin is driven low. When the MODE pin (34) is a logic low, the MODE_OUT pin is driven high. This pin is intended for MUTE control of an external headphone amplifier. Leave unconnected when not used for headphone amplifier control.
PGNDL	18, 19	-	Power ground for left channel H-bridge
PGNDR	42, 43	-	Power ground for right channel H-bridge
PVCCL	14, 15	-	Power supply for left channel H-bridge (tied to pins 22 and 23 internally), not connected to PVCCR or AVC$_C$.
PVCCL	22, 23	-	Power supply for left channel H-bridge (tied to pins 14 and 15 internally), not connected to PVCCR or AVC$_C$.
PVCCR	38,39	-	Power supply for right channel H-bridge (tied to pins 46 and 47 internally), not connected to PVCCL or AVC$_C$.
PVCCR	46, 47	-	Power supply for right channel H-bridge (tied to pins 38 and 39 internally), not connected to PVCCL or AVC$_C$.
REFGND	12	—	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.

RINP	3	I	Positive differential audio input for right channel
RINN	2	I	Negative differential audio input for right channel
ROSC	27	I/O	Current setting resistor for ramp generator. Nominally equal to 1/8*VCC
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
SD	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to VCC.
VARDIFF	9	I	DC voltage to set the difference in gain between the Class-D and VAROUT outputs. Connect to GND or AVDDREF if VAROUT outputs are unconnected.
VARMAX	10	I	DC voltage that sets the maximum gain for the VAROUT outputs. Connect to GND or AVDDREF if VAROUT outputs are unconnected.
VAROUTL	31	O	Variable output for left channel audio. Line level output for driving external HP amplifier.
VAROUTR	32	O	Variable output for right channel audio. Line level output for driving external HP amplifier.
VCLAMPL	25	-	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	-	Internally generated voltage supply for right channel bootstrap capacitors.
VOLUME	11	I	DC voltage that sets the gain of the Class-D and VAROUT outputs.
VREF	8	I	Analog reference for gain control section.
V2P5	4	O	2.5-V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
— Thermal Pad		-	Connect to AGND and PGND—should be center point for both grounds.

11.31. µPA672T

11.31.1. General Description

The µPA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

11.31.2. Features

• Two MOS FET circuits in package the same size as SC-70
• Automatic mounting supported

11.31.3. Pin Connection

1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)
Marking: MA
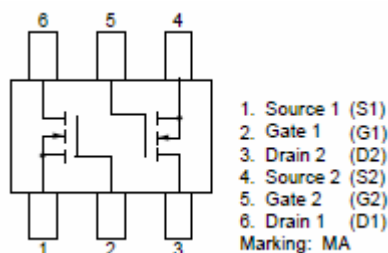
11.32. VPC3230D

11.32.1. General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are
• high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
• multi-standard colour decoder PAL/NTSC/SECAM including all substandards
• four CVBS, one S-VHS input, one CVBS output
• two RGB/YCr Cb component inputs, one Fast Blank (FB) input
• integrated high-quality A/D converters and associated clamp and AGC circuits

• multi-standard sync processing
• linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panorama-vision'
• PAL+ preprocessing
• line-locked clock, data and sync, or 656-output interface
• peaking, contrast, brightness, color saturation and tint for RGB/ YC $_r$ C $_b$ and CVBS/ S-VHS
• high-quality soft mixer controlled by Fast Blank
• PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
• 15 predefined PIP display configurations and expert mode (fully programmable)
• control interface for external field memory
• I^{2}C-bus interface
• one 20.25-MHz crystal, few external components
• 80-pin PQFP package

11.32.2.   Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input
3	R1/CR1IN	IN	VREF	Read1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Read2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND$_F$
8	FFRSTWIN	IN	LV or GND$_D$	FIFO Reset Write Input
9	V$_{SUPCAP}$	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V$_{SUPD}$	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND$_D$	SUPPLYD	X	Ground, Digital Circuitry
12	GND$_{CAP}$	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^{2}C Bus Clock
14	SDA	IN/OUT	X	I^{2}C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND$_D$	Test Pin, connect to GND$_D$
17	VGAV	IN	GND$_D$	VGAV Input
18	YCOEQ	IN	GND$_D$	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock output 20.25 MHz
25	GND$_{PA}$	OUT	X	Pad Decoupling Circuitry GND
26	V$_{SUPPA}$	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V$_{SUPLLC}$	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND$_{LLC}$	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND$_Y$	Picture Bus Luma (MSB)
32	Y6	OUT	GND$_Y$	Picture Bus Luma
33	Y5	OUT	GND$_Y$	Picture Bus Luma
34	Y4	OUT	GND$_Y$	Picture Bus Luma
35	GND$_Y$	SUPPLYD	X	Ground, Luma Output Circuitry
36	V$_{SUPY}$	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND$_Y$	Picture Bus Luma
38	Y2	OUT	GND$_Y$	Picture Bus Luma
39	Y1	OUT	GND$_Y$	Picture Bus Luma
40	Y0	OUT	GND$_Y$	Picture Bus Luma (LSB)
41	C7	OUT	GND$_C$	Picture Bus Chroma (MSB)

42	C6	OUT	GND$_C$	Picture Bus Chroma
43	C5	OUT	GND$_C$	Picture Bus Chroma
44	C4	OUT	GND$_C$	Picture Bus Chroma
45	V$_{SUPC}$	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND$_C$	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND$_C$	Picture Bus Chroma
48	C2	OUT	GND$_C$	Picture Bus Chroma
49	C1	OUT	GND$_C$	Picture Bus Chroma
50	C0	OUT	GND$_C$	Picture Bus Chroma (LSB)
51	GND$_{SY}$	SUPPLYD	X	Ground Sync Pad Circuitry
52	V$_{SUPSY}$	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front End/Back-End Data/Front-End Vertical Sync Output
59	V$_{STBYY}$	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
61	NC	-	LV or GND$_D$	Not Connected
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND$_F$
65	GND$_F$	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog
67	I2CSEL	IN	X	I^{2}C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND$_F$
69	V$_{SUPF}$	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV	Chroma/Analog Video 5 Input
72	VIN1	IN	VRT	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V$_{SUPAI}$	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND$_{AI}$	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND$_{AI}$

12. SERVICE MENU SETTINGS

To enter the service menu, first enter the MENU by pressing "**MENU**" button and then press the digits 4, 7, 2 and 5 respectively.

12.1. Picture Adjust

- *Source* => *All possible sources given with the chasis as a list.*
- *Mode* => *Three items as a list; NATURAL, DYNAMIC, CINEMA*
- *Colour Temp* => *Three items as a list; COOL, NORMAL, WARM*
- *Contrast* => *Slider Bar. Changing value between 0 to 63.*
- *Brightness* => *Slider Bar. Changing value between 0 to 63.*

- *Sharpness* => *Slider Bar. Changing value between 0 to 31.*
- *Colour* => *Slider Bar. Changing value between 0 to 99.*
- *R* => *Slider Bar. Changing value between 0 to 31.*
- *G* => *Slider Bar. Changing value between 0 to 31.*
- *B* => *Slider Bar. Changing value between 0 to 31.*
- *Backlight* => *Slider Bar. Changing value between 0 to 255.*

In this menu preset values for each Mode (Contrast, Brightness, Sharpness, Colour values for each Mode-NATURAL, DYNAMIC, CINEMA) and for each Colour Temp. (R, G, B values for each Colour Temp- COOL, NORMAL, WARM) are determined for each source.

12.2. SOUND1

- *Menu Subwoofe* => *If ON, Subwoofer option is available in TV set, and the item is visible in sound menu, else Subwoofer is not available.*
- *Subwoofer Level (dB)* => *This value is gain value of Subwoofer output in dB. -30...12*
- *Subwoofer Corner Freq. (x10Hz)* => *Last low frequency value that is amplified. 5...40*
- *Menu Equalizer* => *If ON, visible in sound menu, else invisible.*
- *Menu Headphone* => *If ON, visible in sound menu, else invisible.*
- *Menu Effect* => *If ON, visible in sound menu, else invisible.*
- *Menu Wide Sound* => *If ON, visible in sound menu, else invisible.*
- *Menu Dynamic Bass* => *If ON, visible in sound menu, else invisible.*
- *Menu Virtual Dolby* => *If ON, visible in sound menu, else invisible.*
- *Carrier Mute* => *If ON, in the absence of an FM carrier the output is muted, else not.*
- *Virtual Dolby Text* => *Active if VIRTUAL DOLBY is ON. According to the selection; seen in sound menu as 3D PANORAMA or VIRTUAL DOLBY.*

12.3. SOUND 2

- *AVL* => *AVL is controlled from this menu by service user. ON/OFF*
- *Menu AVL* => *If ON, AVL item is visible in sound menu, and AVL can be controlled from sound menu by normal user, else AVL is invisible to normal user.*
- *FM PRESCALE AVL ON* => *If AVL ON, set value in this item is used as prescale value for the related standard. 0...127*
- *NICAM PRESCALE AVL ON* => *If AVL ON, set value in this item is used as prescale value for the related standard. 0...127*
- *SCART PRESCALE AVL ON* => *If AVL ON, set value in this item is used as prescale value for scart outputs. 0...127*
- *SCART VOLUME AVL ON* => *If AVL ON, set value in this item is used as volume value for scart1 and scart2. 0...127*
- *FM PRESCALE AVL OFF* => *If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127*
- *NICAM PRESCALE AVL OFF* => *If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127*
- *SCART PRESCALE AVL OFF* => *If AVL OFF, set value in this item is used as prescale value for scart outputs. 0...127*
- *SCART VOLUME AVL OFF* => *If AVL OFF, set value in this item is used as volume value for scart1 and scart2. 0...127*

12.4. Options

- *Burn-In Mode* => *If ON, When TV is powered ON Green, Blue, Red is displayed in sequence until Menu button is pressed.*
- *FIRST APS* => *If ON, "First APS" menu is displayed when the TV is switched on with the factory default settings.*
- *APS Volume* => *After First APS function finishes, the volume of the TV is that value.*
- *AGC (dB)* => *Tuner AGC value.*
- *Power-Up Mode* => *Mode defines the TV set power on state.*
  - *Stand-by : When TV is ON set is in stand-by mode*
  - *Normal : When TV is ON set is in normal mode*
  - *Last State: When TV is ON set is in Last State mode*

- Factory Reset => OK to activate. When OK is pressed on this item, factory defaults loaded.
- Enter Flash Mode => Before uploading SW this mode must be selected.
- Reset Eeprom => Initialize default settings

12.5. TV Norm

- BG => If ON, supported, else not supported
- DK => If ON, supported, else not supported.
- I => If ON, supported, else not supported.
- L => If ON, supported, else not supported.
- LP => If ON, supported, else not supported.
- M => If ON, supported, else not supported.

12.6. Features

- PIP/PAP => If ON, PIP/PAP available else not.
- Blue Background => If ON, Blue Background is visible in Feature Menu else not.
- Menu Transparency => If ON, Menu Transparency is visible in Feature Menu else not.
- Menu Timeout => If ON, Menu Timeout is visible in Feature Menu else not.
- Backlight => If ON, Backlight is visible in Feature Menu else not.
- Single Tuner => If TV set has one tuner Single Tuner must be ON.
    If TV set has double tuner Single Tuner must be OFF.
- Dynamic WB => Dynamic White Balance

12.7. Teletext

- TOP TXT => If ON, Top Text feature is available else not.
- Fast TXT => If ON, Fast Text feature is available else not.
- Teletext Language => Teletext Language may be controlled from this menu by service user.
- Menu Teletext Language => If ON, Teletext Language item is visible in Feature Menu, and Teletext Language can be controlled from Feature Menu by normal user, else Teletext Language is invisible to normal user.

12.8. Source

- TV
- SC1
- SC2
- SC2 SVHS
- SC3
- SC3 SVHS
- YPBPR
- FAV
- SVHS
- HDMI
- PC

This menu is related with the options of the chassis. These items may be ON or OFF. If ON, the source is available in TV set, and the item is visible in source menu, else the source may be available but invisible to user.

12.9. Menu Languages 1 & 2

The language options for the Language item in Feature menu can be set ON or OFF from this menu.

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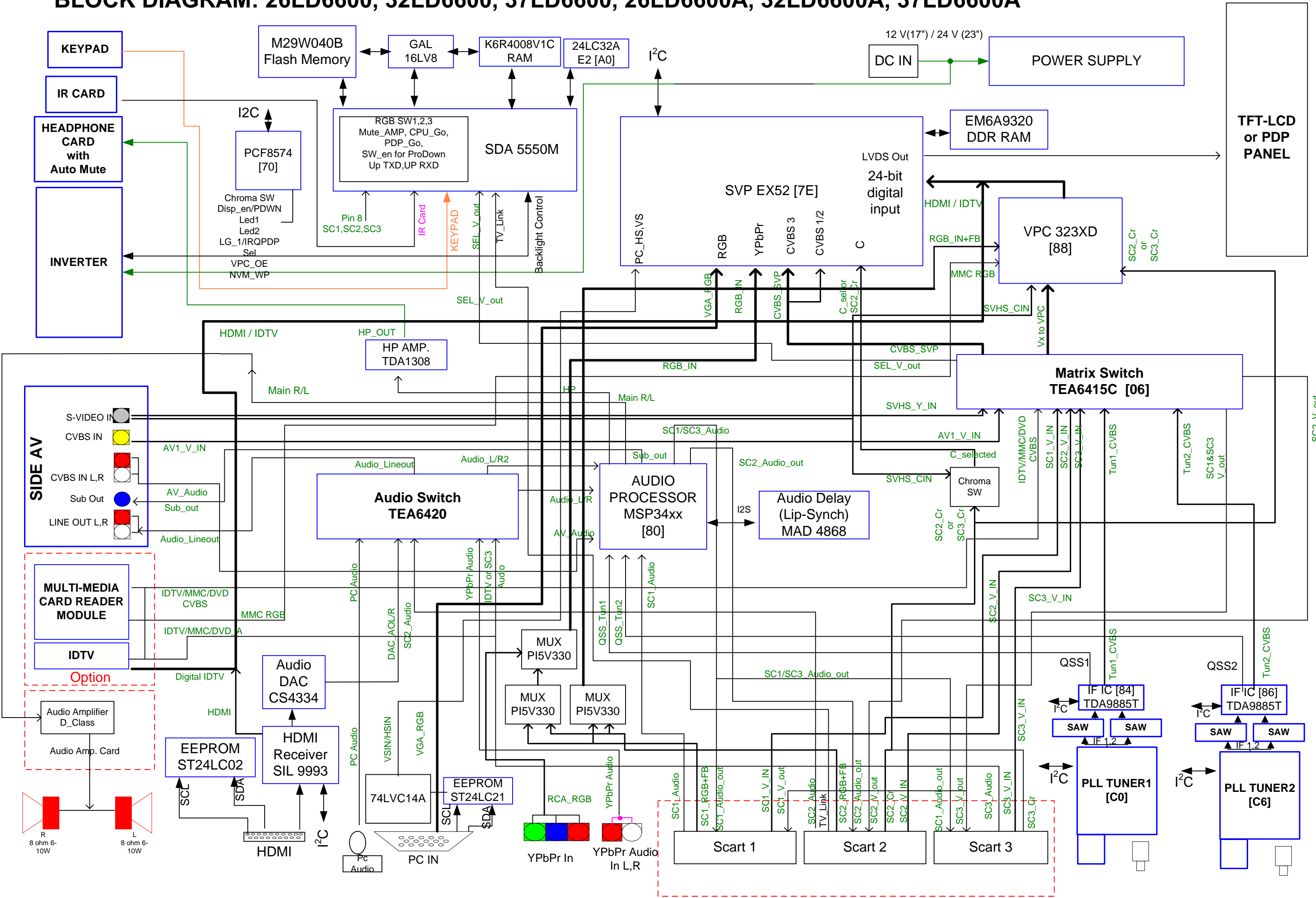
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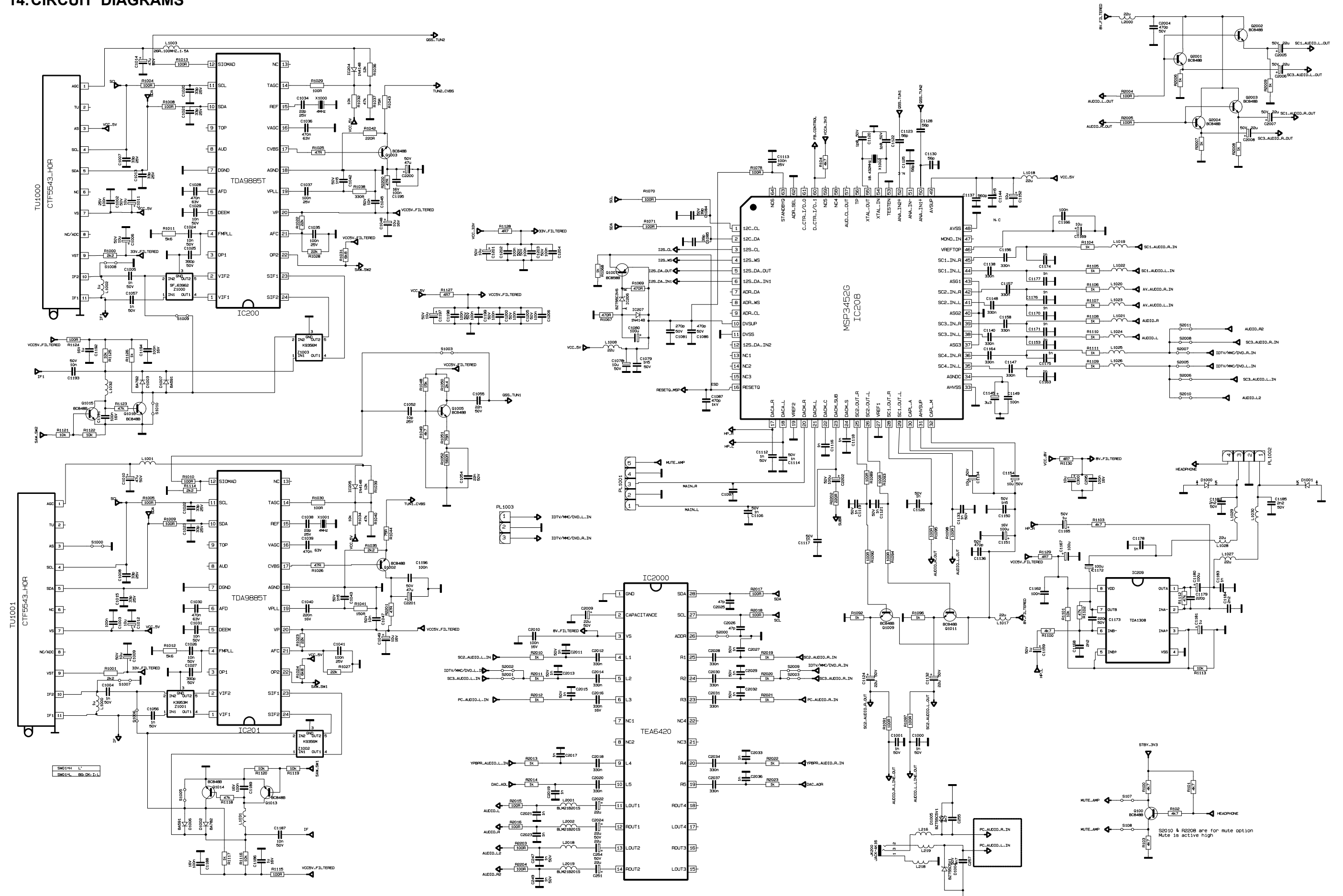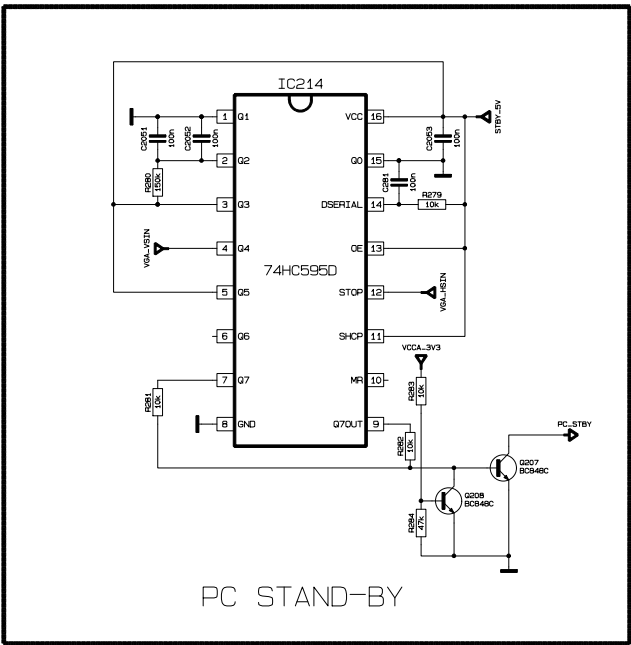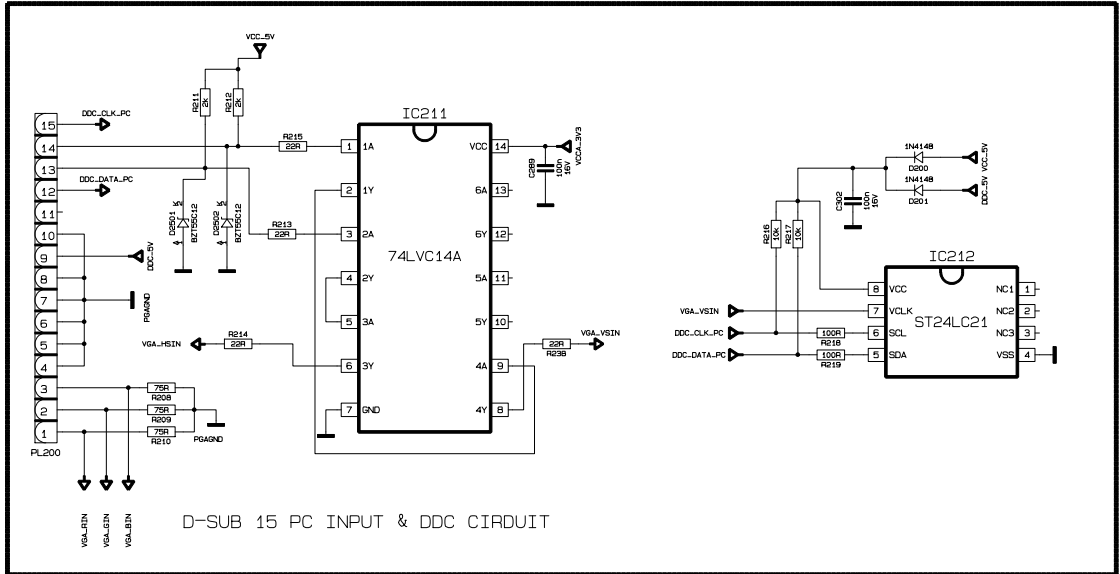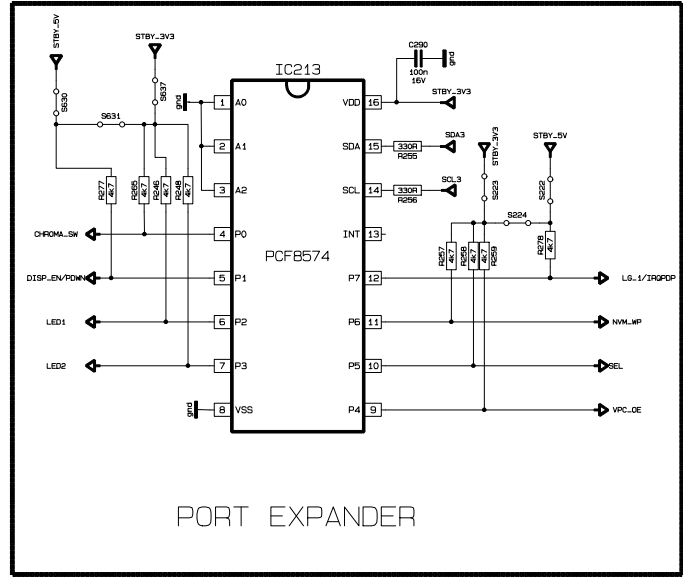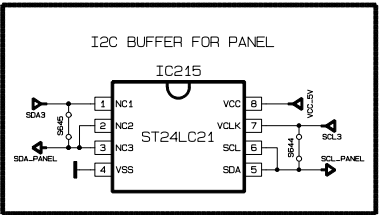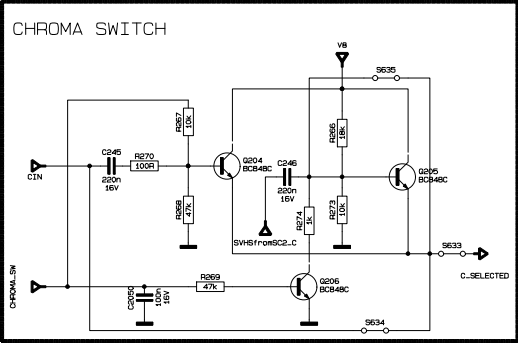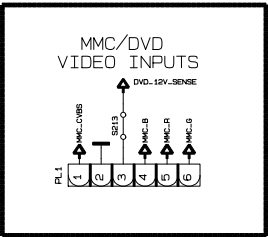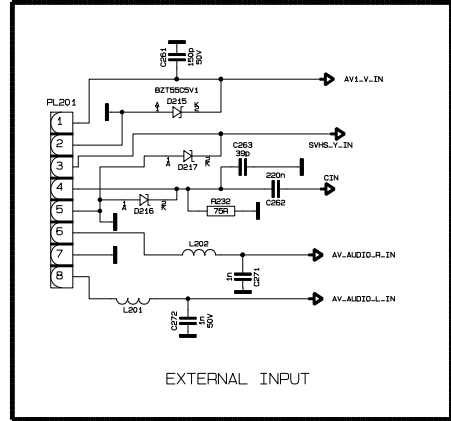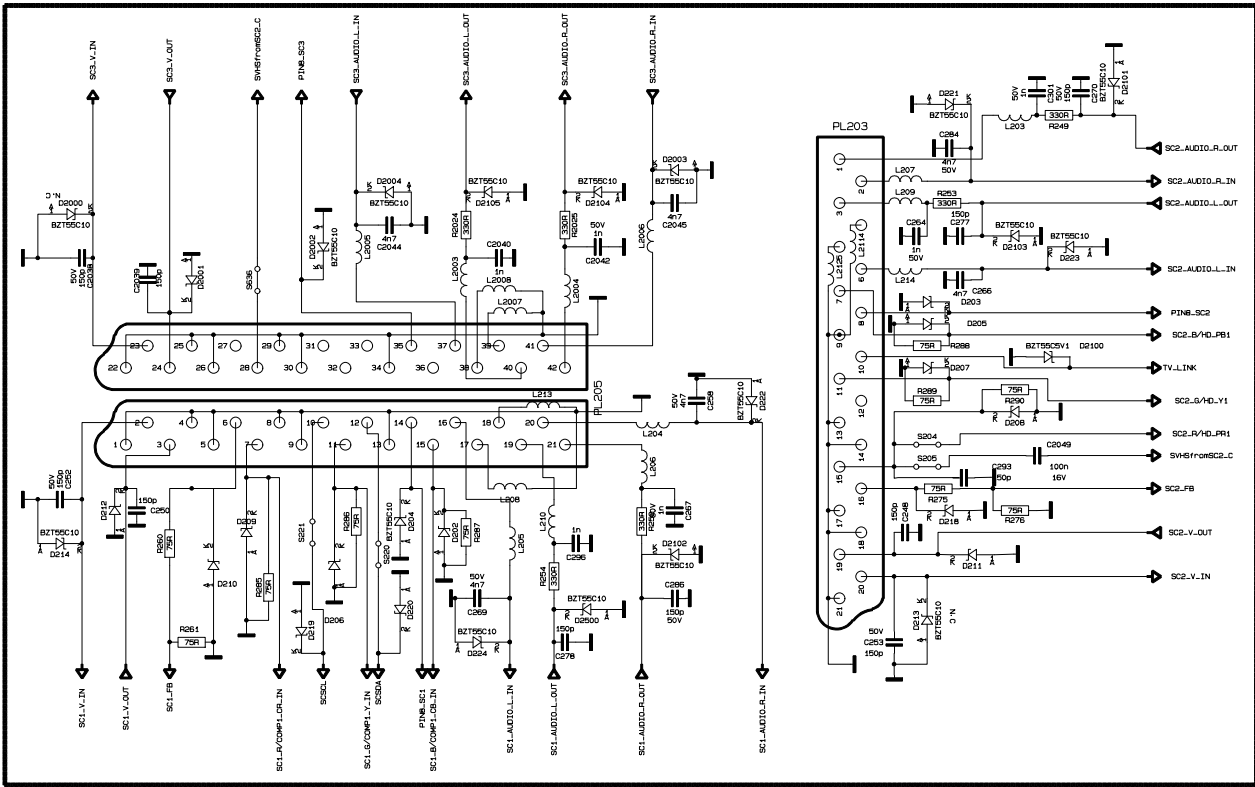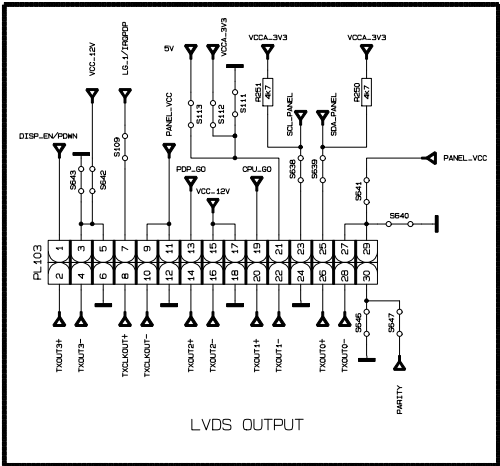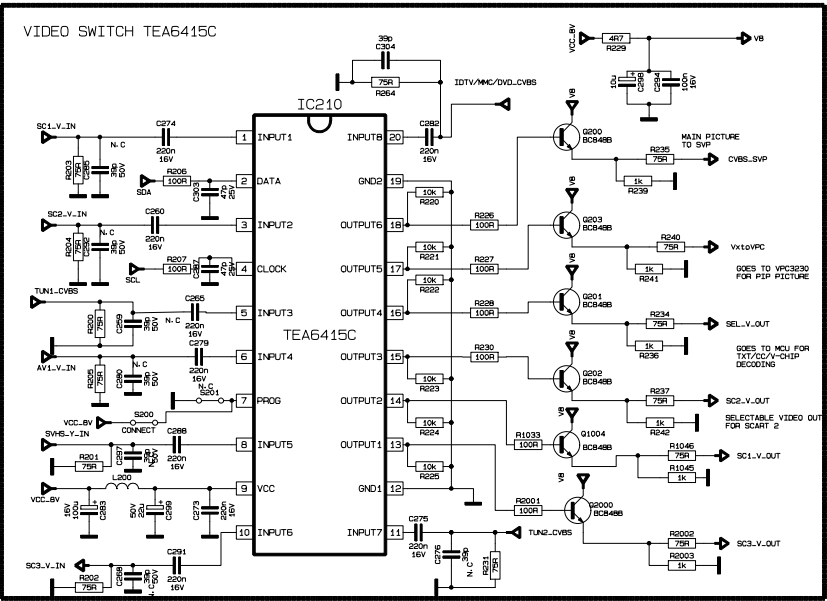
Tuner / IF / Audio

26LD6600, 32LD6600, 37LD6600, 26LD6600A, 32LD6600A, 37LD6600A

VIDEO SWITCH TEA6415C

LVDS OUTPUT

EXTERNAL INPUT

MMC/DVD VIDEO INPUTS

CHROMA SWITCH

I2C BUFFER FOR PANEL

PORT EXPANDER

D-SUB 15 PC INPUT & DDC CIRDUIT

PC STAND-BY

TV In / Out

TV VPC3230

IC107
74LX1G86STR

IC224
SVP_EX_51

PC INPUT (VGA)

MAIN PICTURE

MAIN RGB INPUT

DIGITAL IDTV INPUTS (ITU 601)

LVDS OUT

Video Decoder

26LD6600, 32LD6600, 37LD6600, 26LD6600A, 32LD6600A, 37LD6600A

41

26LD6600, 32LD6600, 37LD6600, 26LD6600A, 32LD6600A, 37LD6600A, 32LD6600B
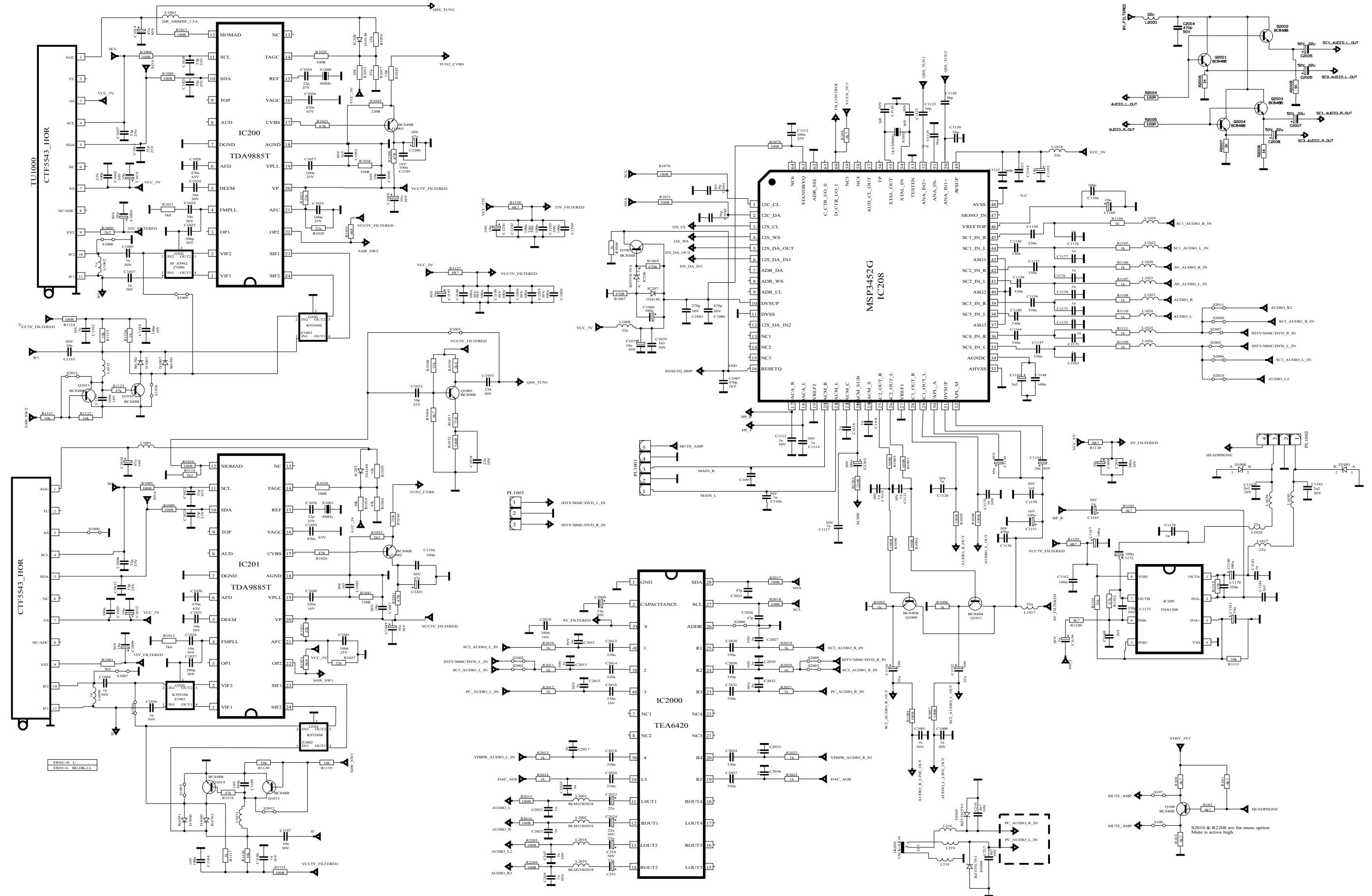

DDR RAM

TV MCU Interface

HDMI / DAC
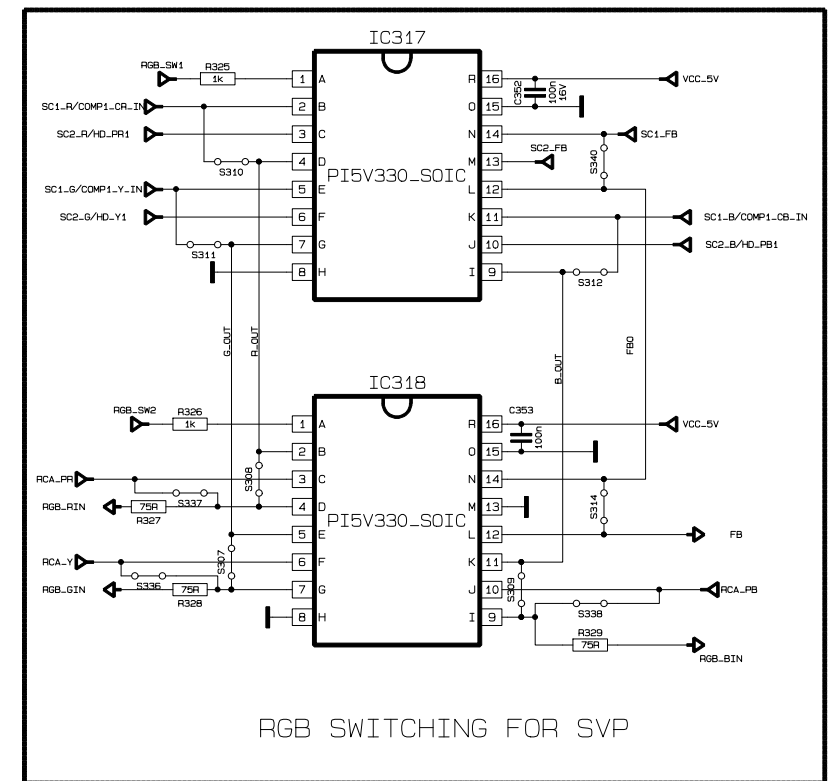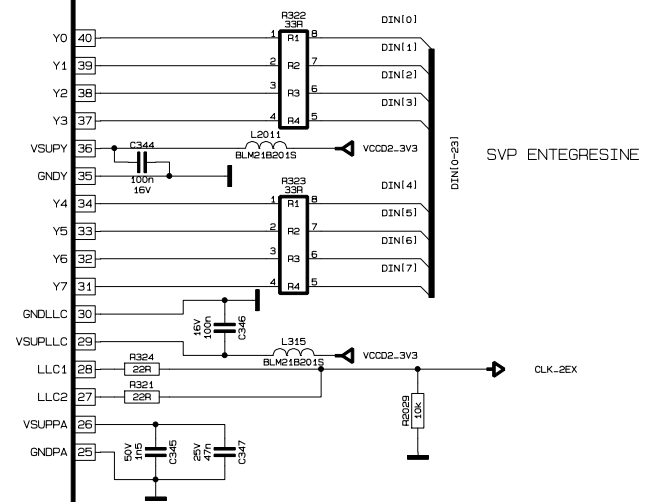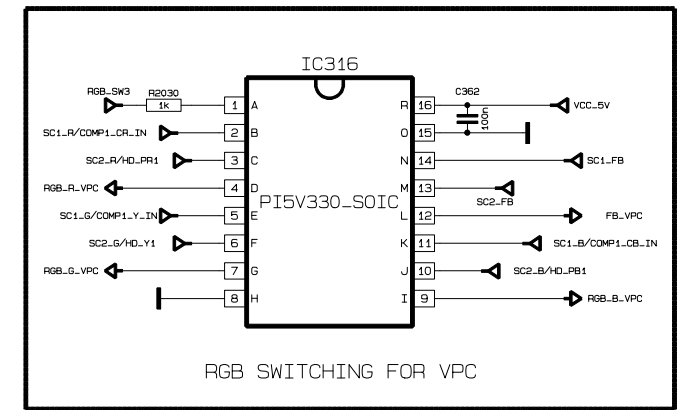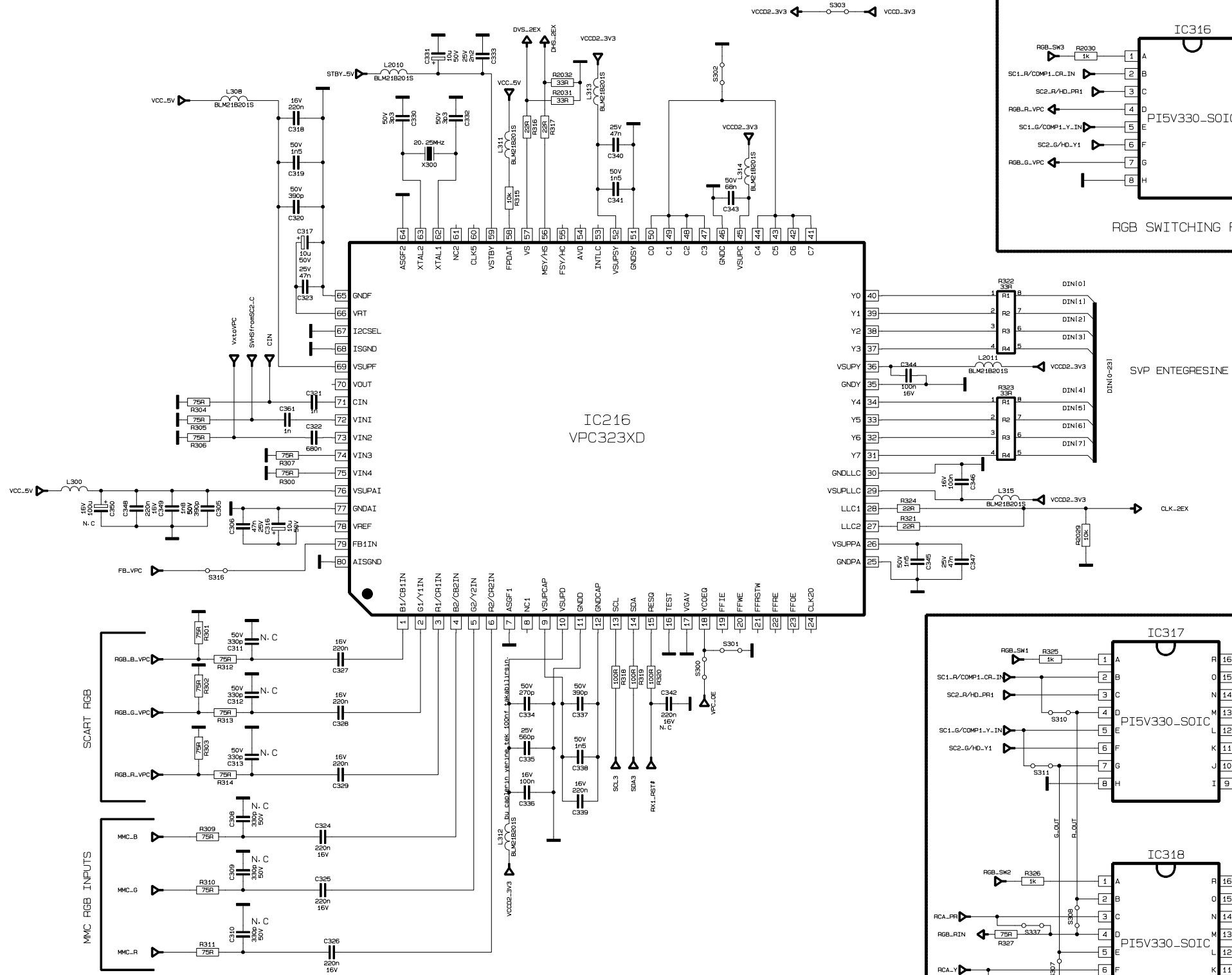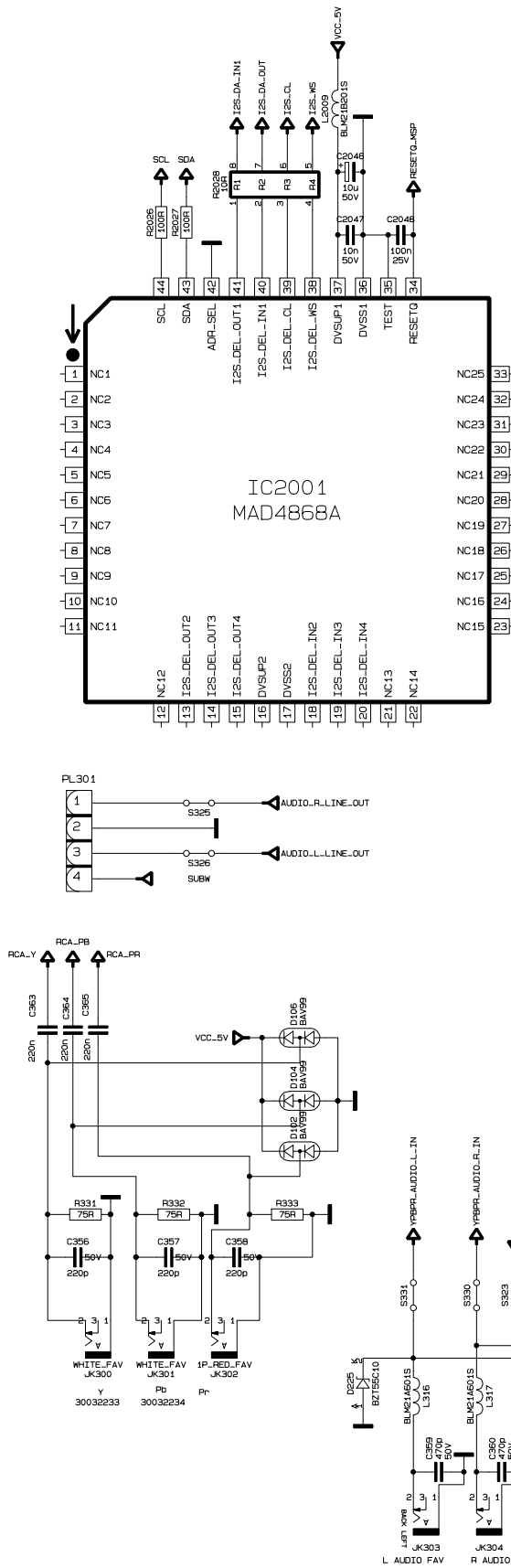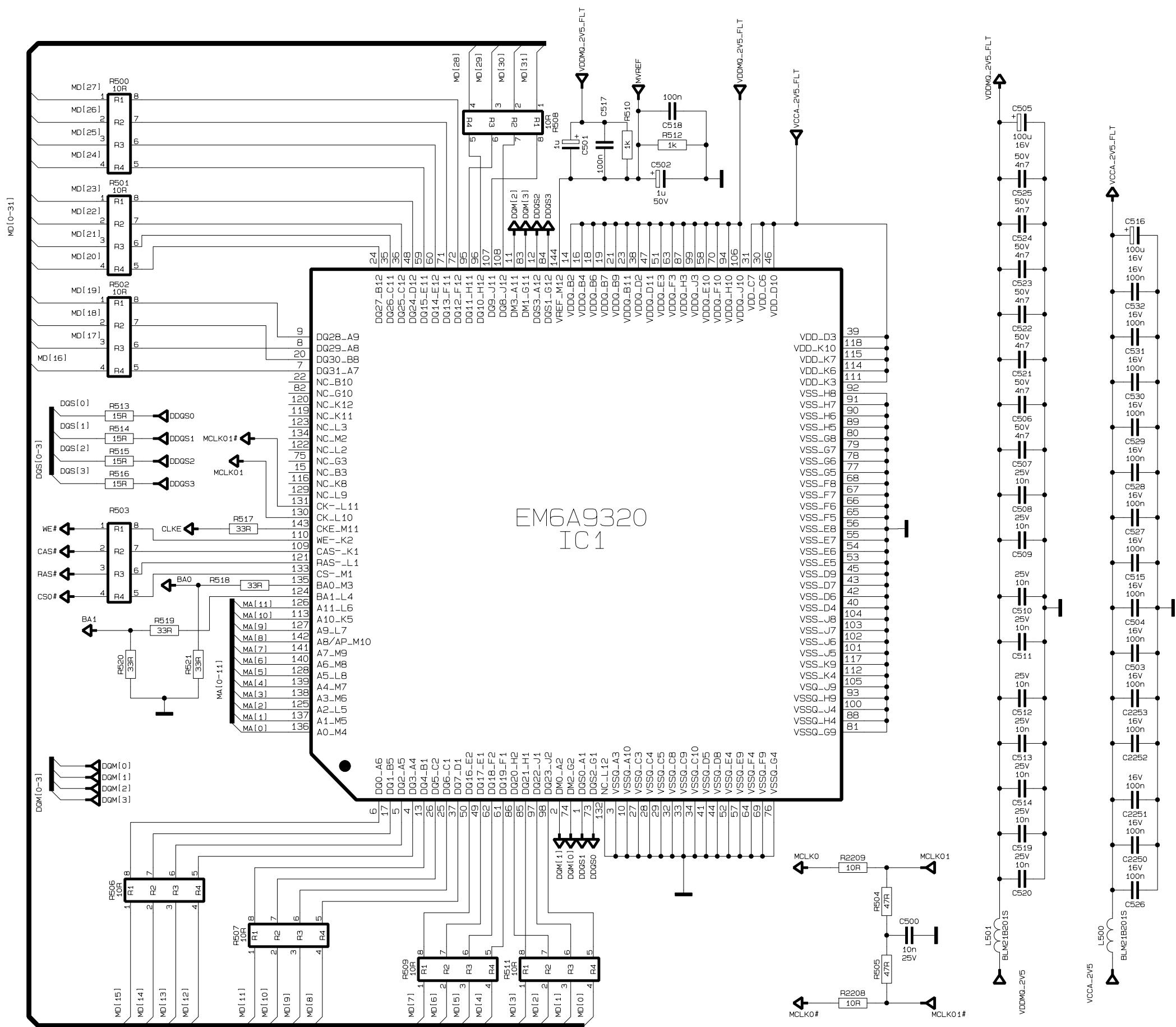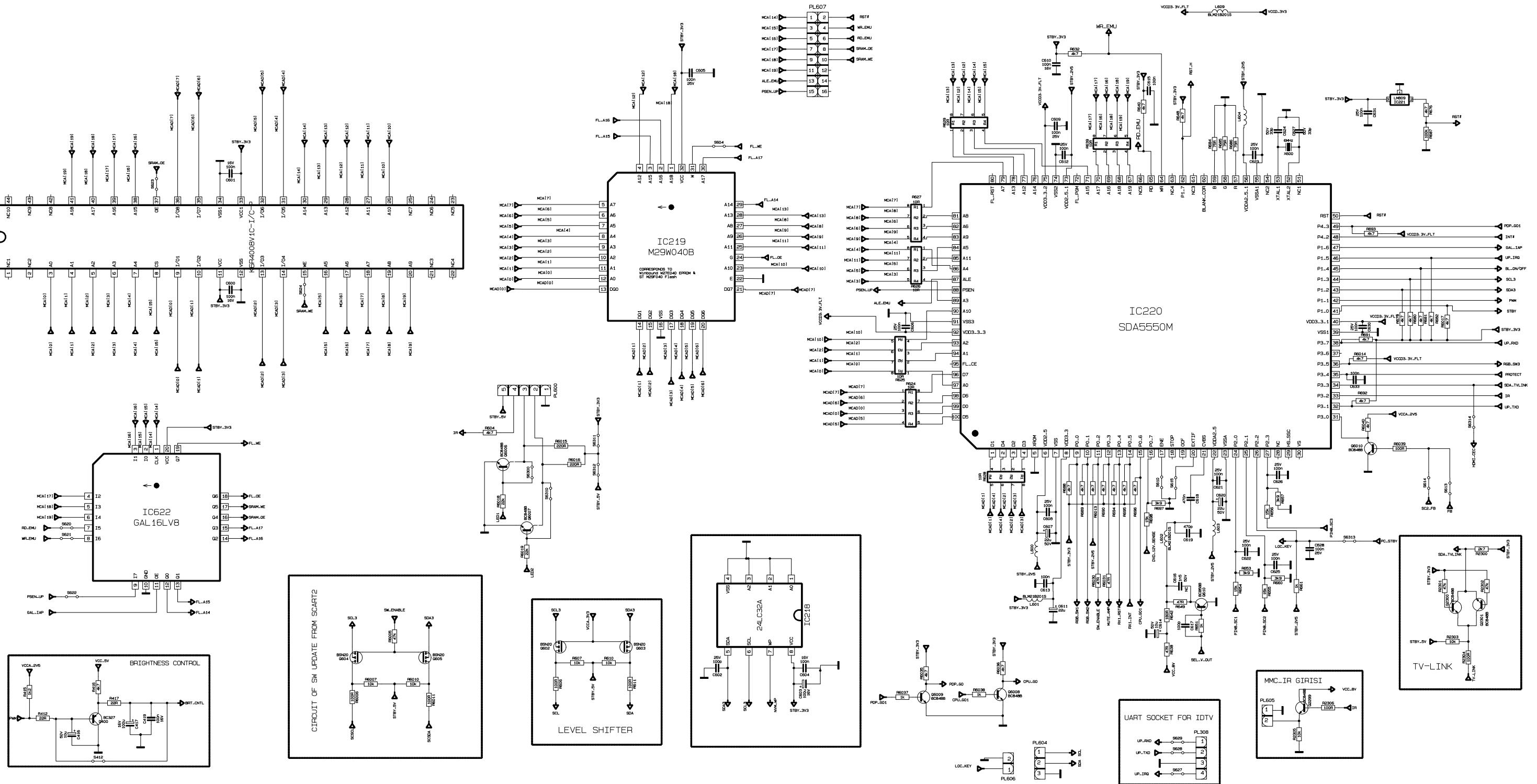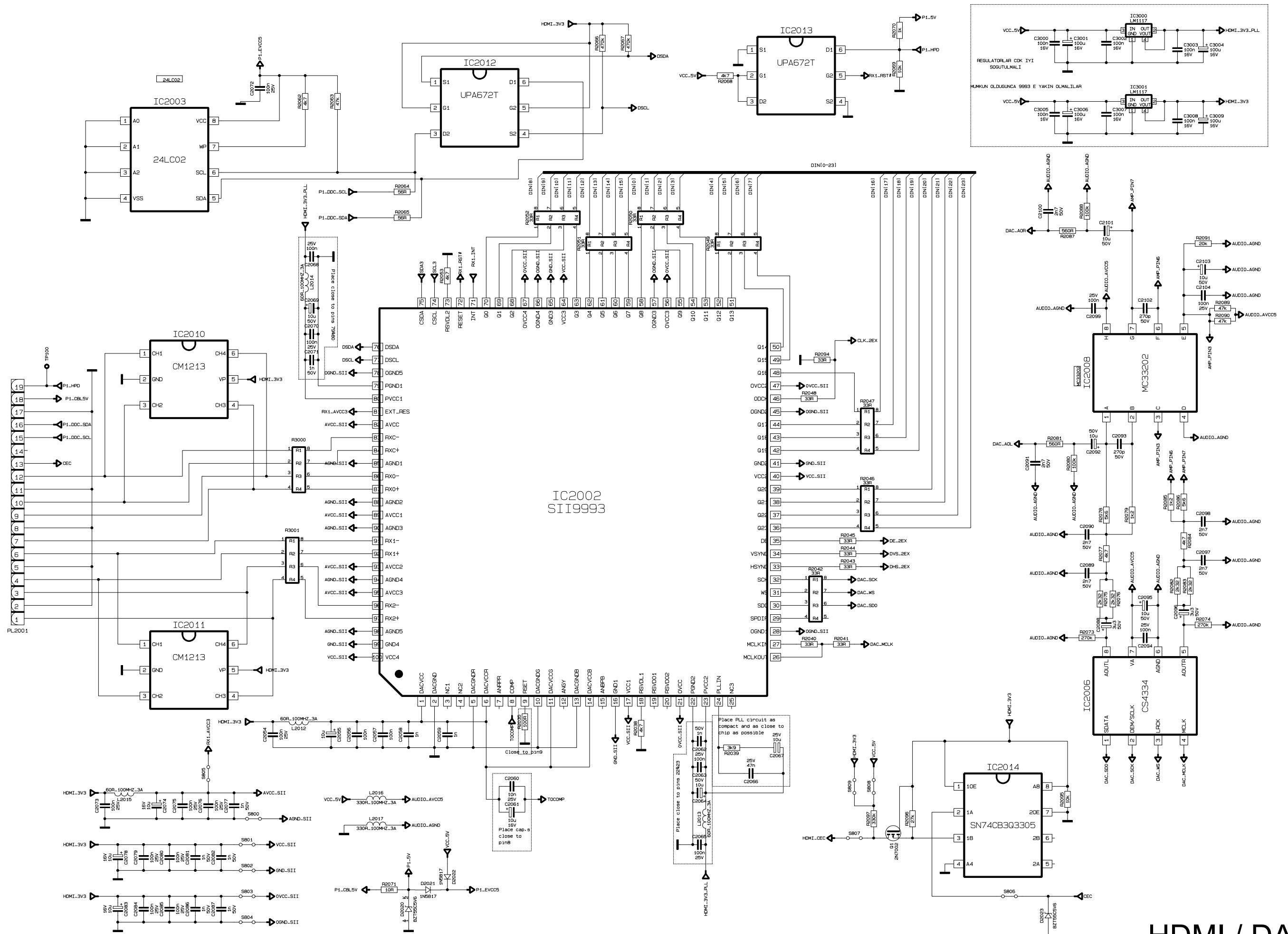
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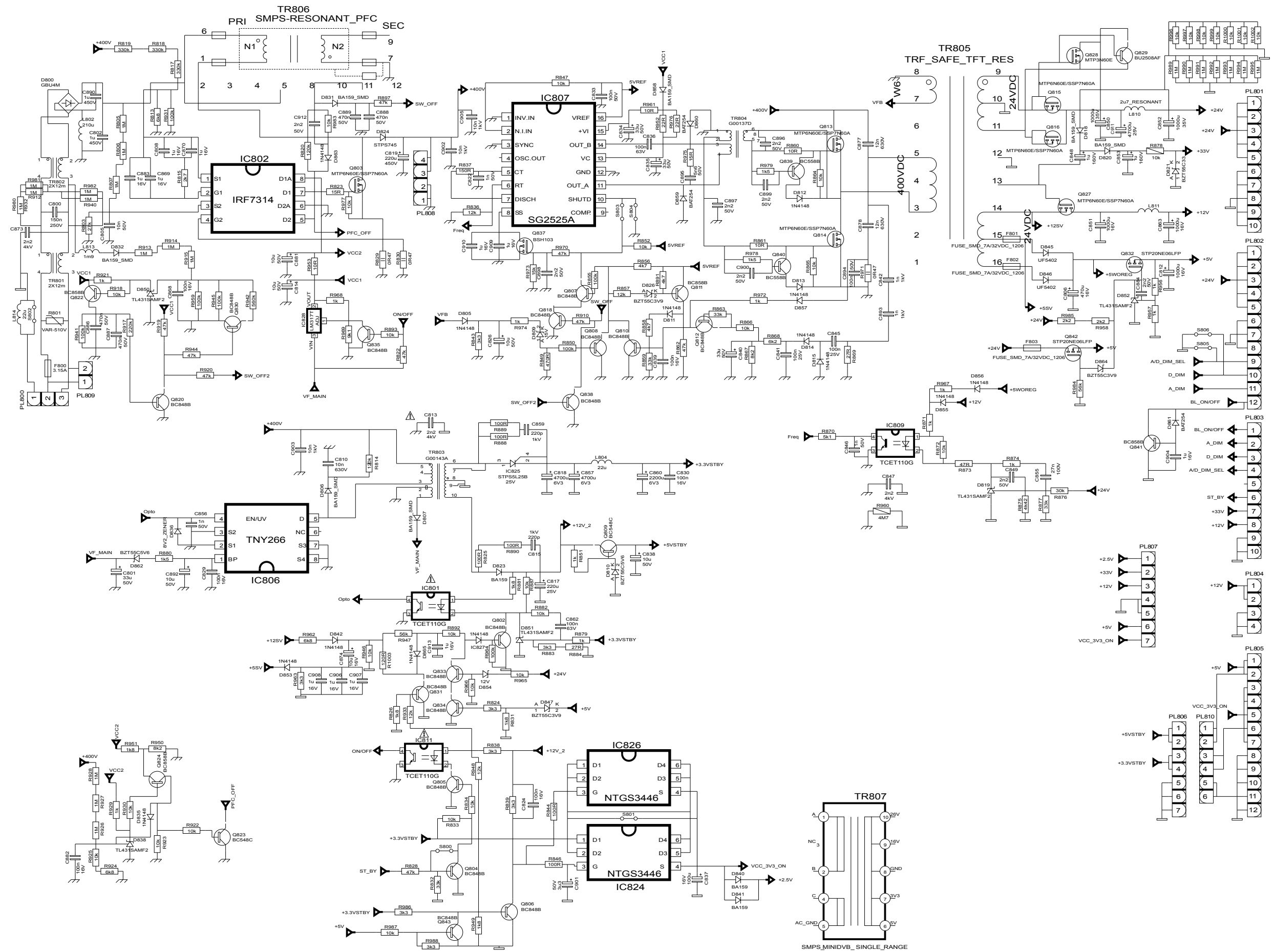
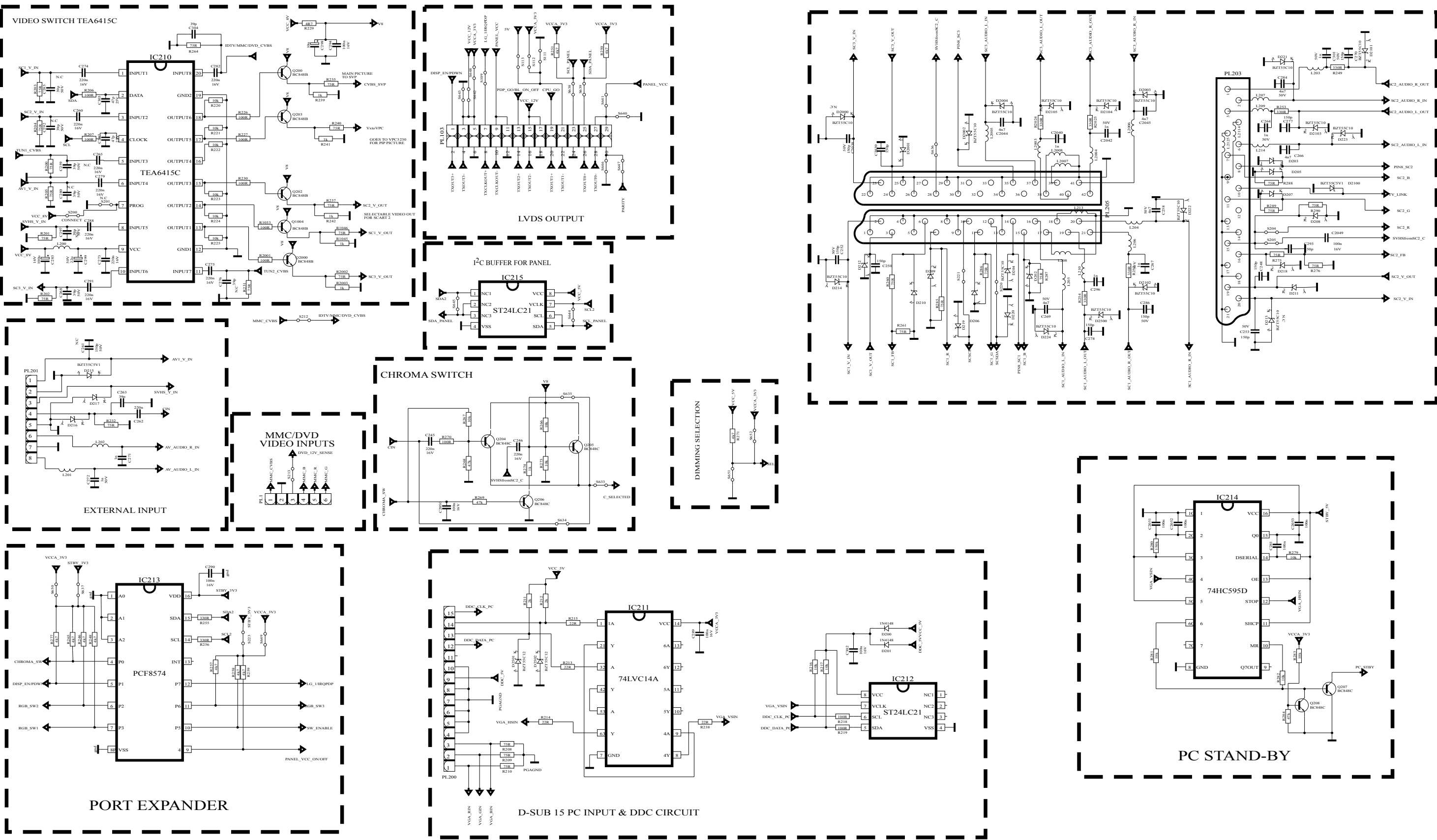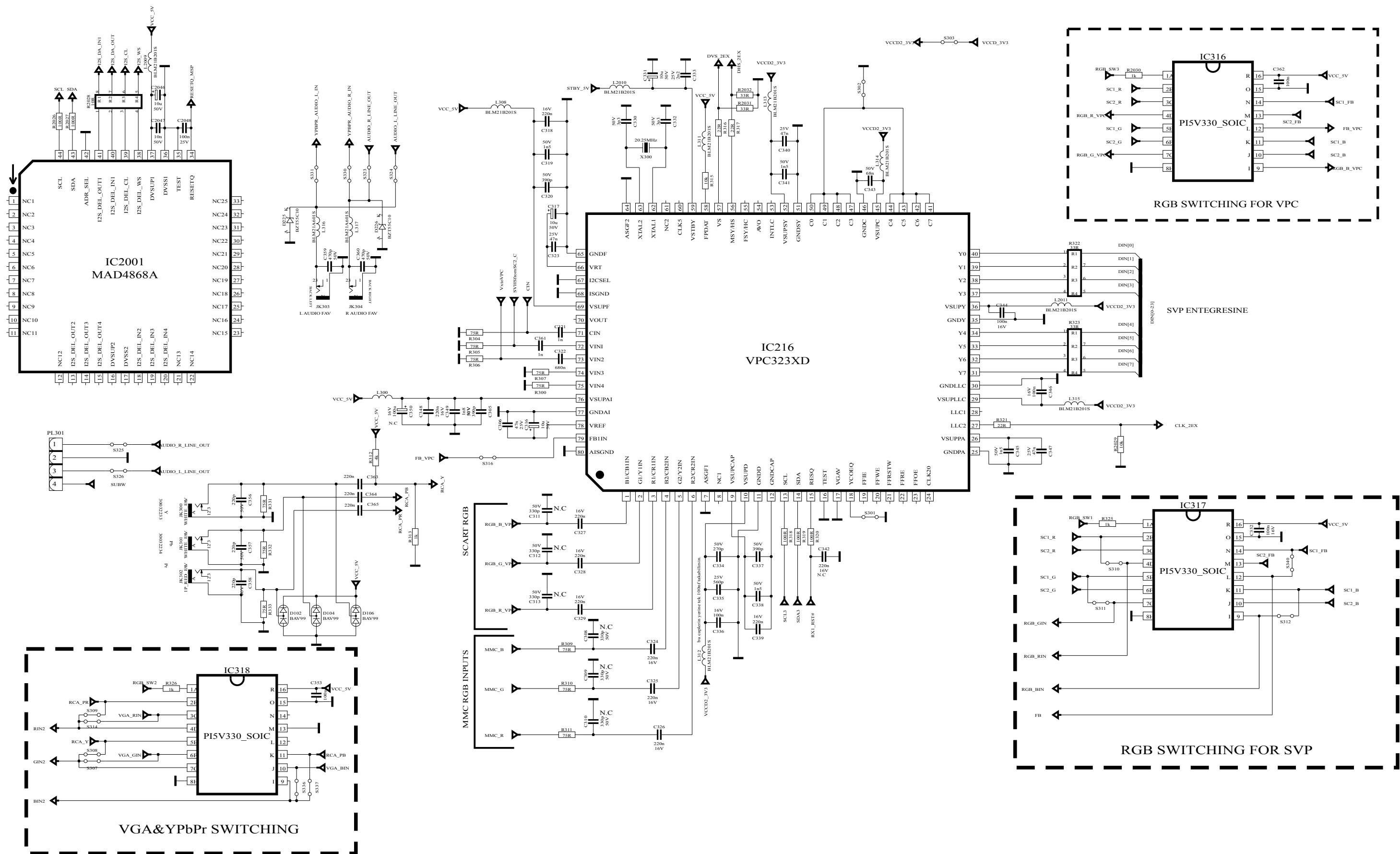# RESONANT MODE TFT POWER SUPPLY

45

BLOCK DIAGRAM - 32LD6600B

MAIN BOARD

AUDIO AMPL. BOARD

AUDIO/VIDEO/GRAPHICS IN/OUT

AUDIO
DECODING
MSP3411G
MICRONAS

MAIN_L, MAIN_R,

AUDIO
AMPLIFIER
D-CLASS

SVP-EX 59

LVDS OUT

IDTV,SVHS,MMC (RGB),PC IN

8-BIT YUV

VPC3230D
VIDEO PROCESSOR
PIP PICTURE
MICRONAS

SDA5550
MCU
MICRONAS

HDMI DECODER
SIL9993

24 BIT RGB

PSU

VIDEO SWITCH TEA6415C

IC210

TEA6415C

LVDS OUTPUT

I²C BUFFER FOR PANEL

IC215

ST24LC2I

CHROMA SWITCH

DIMMING SELECTION

EXTERNAL INPUT

MMC/DVD
VIDEO INPUTS

PORT EXPANDER

IC213

PCF8574

D-SUB 15 PC INPUT & DDC CIRCUIT

IC211

74LVC14A

IC212

ST24LC21

PC STAND-BY

IC214

74HC595D

32LD6600B - VIDEO DECODER

HITACHI

DIGITAL IDTV INPUTS [ITU 601]

IC107
74LX1G86STR

PC&YPbPr INPUT

MAIN PICTURE

MAIN RGB INPUT

IC224
SVP_EX_51

LVDS OUT

DDR RAM

HITACHI

EM6A9320
IC1

26LD6600

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VS20231546

Main PCB - 17MB08
VS20244409
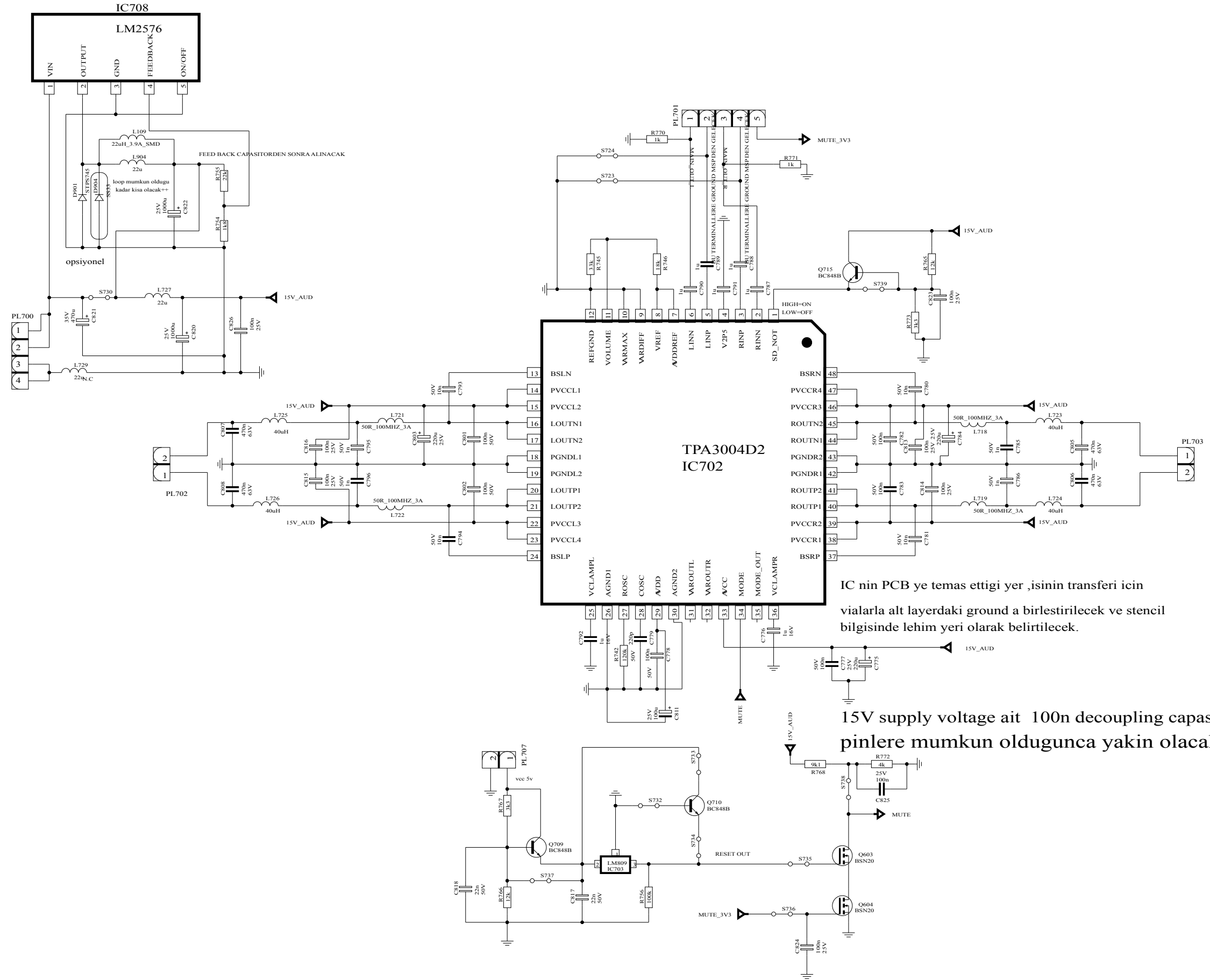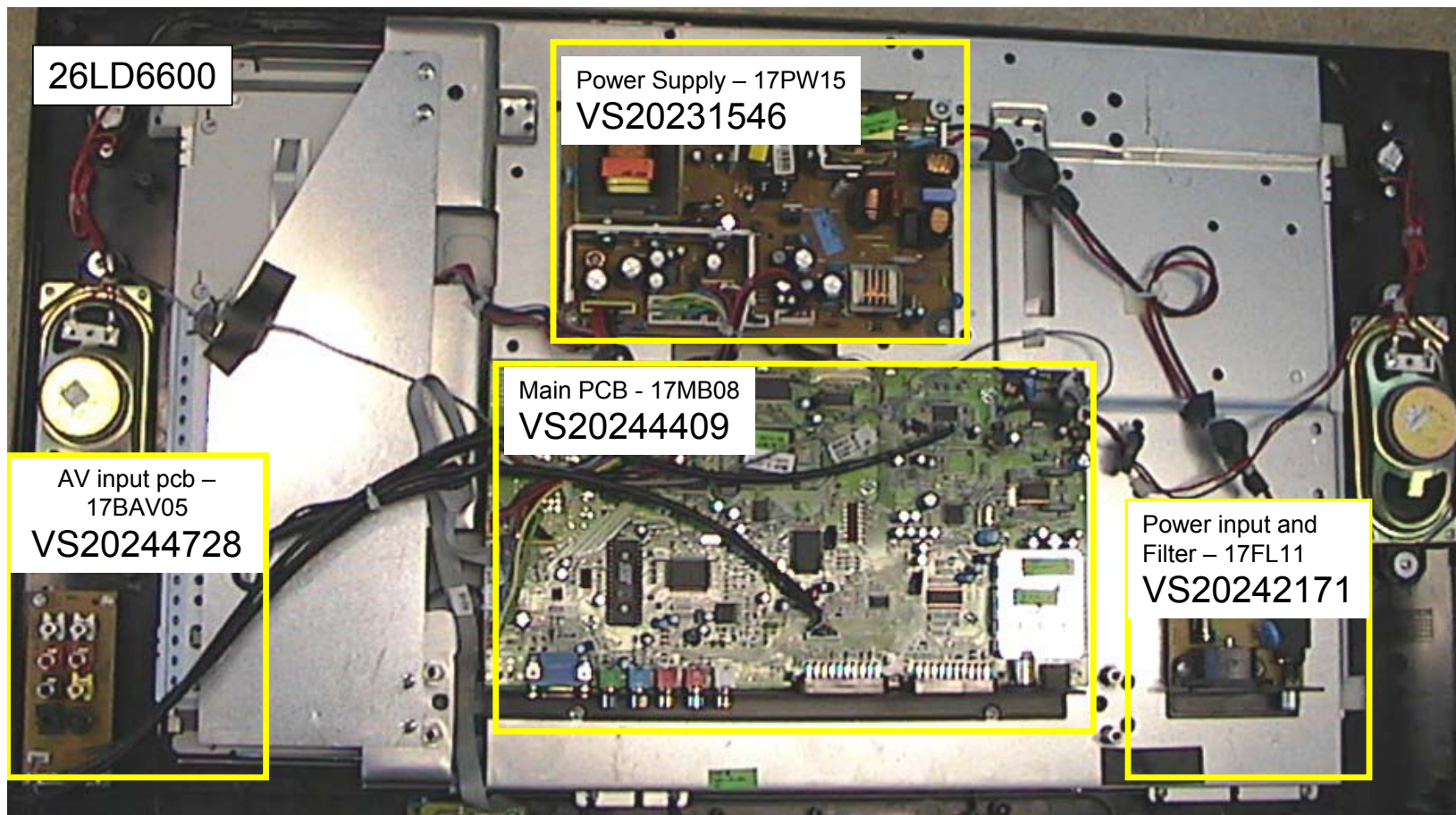
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VS20244728

Power input and Filter – 17FL11
VS20242171
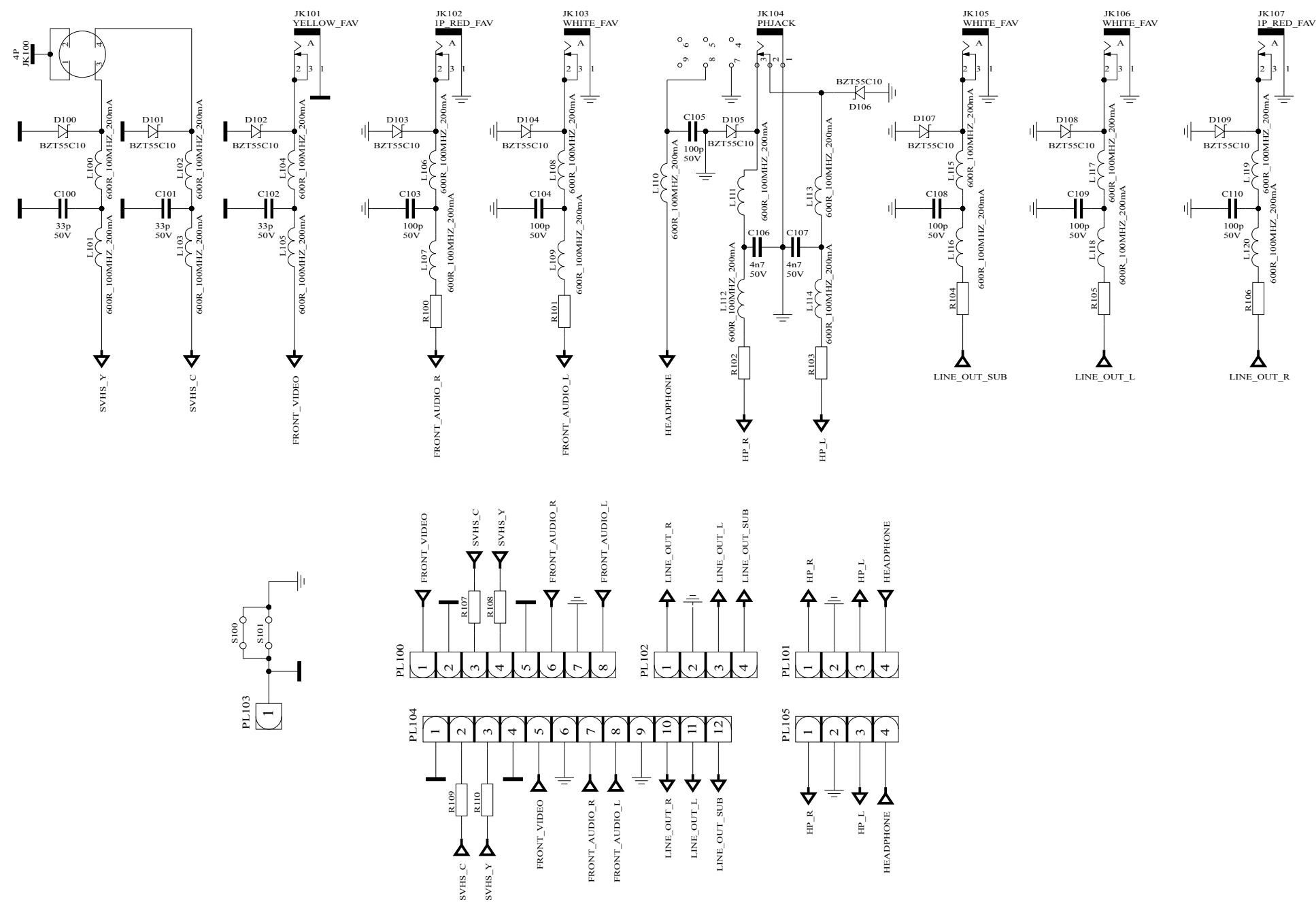
32LD6600

Power Supply – 17PW15
VS20237231

Audio PCB – 17AMP03
VS20232670

Main PCB – 17MB15
VS20224906

AV input 17FAV11
VS20233490

LED PCB
VS20187015

Filter and power input
17FL11
VS20225434

37LD6600

PWB AMPLIFIER / SOUND 18AMP05

VS20217063

PWB POWER BOARD 17PW15
VS20237239

PWB NOISE FILTER 17FL11-4

VS20242224

PWB 17FAV15 (AV/HP/SVHS/VHS/L.OUT)

VS20217401

PWB MAIN 17MB15 - **VS20218117**

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