Solartron
INSTRUMENTATION GROUP

Digital Multimeters 7050, 7140 and 7144

Technical Manual

SOLARTRON
Schlumberger

CONTENTS

CORRIGENDUM

Discontinuation of model 7054

Since the 7054 has been discontinued the reader should ignore all references to this variant.

7050
DIGITAL
MULTIMETER

Part No. 70500117

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Schlumberger

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TECHNICAL MANUAL

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SECTION 1 General

INTRODUCTION

The 7050 Digital Multimeter (DMM) combines the advantages of a compact and versatile multimeter with the precision and convenience of a digital instrument. Automatic range selection and polarity decision give rapid readings. The complete absence of range switching enables the user to concentrate on the task in hand and apart from selecting the actual measurement mode required all other measurement decisions are undertaken automatically, so reducing the risk of damage to the user's equipment, as well as to the DMM.

The DMM covers the following measurement modes, all auto-ranging.

DC VOLTAGE

10μV - 1000V

AC VOLTAGE

10μV - 750V

RESISTANCE

100mΩ - 11MΩ

DC CURRENT

1nA - 1A

With a scale length of 109.999.

Model 7050 also incorporates an automatic over-range indication, automatic overload protection and automatic blanking of unused digits.

Model 7054 incorporates a digital output in parallel BCD form for use with printers and other output devices.

SECTION 2 Operation

This section provides all the necessary instructions concerning preliminary adjustments and operating procedures required to put the instrument into everyday use.

PRELIMINARY ADJUSTMENTS

Before using the instrument for the first time the following preliminary adjustments should be carried out:

(a) Check that the voltage selection switch on the rear panel is in the correct position.

(b) Check that the correct fuse is fitted as follows:-

230V	150mA	Slo-Blo	1¼" x ¼"
115V	300mA	Slo-Blo	1¼" x ¼"

(c) Connect a suitable connector to the input mains lead as follows:-

Brown	-	Line (Live)
Blue	-	Neutral
Yellow/Green	-	Earth

This earth connection is essential for stability of readings and user safety

(d) Plug into the mains supply and switch the instrument ON.

OPERATION

The operation of this instrument under most conditions will be found to be self-evident. The only operator decision required is the selection of the measurement mode required.

During operation, the following factors should be borne in mind:-

1. Since the instrument will automatically change ranges to suit the applied input potential, care should be taken to note the decimal point position in combination with the unit indicators.

2. In the event of an unintentional voltage or current overload, the offending potential should be removed as soon as possible since continuous overload may eventually cause damage to the instrument.

3. Due to the high input impedance of the input amplifier, the display readings will be random when the instrument is left with its input terminals as follows:-

   (a) Open circuited on 'V.DC' and 'V.AC' modes.

   (b) Short circuited on 'μA' and 'mA' modes.

   Random readings can cause the range relay to switch on and off which can be prevented by short circuiting the input terminals in the case of (a) and open circuiting them in the case of (b).

4. In the 'Ω' mode, open circuited input terminals produce an overload condition i.e. a steady '1' being displayed. Short circuited input terminals produce a nominal zero condition.

5. When measuring voltages on the lowest range and resistance on the highest range of the DMM, pick-up on the input leads may become a problem. If this occurs it is recommended that the leads be kept as short as possible and/or screened.

SECTION 3 Servicing

This section provides detailed servicing information for the instrument. Setting-up procedures and calibration are covered in Section 4.

INTRODUCTION

This Servicing Section is based on the functional block system of circuit diagrams, whereby components are grouped together to form a functional entity. A large scale block diagram is used to describe the overall operation of the Digital Multimeter (DMM). This diagram is then sub-divided to produce blocked circuit diagrams.

Information regarding circuit descriptions, component locations, printed circuit board layouts and any specific cautionary notes concerning components or testing procedures are arranged to be fully visible with the appropriate circuit diagram. Full calibration and setting up procedures are located in Section 4.

PRESENTATION OF INFORMATION

A brief glance through this section will reveal that the section is sub-divided into three major sub-sections, each of which deals with a major function in the DMM. Located within each section are block type circuit diagrams, always folding out clear to the right, with a functional description of each on the left hand text page. The pcb layout diagrams are arranged to fold out clear to the left, allowing cross reference between diagram and component location.

Referring to any of these diagrams, it can be seen that the major functional signal pathways are shown as bold lines, whilst those of a minor or control function are shown with thinner lines. The arrows indicate the direction of functional flow, which in the majority of cases will be from left to right of the diagram. Most feedback paths however, will flow from right to left.

These rules, although generally followed, are not rigidly adhered to where observance may cause ambiguity or is extravagant of space.

COMPONENT LOCATION

Diagrams of the printed circuit boards associated with each circuit diagram and photographs illustrating the method of access are reproduced in a manner enabling them to be examined in conjunction with the diagrams. By this method the physical position of any component can be quickly established.

COMPONENT NUMBERING

Each printed circuit has its own component numbering. This means that on a circuit diagram more than one component may be shown with the same component number. When this occurs care must be taken to ensure that the correct part is identified if it is required to replace the component. For instance, in the 7050 there are several pcb's, all of which include a component numbered R1.

The correct item must be identified from the parts list by reference to the pcb or assembly on which it is mounted.

POWER RAIL NOTATION

The power rails are shown as short detached bars with the nominal voltage annotated. On any one pcb, all bars annotated with the same voltage are electrically connected together and correspond to the appropriate rail notation shown on the power supplies circuit diagram, referenced 10.

The 0V rail in some cases is associated with the signal paths, annotated SIGNAL 0V and followed by a reference number 1 to 4 inclusive, thereby identifying the decoupling components used for that particular group of components. All identically referenced zero volt lines are electrically connected together at the 0V STAR POINT on pcb 1 (C18 –ve).

It must be remembered that the voltages shown are approximate, being proportional to the load taken through the appropriate decoupling resistors. A voltage reading which is inconsistant with the value given on the diagram should not, therefore, be taken as a symptom of unserviceability without reference to other indications.

ELECTRICAL CONNECTIONS

Electrical connections used are mainly of the Berg pin and socket type. Two plugs and sockets are employed using Berg pin/socket combinations. These are clearly identified, with all the remaining Berg pin/socket connections bearing only a number.

Transformer connections used are of the disconnect pin type.

SPLIT PADS

The split pads provide a means of adjusting circuit resistance and also for isolating various parts of the circuit during fault diagnosis.

They are short circuited by running solder across the gap and open circuited by removing the solder track. Care should be taken not to apply excessive heat during these operations.

FUNCTIONAL DESCRIPTION

The Model 7050 Digital Multimeter (DMM) may be looked upon as an instrument which divides down into three major functional areas. These are shown as coloured areas in the adjacent KEY DIAGRAM.

This diagram should be looked upon as a pictorial index as within each of these coloured areas are further blocks, each referenced with a number which refers to a specific block/circuit diagram within each section of this manual.

It is important when using these diagrams that the information should be looked at from a functional view-point before dealing with any actual detailed servicing. That is to say, deduce what could be the problem before actually looking at specific circuit details.

With reference to the KEY DIAGRAM, the input signal is applied to an ANALOGUE signal processing section. The primary function of this block is to scale the input signal into a form suitable for use by the DIGITAL (A/D Converter) section.

The input signal in all cases is converted into a dc signal. Since the A/D Converter can only handle signals within the range 0-11V directly, the analogue section provides a 100/1 attenuation on the higher ranges, also 10/1 on the acV mode.

The scaled analogue input is then converted into a digital form by means of the triple ramp technique of integration (for a detailed explanation, refer to Section 3B), the result of which is displayed on a light emitting diode (LED) display.

The third major functional block provides the power supplies to operate the whole instrument. This block also provides timing pulses to relate the measurement to the incoming mains supply frequency in order to overcome ac interference.

GENERAL NOTE:-

The numbers in each of the blocks shown below refer to the appropriate block and circuit diagrams contained in this section.

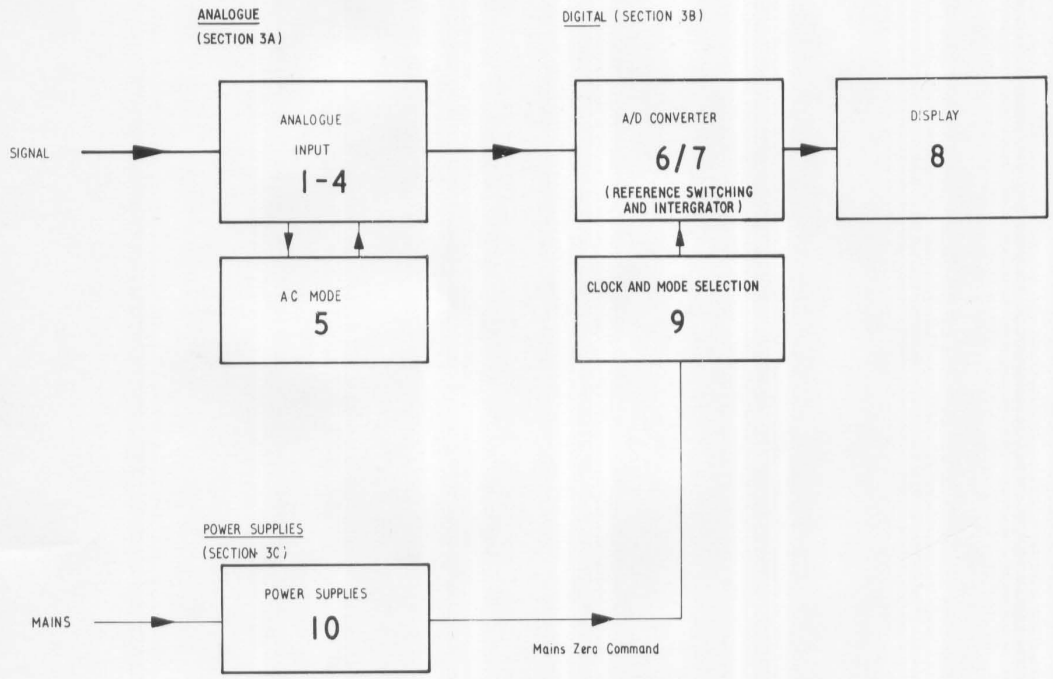


Fig. 3.1. Key Diagram (Pictorial Index).

SUB SECTION 3a Analogue

This sub-section deals with the ANALOGUE section of the instrument whose primary function is to convert the input signal into an acceptable form suitable for digital conversion by the DIGITAL section (SUB-SECTION 3B - DIGITAL).

SIGNAL CONVERSION

INTRODUCTION

The purpose of these sections of circuitry is to convert the incoming signal into dc suitable for conversion by the A/D Converter in the DIGITAL section of the instrument.

DC MEASUREMENT

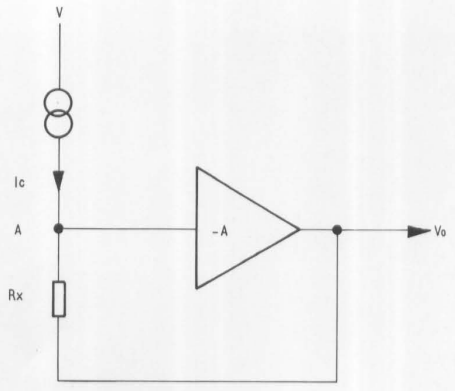
In this mode of operation, since the applied signal is already dc, the circuitry serves to scale the input to within the upper 11V limit acceptable to the A/D Converter input.

The INPUT AMPLIFIER is arranged in a series feedback configuration to provide a very high input impedance to the applied signal on the unattenuated ranges (0-11V).

The Analogue Input circuit in the 'V.DC' mode is shown on DIAGRAM 1.

RESISTANCE MEASUREMENT

The resistance measuring mode, 'Ω', is shown on DIAGRAM 2. Consider the following simplified diagram.



Point A is a 'virtual earth' input to a very high gain amplifier (INPUT AMPLIFIER). In order that the current flowing into and out of point A is balanced, the output of the amplifier Vo must rise to develope a potential drop across the applied unknown resistance Rx such that the constant current Ic derived from the reference voltage all flows through Rx. The final value of Vo when the circuit balances will be proportional to Rx and it is this output which is used by the A/D Converter for conversion to units of resistance.

CURRENT MEASUREMENT

Following from the above description of resistance measurement, it can be seen that if we make Rx a known value (RV6/R6 on DIAGRAM 3), the output of the amplifier Vo will be proportional to the unknown applied current.

AC MEASUREMENT

The section of circuitry used for converting the applied input to dc is shown separately on DIAGRAM 5.

The applied signal passes through a separate INPUT ATTENUATOR network and, via the AC AMPLIFIER buffer stage and SCALING RESISTORS, to the SUMMING JUNCTION. This point acts as a 'virtual earth' to the INPUT AMPLIFIER which follows. The output of this amplifier passes through the RECTIFIER SYSTEM which then divides the amplifier output into positive and negative half cycles by rectifier action. The positive half cycle output is filtered by the LOW PASS FILTER to form the equivalent dc input to the A/D Converter.

Since the rectified output would produce the mean value of the applied input, provision is made (RV3) to scale the signal input such that the final displayed reading is the rms (root mean square) as opposed to mean value of the applied signal. It should be remembered that this scaling action will only be valid when the input wave form is sinusoidal.

TEST WAVEFORMS

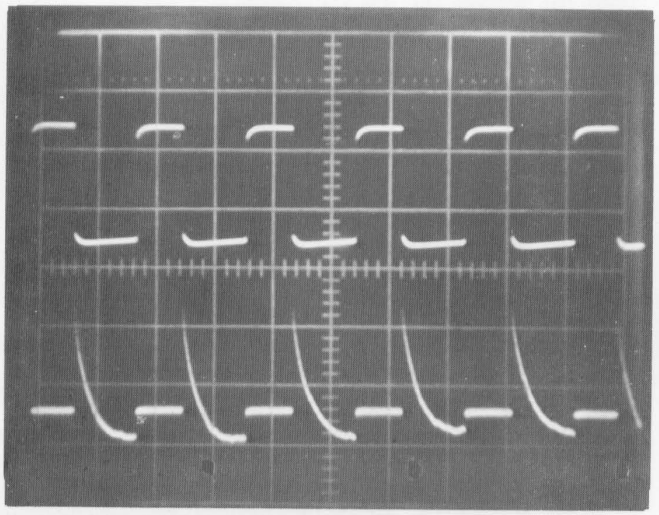
FRAME 3A - 1

UPPER TRACE

A typical output waveform produced by the CHOPPER DRIVE (DIAGRAM 4) at TR4 collector. The output at TR3 collector is an inverted form of this trace.

LOWER TRACE

A typical output waveform produced by the DEMODULATOR (DIAGRAM 4) at the junction of C5 and R11.



Time/cm:- 2ms.

Volts/cm:- 500mV.

Frame 3A-1 Chopper/Demodulator waveforms.

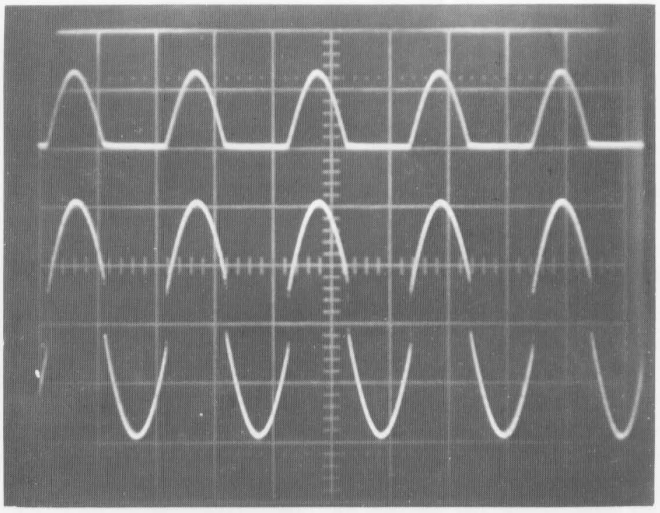
FRAME 3A - 2

UPPER TRACE

A typical output waveform produced at diode D3 cathode, the output from block RECTIFIER SYSTEM (DIAGRAM 5) used to provide dc to the A/D Converter for operation on ac V mode.

LOWER TRACE

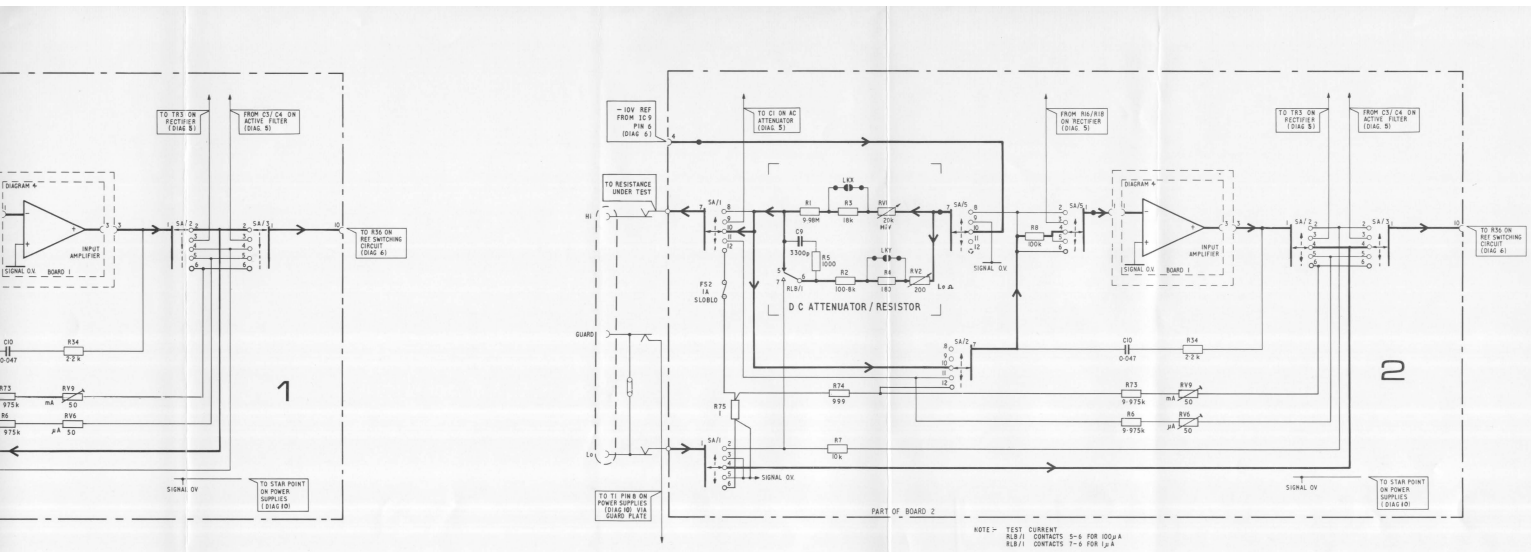
A typical output waveform provided by the complementary common base stage formed by TR1/2 in block RECTIFIER SYSTEM (DIAGRAM 5) and used to drive both halves of the diode feedback loop. The sharp transitions about the zero of the output waveform overcome possible non-linear rectification, due to diode characteristics up to about 0.7V.

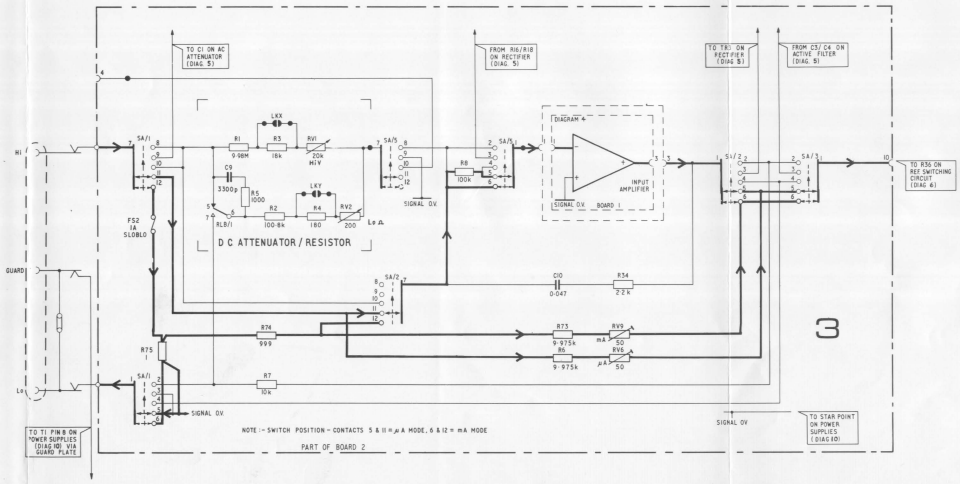


Time/cm:- 1ms.

Volts/cm:- 1V.

Frame 3A-2 Rectifier System waveforms.



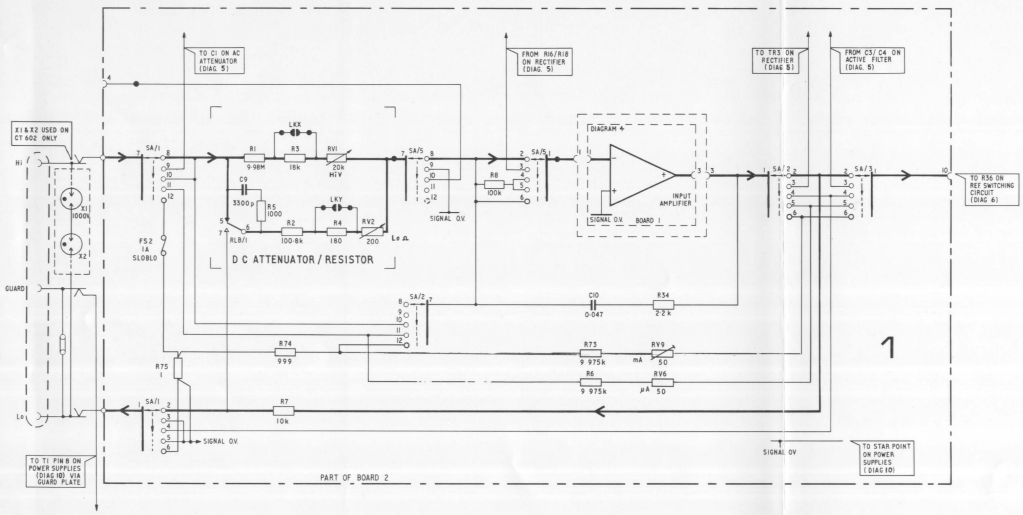


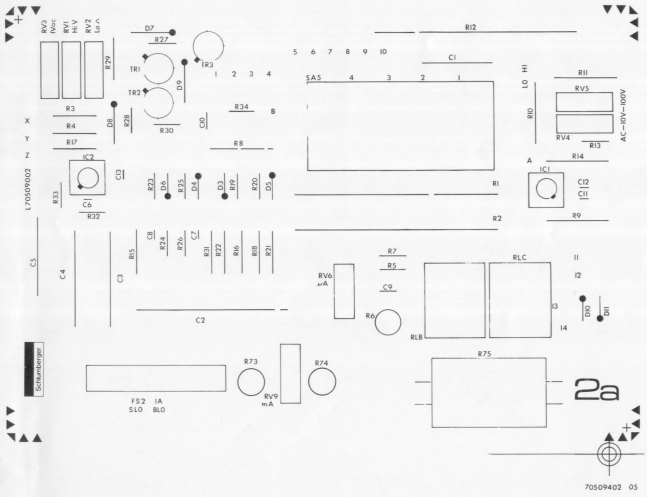
1 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN DC MODE)*

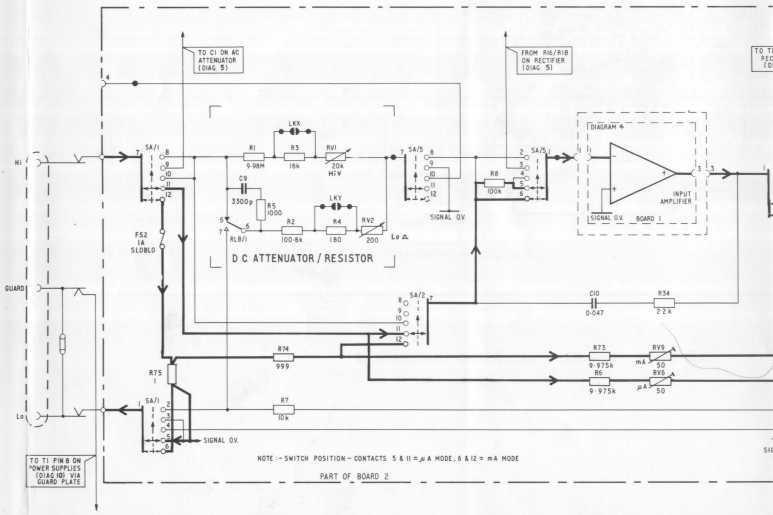
2 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN OHMS MODE)*

2a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*

3 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN CURRENT MODE)*


TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG. 5)
TO TR3 ON RECTIFIER (DIAG 5)
FROM C3/ C4 ON ACTIVE FILTER (DIAG. 5)
X1 & X2 USED ON CT 602 ONLY
Hi
Lo
GUARD
X1 1000k
X2
FS2 1A SLOBLO
SA/1
R1 9·98M
LKX
R3 18k
RV1 20k HI V
C9 3300p
R5 1000
RLB/I
R2 100·8k
LKY
R4 180
RV2 200
Lo Ω
SA/5
R8 100k
SIGNAL O.V.
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V.
BOARD 1
SA/2
C10 0·047
R34 2·2k
R74 999
R75
R73 9·975k
RV9 mA 50
R6 9·975k
RV6 µA 50
R7 10k
SA/1
SIGNAL O.V.
TO R36 ON REF. SWITCHING CIRCUIT (DIAG 6)
SIGNAL O.V.
TO STAR POINT ON POWER SUPPLIES (DIAG 10)
TO TI PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
PART OF BOARD 2
D C ATTENUATOR / RESISTOR
1


RV3 RV1 HI V
RV2 Lo Ω
D7
R27
TR1
TR2
TR3
D9
R39
R30
D8
R28
C10
R34
R3
R4
R17
IC2
C13
C6
R32
R33
C5
C4
C3
C2
R23
D6
R25
D4
R19
D3
R20
D5
R15
C8
R24
R26
C7
R31
R22
R16
R18
R21
R12
C1
SA/5
RII
RV5
RV4
R13
R14
IC1
C12
C11
R9
R2
R1
RLC
RLB
D10
D11
RV6 µA
R6
C9
R5
R7
R73
R74
R75
RV9 mA
FS2 1A SLO BLO
Schomberger
2a
70509402 05


TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG. 5)
Hi
Lo
GUARD
FS2 1A SLOBLO
SA/1
R1 9·98M
LKX
R3 18k
RV1 20k HI V
C9 3300p
R5 1000
RLB/I
R2 100·8k
LKY
R4 180
RV2 200
Lo Ω
SA/5
R8 100k
SIGNAL O.V.
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V.
BOARD 1
SA/2
C10 0·047
R34 2·2k
R74 999
R75
R73 9·975k
RV9 mA 50
R6 9·975k
RV6 µA 50
R7 10k
SA/1
SIGNAL O.V.
NOTE :- SWITCH POSITION - CONTACTS 5 & 11 = µA MODE, 6 & 12 = mA MODE
TO TI PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
PART OF BOARD 2
D C ATTENUATOR / RESISTOR

INPUT AMPLIFIER

PROTECTION NETWORK

D1 and D2 protect the CHOPPER AMPLIFIER during overload conditions. D3/D4 in conjunction with D5/D6 limits the OUTPUT AMPLIFIER output to within ± 12V.

LOW-PASS FILTER

R3, R4 and C1 form a low-pass filter which removes the high frequency components (> 100Hz) from the dc channel and prevents spikes from the CHOPPER (Modulator) circuitry reaching the input terminals.

CHOPPER DRIVE

A 275Hz emitter-coupled Multivibrator TR3/4 for driving the CHOPPER and DEMODULATOR.

A small proportion of the anti-phase output is applied via RV2 to minimise chopper-spikes produced by TR1 in the CHOPPER (Modulator) circuitry.

(Refer to Section 4 - Setting Up Procedure for details on the adjustment of RV2).

CHOPPER (MODULATOR)

The filtered output from the LOW PASS FILTER is 'chopped up' by alternately shorting the signal to earth via TR1 to form an ac type signal. The chopping frequency is determined by the in-phase output of the CHOPPER DRIVE multivibrator.

Anti-phase chopper drive is applied to G2 of TR1 to minimise chopper spikes.

RV1 (Vo) provides a small dc voltage to the Chopper output, compensating for small offsets.

CHOPPER AMPLIFIER

IC1, whose gain and frequency response are defined by C3, C4, R8 and R9, amplifies the input (chopped) waveform produced by the CHOPPER (Modulator). The ac gain is 10,000 and the dc gain is unity.

DEMODULATOR

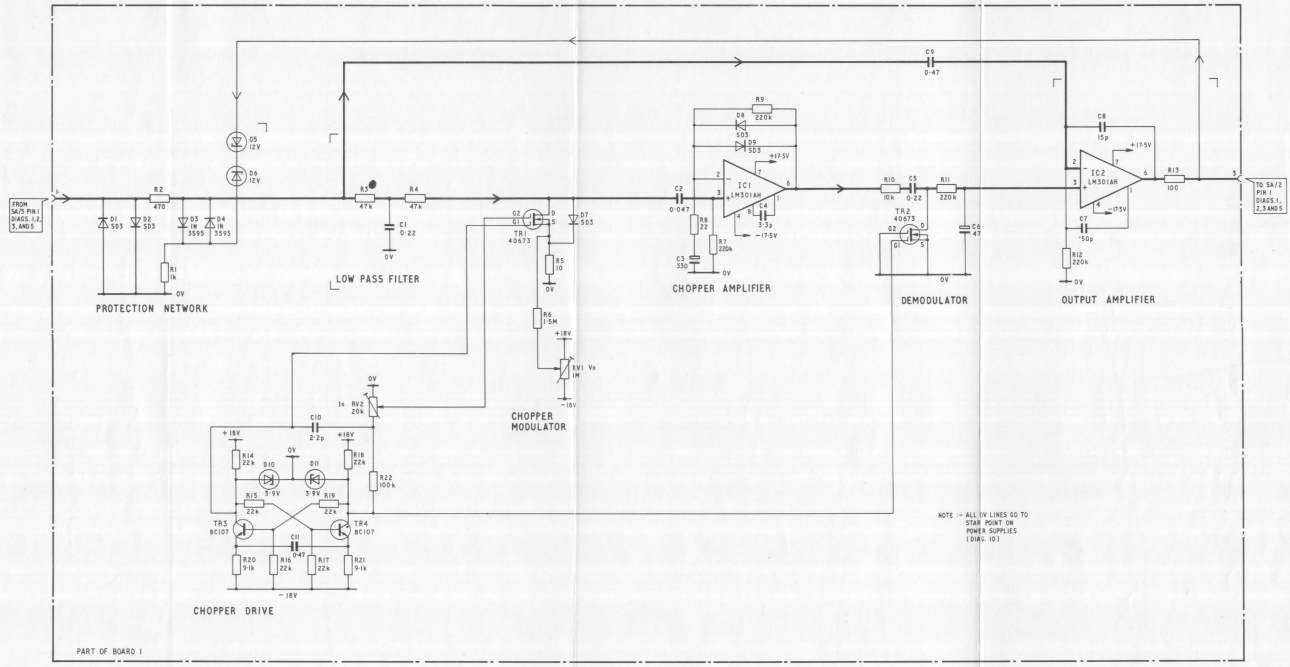
The output from the CHOPPER AMPLIFIER is fed via C5 to TR2 where it is dc restored. The ac component is removed by filter R11 and C6, leaving the dc component only.

OUTPUT AMPLIFIER

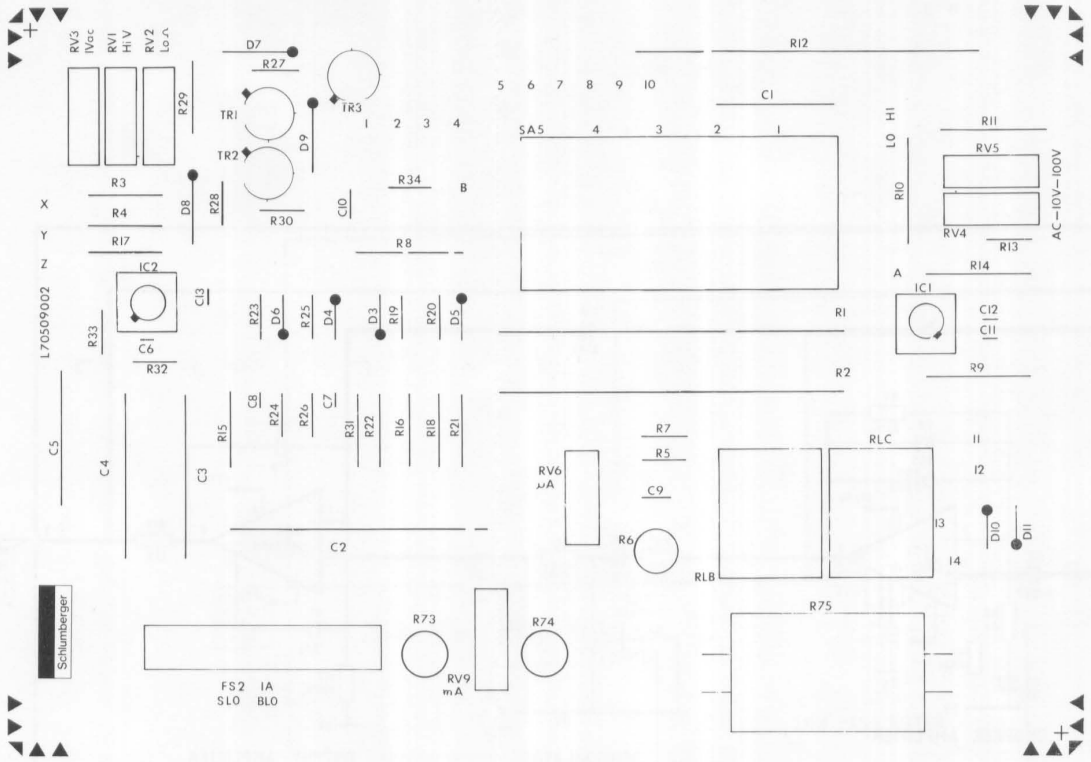
The ac component (> 2Hz) of the input voltage is coupled directly via R12/C9 to the inverting input of the amplifier while the dc component on C6 (DEMODULATOR) is added into the non-inverting input.

The output is applied to the PROTECTION NETWORK which limits the over-all amplifier output to within ± 12V.

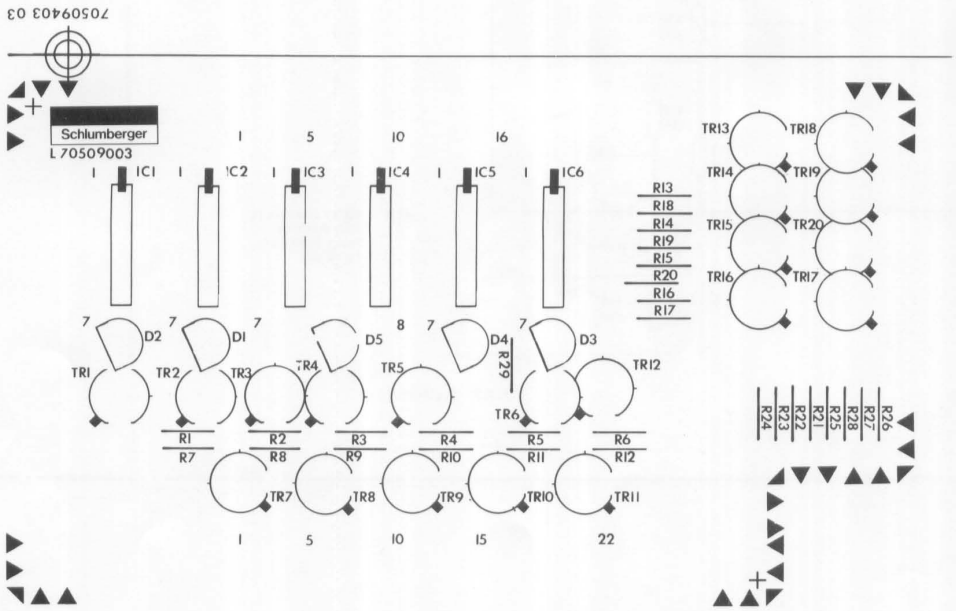
◄ *DIAGRAM 3a PCB 1 COMPONENT AND COPPER TRACK LAYOUT*



4 INPUT AMPLIFIER CIRCUIT DIAGRAM



4a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*



4b *PCB 3 COMPONENT AND COPPER TRACK LAYOUT*

AC MODE

INPUT ATTENUATOR

On the 100V and 750V ranges, relay RLB is energised to attenuate the input signal by a factor of 100. On the 10V range RLB and RLC are energised to attenuate the input signal by a factor of 10. The input impedance is 1MΩ whether the attenuator is energised or not.

AC AMPLIFIER

This is a voltage follower stage, isolating the input from the SCALING RESISTORS. R14 in conjunction with IC1 provides overload protection.

SCALING RESISTORS

The applied input plus the feedback signals via R16/R18 in the RECTIFIER SYSTEM are summed at the 'virtual earth' of the INPUT AMPLIFIER. RV3 scales the input signal so that the final displayed value on the LED module represents the rms (root-mean-square) value of the applied input assuming a pure sine-wave shape.

RECTIFIER SYSTEM

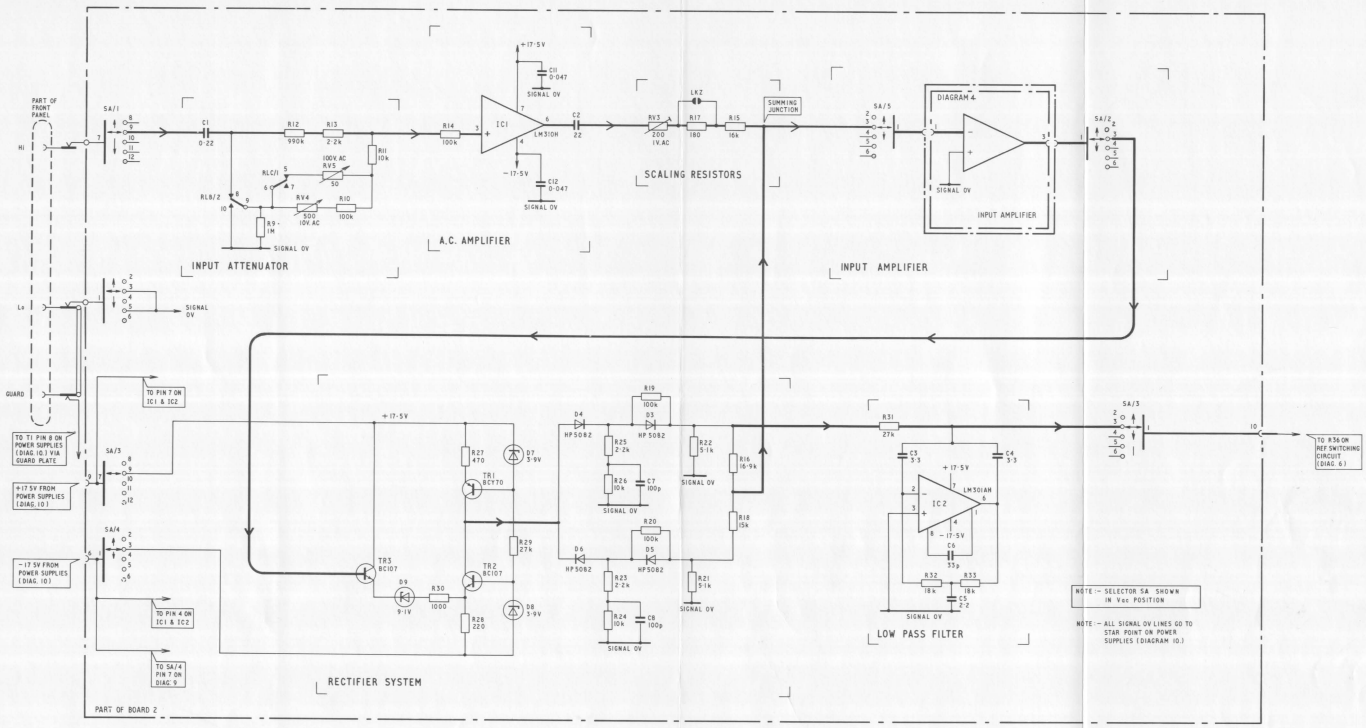
The output of the INPUT AMPLIFIER (DIAGRAM 4) drives the complementary common base stage formed by TR1/2. Positive half-cycles are fed back to the 'virtual earth' via D4/D3 and precision resistor R16. Negative half-cycles are fed back via D6/D5 and R18. Only the positive half-cycles are taken for digital conversion.

R25/R26/C7 and R23/R24/C8 are shaping networks which improve frequency response at low signal levels.

LOW PASS FILTER

IC2 is connected as a low-pass active filter to remove high frequency components from the rectified ac signal. The filter has a nominal cut-off frequency of 3Hz and provides at least 60dB per decade attenuation.

◄ *DIAGRAMS 4a & 4b PCB 2 & 3 COMPONENT AND COPPER TRACK LAYOUTS*



5 *AC MODE CIRCUIT DIAGRAM*

SUB SECTION 3b Digital

This sub-section deals with the DIGITAL section of the instrument whose primary function is to convert the dc analogue input into digital form.

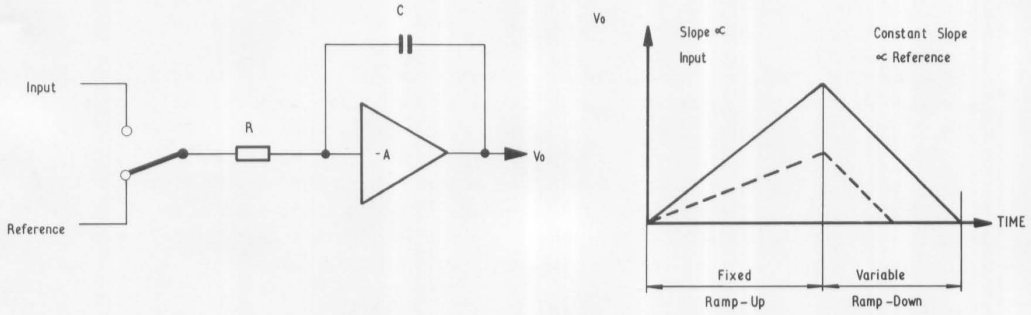
TRIPLE RAMP DIGITAL CONVERSION

INTRODUCTION

The triple ramp technique of analogue to digital conversion may be considered as a refined version of the well known dual ramp technique with the addition of a third ramp. This third ramp (known as fine ramp-down) acts like a 'vernier' upon the usual ramp-down period.

BASIC PRINCIPLES OF OPERATION

Examination of the following simplified cirucit diagram serves to illustrate the principles used to perform analogue to digital conversion in this instrument.



BASIC DUAL-RAMP SYSTEM

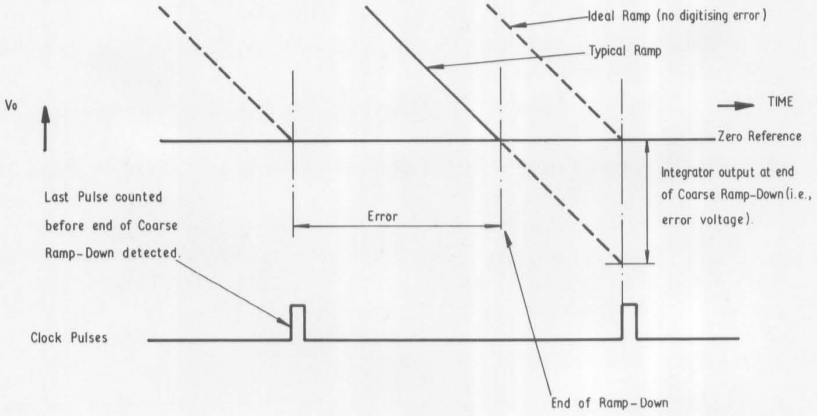
When the integrator is connected to the input its output 'ramps-up' at a rate which is proportional to the value of the input. After a fixed time the switch changes over and connects the reference in place of the input. It is so arranged that the reference voltage is of opposite polarity to that of the input, so that the integrator output now 'ramps-down' at a defined rate which is determined by the value of the reference.

If the ramp-up period is made constant by using a clock pulse generator to gate the input switch, the number of pulses produced during the 'ramp-down' period, the length of which is controlled by the slope of the reference voltage, will be directly proportional to the applied input.

Since both ramp-up and ramp-down periods are related to a common timebase, any variations of clock frequency do not affect the reading.

In the DMM, the reference voltage used during this 'ramp-down' period (known as 'coarse ramp-down') is actually 10V, so each ramp-down pulse with a 'full-house' counter length of 10,000 will represent 1mV. The total number of pulses collected between the end of ramp-up and the point where the integrator output was driven to zero is a direct measure of the applied input voltage to within 1mV.

Looking at a greatly magnified view of the integrator output waveform at the point where the integrator output passed through zero, it can be seen that there is an inherent digitising error within the system, the magnitude of which can be 1mV.



If we allow the integrator output to continue beyond zero until the next clock pulse, the integrator capacitor will be charged to a level representing the difference between 1mV and the true measured input.

By adding two extra less significant decades to the counter, the minimum decade would represent 10μV. If we complement* the counter and then re-organise it such that it counts down to zero when driven by further clock pulses, by changing the ramp-down rate, the final count overall could represent the applied input when the integrator output again passes through zero.

In the DMM, this second ramp-down reference voltage is 100mV so that each new clock pulse will represent 10μV. In order to drive the integrator output to zero, the new ramp-down reference polarity is made opposite to the coarse ramp-down polarity. This third ramp is known as 'fine ramp-down'.

It can be seen that the final measurement could, in theory, be within 10μV of the applied input.

* COMPLEMENTING

The action of complementing a number within a counter can be followed by referring to the following example.

We have a hypothetical counter capable of holding a total count of 100 pulses. If we count say 60 input pulses, still required to 'fill-up' the counter will be 100-60 i.e. 40. It is this number which is defined as the complement of the number 60 in this example.

MEASUREMENT CYCLE DRIVES

INTRODUCTION

All stages of analogue to digital conversion are controlled by IC7-board 1, whose outputs turn on or off appropriate FET switches to select the appropriate sections of circuitry required at each stage of a measurement cycle.

ELECTRICAL ARRANGEMENT

There are eight cycle control drive outputs as follows:-

IC7-pin 11	Drift Correct
pin 12	Earth Clamp
pin 13	Spoiler
pin 14	Neg. Fine Reference
pin 15	Pos. Fine Reference
pin 16	Pos. Coarse Reference
pin 17	Neg. Coarse Reference
pin 18	Input Switch

During a typical measurement cycle, each of these pins will assume the states shown in Table 3B-1. The Pause periods 1-4 are for internal use within the integrated circuit to allow time for internal re-organisation of the counter, range selection and other tidying up operations required. The duration of these periods will change depending upon the range, length of ramp-down, spoiler time etc. so differing pause periods should not be interpreted as indications of faulty operation.

TABLE 3B - 1 CONTROL CYCLE SEQUENCE

L = low $\leqslant$ - 16V H = high $\geqslant$ + 8V

IC7 - Board 1

Period	11	12	13	14	15	16	17	18
Drift Correct	L	L	H	H	H	H	H	L
Pause 1	H	L	H	H	H	H	H	L
Ramp-Up	H	H	H	H	H	H	H	L
Spoiler Period	H	H	L	H	H	H	H	L
Pause 2	H	L	H	H	H	H	H	L
Coarse Ramp	H	L	H	H	H	H*	L*	H
Pause 3	H	L	H	H	H	H	H	L
Fine Ramp	H	L	H	L*	H*	H	H	H
Pause 4	H	L	H	H	H	H	H	L

Levels marked* will be inverted when the applied signal input is negative (with respect to the - terminal on the front panel).

AUTO-RANGING

INTRODUCTION

The DMM is fully auto-ranging for all modes of operation. Range switching is divided into two parts, basic range selection and/or attenuator switching.

RANGE SELECTION

Each of the ranges is coded with a letter, the actual range depicted by each being dependent upon the measurement mode selected (refer Tables 3B - 2 to 4).

The basic ranges are coded A, B and C and progress in decade steps with A the highest. A, B or C followed by the letter R indicates the basic range together with the 100/1 or 10/1 attenuator stage, making a range selection with a full scale reading 100 or 10 times greater than that for the basic range alone.

TABLE 3B-2 VOLTAGE MEASUREMENT CODING

Nominal Range	Range of Voltages Displayed	Range Coding DC	Range Coding AC
1000V	1099.00 to 100.00V	AR	AR
100V	109.999 to 10.000V	BR	BR
10V	10.9999 to 1.0000V	A	CR
1V	1.09999 to 1.00000V 999.99 to 0.00mV	B	B

TABLE 3B - 3 RESISTANCE MEASUREMENT CODING

Nominal Range Ω	Range of Resistance Displayed	Range Coding
10M	10999.9 to 1000.0k	AR
1M	1099.99 to 100.00k	BR
100k	109.999 to 10.000k	A
10k	10.9999 to 1.0000k 999.9 to 0.0Ω	B

TABLE 3B - 4 CURRENT MEASUREMENT CODING

Nominal Range	Range of Current Displayed	Range Coding
100μA μA mode	1099.99 to 100.00μA	A
100μA	109.999 to 0.000μA	B
1000mA mA mode	1099.99 to 100.00mA	A
100mA	109.999 to 0.000mA	B

Ranging up or ranging down occurs just after the fine ramp-down period in the measurement cycle, and unless a range change decision occurs, the range in use will remain constant for the remainder of the cycle.

RANGE-UP SEQUENCE

A range-up decision will occur if the total count at the end of fine ramp-down in the counter equals or exceeds 1.1 times that count which corresponds to the nominal full-scale count for the particular range in use. Take for example the 1V range, a range-up decision occurs if the measured voltage is 1.1 volts or higher, making 1.09999V the highest voltage which will not cause a range-up decision.

RANGE-DOWN SEQUENCE

A range-down decision will occur if the total count in the counter after a measurement falls below 0.1 times that which corresponds to nominal full-scale count except when the particular range in use is the lowest for the mode of operation. In this instance, operation will be maintained on that range for all readings down to zero. Therefore for all but the lowest of a group of ranges 0.10000 times the nominal full-scale value is the lowest reading which will not cause a range-down decision.

RANGE SWITCHING (DIAGRAM 7)

The input signal to the INTEGRATOR may or may not be rescaled by means of changing the effective input resistance. When Range A is selected (i.e. Ranges B/C not turned on) the signal is applied through R41 (1M). When Range B or C is selected, the effective input resistance will be 100k (1M//110k $\simeq$ 100k) thus the integrator input signal will be rescaled by a factor of 10. By this method, the input dynamic range of the INTEGRATOR may be 0 - 11V, or 0 - 1.1V respectively. For inputs above 11V, the attenuator relays RLB and RLC provide the following functions:-

RLB/1:- Provides 100/1 attenuation on dc ranging

RLB/2:- Provides 100/1 attenuation on ac ranging

RLC/1:- Provides 10/1 attenuation on ac ranging (in conjunction with RLB/2)

RLC/2:- In conjunction with C49 and a 100k ohm to Vss (internal resistance in IC7) provides a delay of range change (approximately 2 readings) whilst in AC mode.

SELECTED FET'S TR17 - 20 (PCB No. 1)

Whenever any one of these components is replaced, it is essential that a component with the same colour coding is used or alternatively, replace the whole set.

NOTE. Reference should be made to the selection procedure detailed in the APPENDIX section of this manual.

IC7 - PCB No. 1 (MOS - LS1) INTEGRATED CIRCUIT

This 40 - lead dual-in-line ceramic package contains the digital circuitry used to control the measurement cycle, count and gate clock pulses, provide signals to drive the LED display and to rescale the Integrator during auto-ranging.

Details of all pin connections and functions are on the Clock and Mode Selection diagram, referenced 9. Where inputs from, and outputs to IC7 occur on other circuits, these are identified by the effected IC7 terminal number shown enclosed in a square.

WARNING

Before attempting to remove this integrated circuit, ensure that all power supplies are switched off.

MOS Integrated Circuits are prone to damage by static charges. It is therefore advisable to ensure that all items likely to come into contact with MOS ICs and/or the circuits in which they are employed are bonded together and are earthed. Affected ICs are notified on their pcbs.

DISPLAY

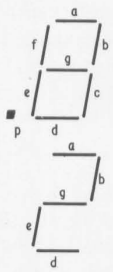
INTRODUCTION

The type of display used in this instrument is a light emitting diode (LED) 7-bar segment, time-shared type arranged to display 6 digits and a polarity sign.

7-bar SEGMENT FORMAT

Each of the possible digits, 0 to 9, is displayed using the universally accepted 7-bar segment format. In order to display a digit, a specific group of bars, each comprising a light emitting diode, is energised.

Each bar has been referenced with a letter a-g, and are arranged in the form of a figure 8 as shown below.

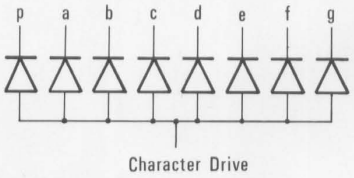


For example, suppose we wish to display the digit 2. In this case, bars a, b, d, e and g would be energised, all other bars being left de-energised.

The actual bars used to represent each digit are shown on DIAGRAM 8.

GENERAL ORGANISATION OF DISPLAY

The display used can display up to 6 characters, each of which comprises a 'diode tree' as shown below. The most significant digit can only display a one or a minus.



Each diode of a 'tree' corresponds to a specific bar as detailed above.

NOTE: The decimal point for each character is positioned to the left and will be energised whenever the 'p' bar is called for at the same time as the appropriate character.

In the DMM, each of the 6 possible characters is energised via the appropriate CHARACTER DRIVER (DIAGRAM 8) in sequence. In order that a particular digit may be displayed, the appropriate 7-BAR SEGMENT DRIVERS (DIAGRAM 8) are energised. For a group of diodes to light, both the segment and character drives must be present at the same time but since only one character drive will be present at any one time only one character will ever be on. It should be noted that the 1st character is incomplete, the surplus segments of which are arranged as the UNITS ANNUNCIATOR DISPLAY (DIAGRAM 8).

The polarity window will only display a negative sign, absence of display signifying a positive potential applied to the instrument. When 'V.AC' or 'Ω' is selected, no sign is displayed.

LOGIC ELEMENTS

NAND GATES (DIAGRAM 9)

Elements IC10a and b are logic elements performing a NAND function (positive logic) for which the following truth tables apply:

IC10a Pin No.	1	2	3
	H	H	L
	L	H	H
	H	L	H
	L	L	H
IC10b Pin No.	4	5	6
	H	H	L
	L	H	H
	H	L	H
	L	L	H

Logic Levels

H = -11V to - 14.5V

L = -16.5V to - 17.5V

D - TYPE BISTABLE (DIAGRAM 9)

Elements IC11 a and b are logic bistables (Flip-flops) performing a D-type function (positive logic) for which the following rules apply:

1. Whenever the CK (Clock) input goes high (positive logic), the Q output assumes the same state as that present on the D input.

2. Whenever the CK input is low, the D input level has no effect.

3. The $\overline{Q}$ output is always the complement of the Q output.

VOLTAGE LEVELS

Care should be taken when investigating this section of circuitry not to short any of the logic element connections to the 0V rails, since this action could apply a minimum level of -12V to the element and almost certainly damage it. It is recommended that the -17V rail should be used as a return path for test equipment and make appropriate adjustments to indicated readings.

TEST WAVEFORMS

FRAMES 3B-1/2

UPPER TRACE

This shows a typical input waveform at the INTEGRATOR (DIAGRAM 7) 'virtual earth' input.

LOWER TRACE

A typical ramp-up waveform produced at the input of the X1000 AMPLIFIER (DIAGRAM 7) at C21/R46. The small insert shows a typical fine ramp-down. Note that the coarse ramp-down cycle is shorter than that shown in the main trace for illustration purposes only.

FRAMES 3B - 3/4

UPPER TRACES

These traces illustrate typical CHARACTER DRIVER (DIAGRAM 8) outputs. The outputs are taken from the collector of TR9 instead of the 'floating' collector of TR3, providing a well defined pulse.

LOWER TRACES

These traces illustrate typical 7-BAR SEGMENT DRIVER (DIAGRAM 8) outputs. The outputs are taken from the 'a' bar output, the collector of TR13, and are as follows.

Trace 3B-3 shows the 'a' bar segment, aligned underneath the 3rd character driver output, in a de-energised state. This depicts the missing 'a' bar of the figure 4 in this example.

Trace 3B-4 shows the 'a' bar segment in the energised state, in this example the top of the figure 3.

NOTE:- The traces 3B-3/4 were taken with the BCD Output Module, and its inherent pull-up effect on the SEGMENT DRIVERS, fitted. Under this condition the trace of any bar not selected is pulled up. If tested without this pull-up effect, the position of the non-selected bar trace is indeterminate.

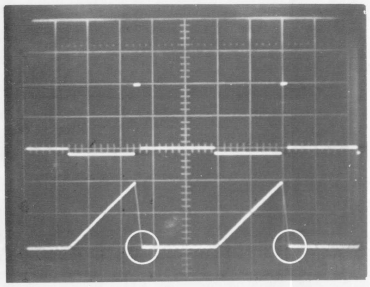
FRAME 3B-5

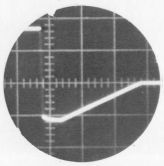
UPPER TRACE

Typical output waveform at IC7-pin 19 of clock input phase ϕ 1 - refer CLOCK DRIVERS (DIAGRAM 9).

LOWER TRACE

This is the clock input at IC7-pin 20 in phase ϕ 2.

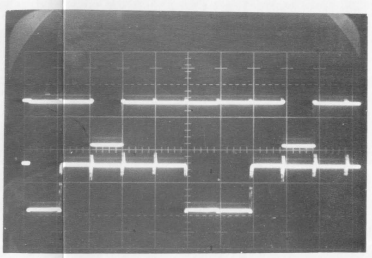




Time/cm:- 50ms.

Volts/cm:- 5V.

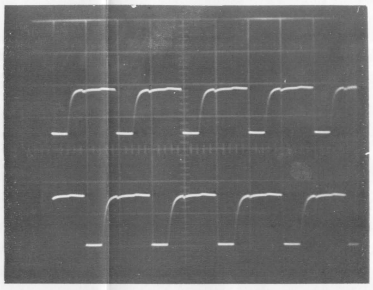
Frame 3B-1 Typical Integrator waveforms.



Time/cm:- 200μs.

Volts/cm:- 5V.

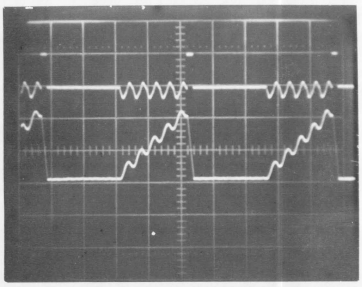
Frame 3B-3 3rd Character with 'a' Segment de-energised (e.g. numeral 4).



Time/cm:- 5μs.

Volts/cm:- 20V.

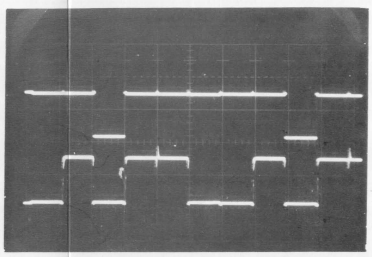
Frame 3B-5 Typical Clock waveforms.



Time/cm:- 50ms.

Volts/cm:- 10V.

Frame 3B-2 Typical Integrator waveforms with ac interference.



Time/cm:- 200μs.

Volts/cm:- 5V.

Frame 3B-4 3rd Character with 'a' Segment energised (e.g. numeral 3).

REFERENCE SWITCHING

REFERENCE VOLTAGE SOURCE

IC8 is connected as a non-inverting amplifier amplifying the voltage of reference zener D38 to give + 10V adjusted by means of R97 to 101 and RV7 to give correct calibration. The output is +10.000V for use as a positive coarse reference. R93/R94 form a potential divider to provide + 100mV for use as positive fine reference.

INVERTER

IC9 is connected as an inverter to produce - 10.000V from the REFERENCE VOLTAGE SOURCE. RV8 is adjusted to compensate for resistor tolerance and any dc offset. R104/R105 form a potential divider to provide - 100mV for use as negative fine reference.

EARTH CLAMP

During ramp-up, IC7-pin 12 goes high, thus via TR26 allowing TR15 to conduct to apply the unknown input signal to the A/D Converter. Similarly, TR16 is turned off thus unclamping the INPUT BUFFER AMPLIFIER from signal earth. At the end of ramp-up, IC7-pin 12 goes low, thus turning off TR15 and reclamping the INPUT BUFFER AMPLIFIER to earth via TR16.

INPUT BUFFER AMPLIFIER

A buffer stage providing input isolation to the INTEGRATOR (DIAGRAM 7). RV3 is provided for trimming out any internal voltage offset of IC3 while RV4 adjusts the input current compensation.

INPUT SWITCH DRIVER and INPUT SWITCH

During ramp-up, IC7-pin 18 goes low, applying the unknown input signal to the INTEGRATOR (DIAGRAM 7). TR17 is chosen such that the FET switches TR18 or TR19 in the COARSE REFERENCE SWITCHES and TR17 are of equal impedance to the INTEGRATOR (DIAGRAM 7) during both ramp-up and the appropriate coarse ramp-down period.

(Refer to the FET Selection Procedure in the APPENDIX of this manual for details of selection).

NEG. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a positive input signal during ramp-up, IC7-pin 17 goes low during the coarse ramp-down period. This turns on TR19 applying -10.000V as a negative reference input to discharge the level (proportional to the applied input signal) stored on the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

NEG. FINE REFERENCE SWITCH

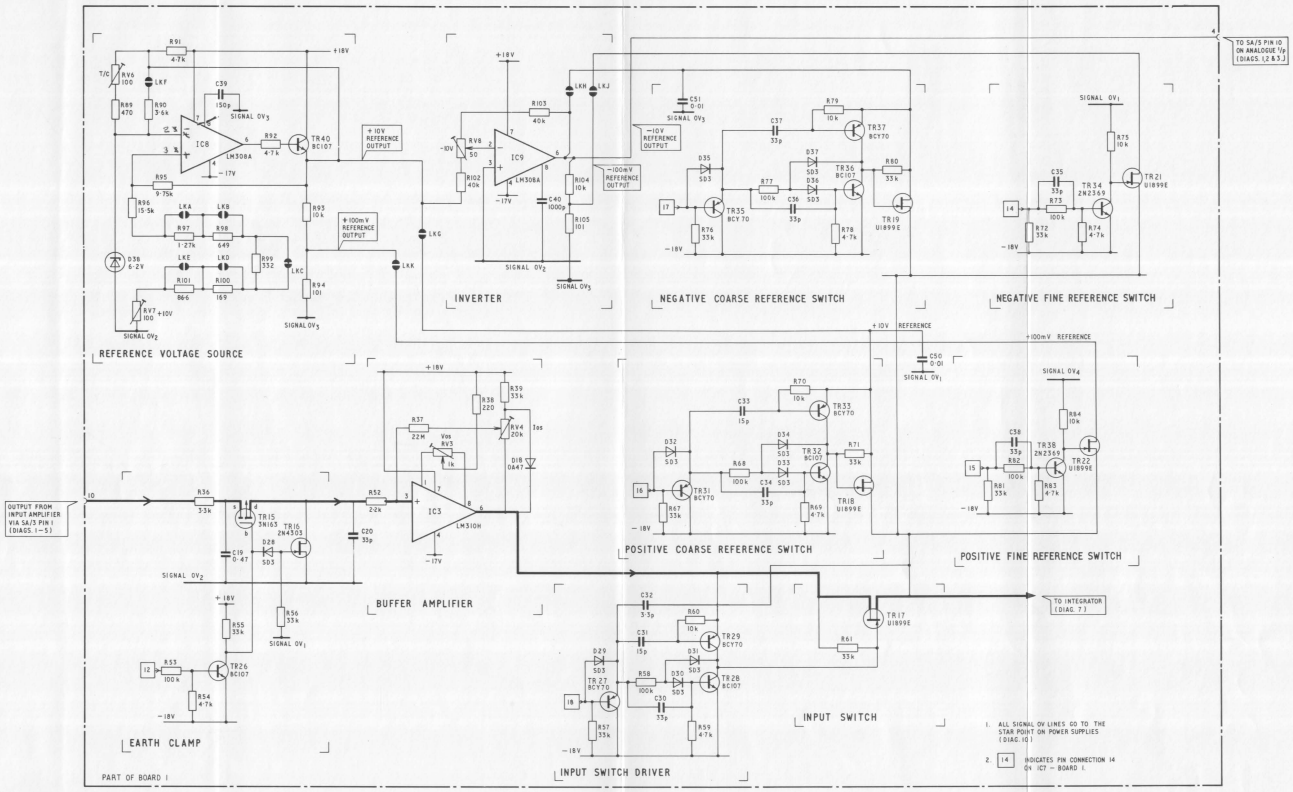
If the input signal was negative during ramp-up, IC7-pin 14 goes low, turning on TR21 during the fine ramp-down period to apply - 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).

POS. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a negative input signal during ramp-up, IC7-pin 16 goes low during the coarse ramp-down period. This turns on TR18 applying +10.000V as a positive reference input to discharge the level (proportional to the applied input signal) stored in the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

POS. FINE REFERENCE SWITCH

If the input signal was positive during ramp-up, IC7-pin 15 goes low, turning on TR22 during the fine ramp-down period to apply + 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).



6 *REFERENCE SWITCHING CIRCUIT DIAGRAM*

INTEGRATOR

INTEGRATOR

IC4 is connected as an operational integrator. The signal input is applied to one side of a differential stage formed by TR23. The other input is a dc level stored in the DRIFT CORRECT circuitry by C23. This maintains the 'virtual earth' of the integrator at 0V with respect to the output of the INPUT BUFFER AMPLIFIER (DIAGRAM 6) and therefore eliminates drift.

X1000 AMPLIFIER

The X1000 amplifier stage is to enable the COMPARATOR to detect very low integrator outputs, thus accurately defining the end of each ramp-down period.

COMPARATOR

The output of the X1000 AMPLIFIER is compared with earth; for a positive input, the output of IC6 will be negative; similarly for a negative input, the output will be positive. The purpose of the comparator is to detect when the input changes from one polarity to the other i.e. when the INTEGRATOR output passes through zero signifying the end of coarse or fine ramp-down as appropriate. The state of this output after completion of ramp-up determines the polarity of the applied coarse and fine reference drives used during the remainder of the measurement cycle. An output of $<+0.5V$ corresponds to positive polarity. A level $>+10V$ corresponds to negative polarity.

DRIFT CORRECT

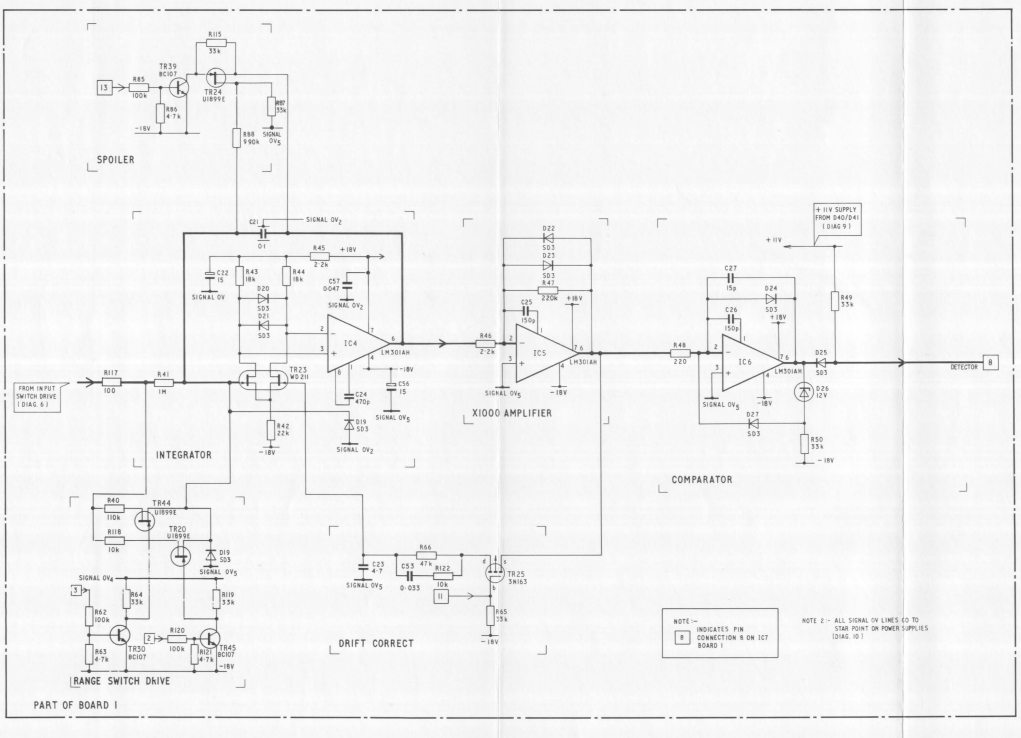
Between the end of fine ramp-down and the start of the next ramp-up, IC7-pin 11 goes low, turns on TR25 and charges up C23 to the level of the combined offset errors of the INTEGRATOR and INPUT BUFFER AMPLIFIER (DIAGRAM 6) so that during the ramp-up and ramp-down periods, these offsets are compensated for.

SPOILER

At the end of ramp-up, IC7-pin 13 goes low, TR24 conducts to allow a small proportion of the INTEGRATOR output to be applied to TR23 to hold the charge on C21 until a "mains zero crossing" occurs, thus enhancing series mode rejection.

RANGE SWITCH DRIVE

When IC7 pin 2 goes low, TR43 is turned off. TR30 is turned off and TR20 turned on. Also if IC7 pin 3 is low TR30 is turned off and TR20 turned on. Thus if either IC7 pin 2 or 3 is low the Integrator input resistance of 100kΩ (R40//R41) is selected.



7 *INTEGRATOR CIRCUIT DIAGRAM*

DISPLAY

7-BAR SEGMENT DRIVERS

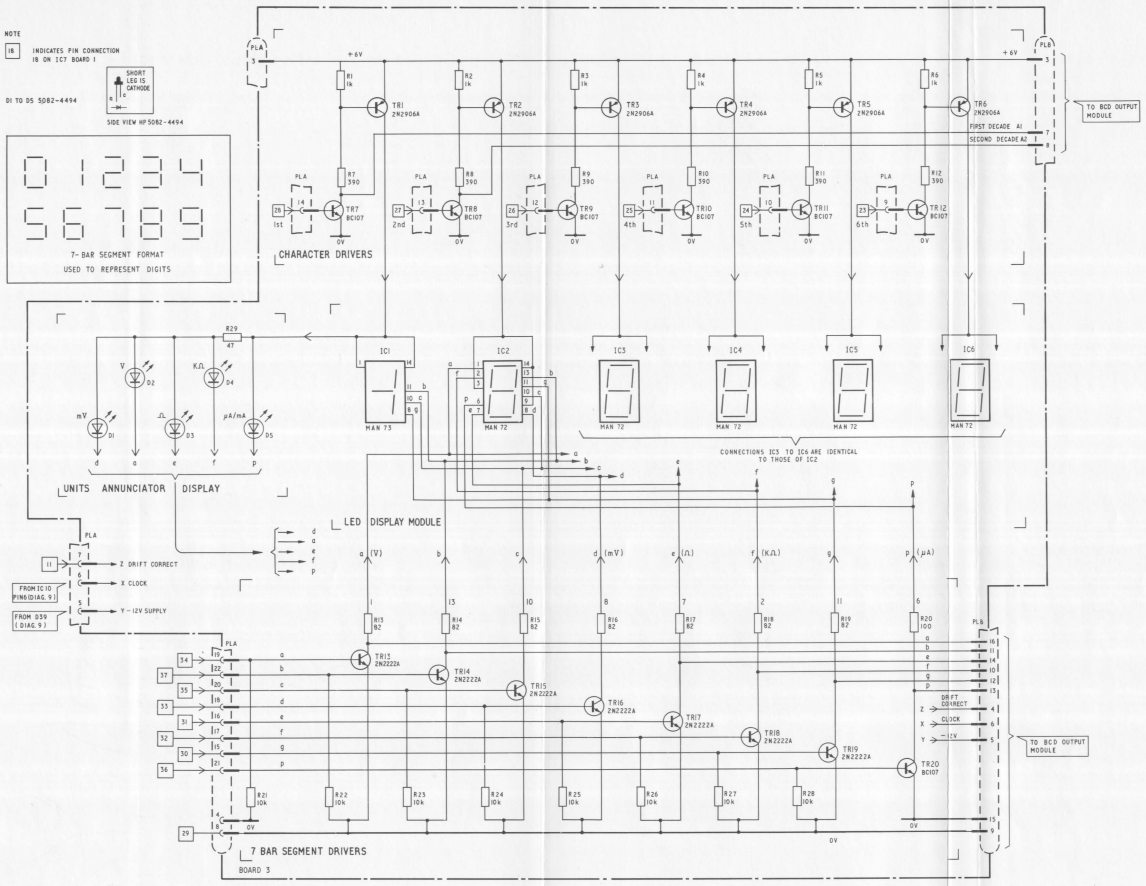
When the relevant output of IC7 goes Hi, the appropriate segment in the display will be lit up, provided that particular character has been selected. For example if IC7 pin 30 goes Hi all the 'g' bars will be selected instantaneously. Since only one CHARACTER DRIVER can be selected at any one time, only the 'g' bar on the selected character will be lit up.

CHARACTER DRIVERS

The characters are displayed serially commencing with the most significant. Whenever the appropriate character input goes Hi all the selected segments within that character will be energised and will light up.

UNITS ANNUNCIATOR DISPLAY

Whenever IC7 pin 28 goes Hi together with any bar segment driver representing a Unit Annunciator (d, a, e, f and p), the affected indicator will light up (mV, V, Ω, kΩ and μA respectively).



8 *DISPLAY CIRCUIT DIAGRAM*

CLOCK AND MODE SELECTION

CLOCK OSCILLATOR

A stable crystal controlled oscillator producing a source of timing pulses at 404kHz.

DIVIDE BY 4

A binary divider stage dividing the input signal by a factor of 4. The resultant output frequency of each output is 101kHz. Reference should be made to the text for details of the phase relationship between each output.

CLOCK DRIVERS

The input clock pulse train (101kHz) drives TR41 and TR42 on and off, forming output pulses between +11V and −17V (maximum amplitude = 28.5V) which are of sufficient amplitude to drive the clock inputs of IC7 (MOS - LSI circuit).

MODE SELECTION SWITCH

At each switch position, the appropriate input of IC7 will be held low thus selecting the appropriate mode. When VDC is selected, all the mode inputs go high and the DC mode is assumed.

RELAY DRIVE

Whenever IC7-pin 38 goes high, relay RLB is energised. Diode D10 (Bd. 2) provides a discharge path for the relay coil back emf when the relay is turned off. Whenever IC7 pin 2 is low TR13 is off and TR14 is on. Thus RLC is energised. Diode D11 (Bd. 2) provides a discharge path for the relay coil back emf when the relay is turned off.

AC Ranging Delay

When RLC is energised IC7 pin 6 drops to −17.5V on a time constant of C49, and 100k ohm (internal resistance in IC7), giving a delay of approximately two readings. D41 clamps C49 (+Ve) to Vss when RLC is de-energised.

IC7 (MOS - LSI) INTEGRATED CIRCUIT

IC7 is illustrated with its function identities and the diagram numbers on which these functions are effected.

The logic used by IC7 is as follows.

Positive Logic:-	Bar Drivers	Negative Logic:-	The remaining functions except the following:-
	IC Drivers (Characters)		Detector
	Top Range		Line Frequency
			Clock (ϕ_1 and ϕ_2)
			Supply Rails

Supply Rail voltages are:-

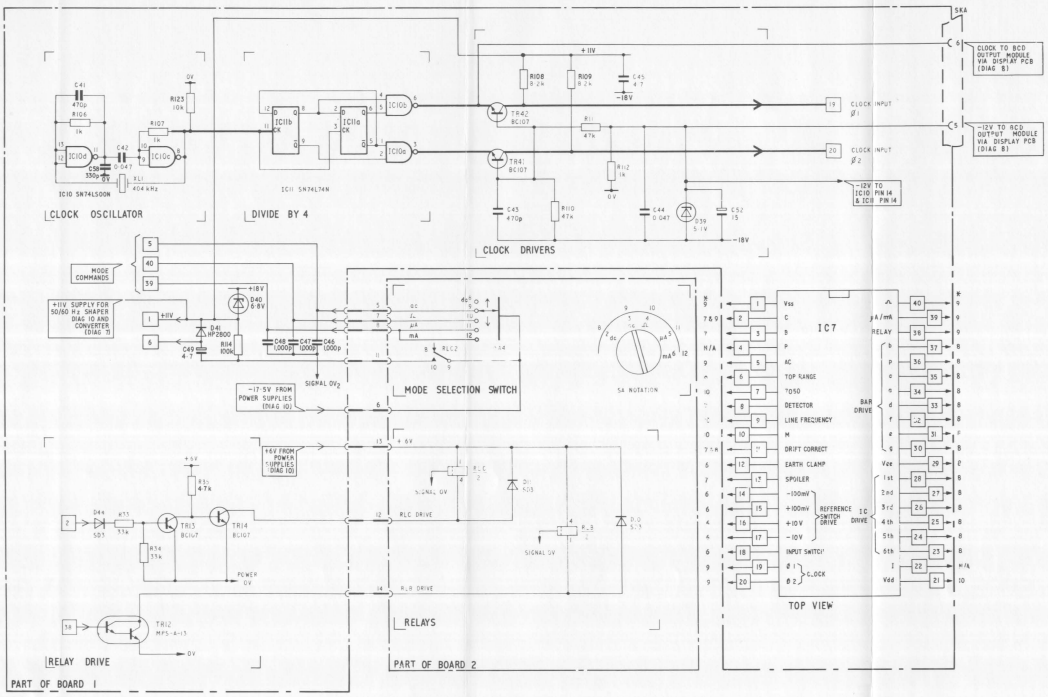
Vss = 11V Nominal

Vdd = −18V Nominal

Vee = 0V

NOTES:- 1. Terminals marked N/A are not used and must not be connected to any other part of the circuitry.

2. Before attempting to remove this MOS Integrated Circuit ensure that all power supplies are switched off and that the necessary anti-static charge measures are taken. See warning on page 3b-5.



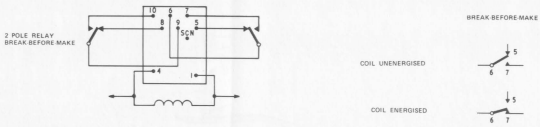
NOTES:—

1 RELAY CONTACTS ARE SHOWN ON DIAGRAMS
5 AC MODE RLB2, RLC1
1-3 ANALOGUE INPUT RLB 1
9 MODE SELECTION RLC2

2 [2] INDICATES PIN CONNECTION 2 ON IC7 BOARD 1

3 ALL 0V AND SIGNAL 0V LINES GO TO STAR POINT ON POWER SUPPLIES (DIAG 10)

4 NUMBERS UNDER ✱ DENOTE DIAGRAMS WHICH ARE AFFECTED



9 CLOCK AND MODE SELECTION CIRCUIT DIAGRAM

SUB SECTION 3c Power Supplies

This sub-section deals with the POWER SUPPLIES section of the instrument whose primary function is to provide all the internal dc levels required to operate the instrument.

POWER SUPPLIES

GENERAL ARRANGEMENT

This section of circuitry provides all the dc voltage levels required to operate the instrument.

0V Rails.

Within the instrument, the common return paths (0V rails) are carefully separated to reduce interference. Care should be taken not to short these rails together other than where shown.

Split Pads LKL and LKM (pcb No. 1)

These pads enable the user to isolate the stabilised supplies from the associated section of circuitry. Since these pads are continuations of the printed circuit copper work, care should be taken not to overheat these connections causing the track to lift away from the board.

50/60Hz SHAPER

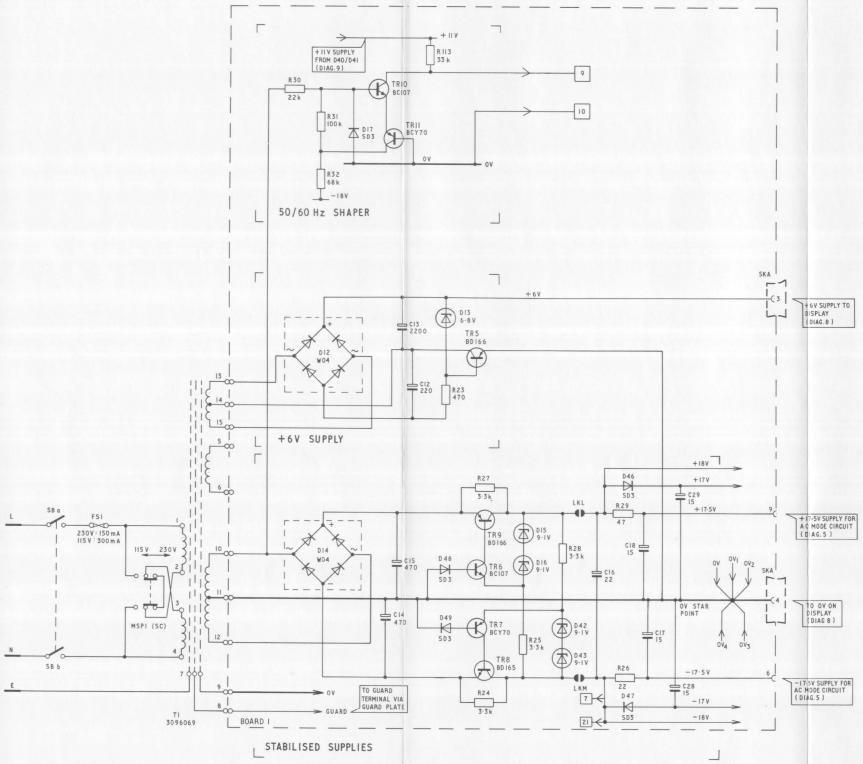
A small proportion of the incoming mains frequency is sampled; the signal is clipped and is used by IC7 (MOS-LS1 circuit) to provide mains zero timing reference points.

VOLTAGE RAIL USAGE

The following table gives the nominal rail voltages provided and the circuit diagrams on which they appear.

+18V	4, 6, 7, 9
−18V	4, 6, 7, 9, 10
+17.5V	4, 5
−17.5V	4, 5, 9
+17V	7,
−17V	6, 7
+6V	8, 9

A nominal 10V rms output is available from transformer T1, terminals 5 and 6 for use on the BCD Output Module.



10 *POWER SUPPLIES CIRCUIT DIAGRAM*

SECTION 4 Setting Up & Calibration

INTRODUCTION

This section provides a comprehensive setting-up and calibration procedure which may be necessary after a rectification and/or component replacement on the Digital Multimeter.

It is divided into two parts as follows.

1. Setting-Up Procedures

   These involve partial strip down of the instrument in order to effect initial adjustments of the circuit parameters.

2. Calibration Procedures

   The final adjustments to provide an instrument performance which is compatible with the specification published in Section 6 of this manual.

   For a normal calibration only Part 2 of this section needs to be carried out. Where an instrument fails a calibration, or has had a rectification and/or component replacement, it is advisable to carry out the full procedure detailed in this section.

NOTE:- It is essential when carrying out Part 1 or 2, that the procedure be completed, and carried out in the order given.

TEST EQUIPMENT

The test equipment used must have an accuracy uncertainty equal to or better than that shown in the calibration test tables.

The following test equipment should be available to perform the following procedures correctly.

(a) Variac.

(b) Digital Voltmeter (e.g. Type 7040).

(c) Oscilloscope Type 1740 or A100.

(d) Decade Resistance Standard (e.g. ESI Model RS624).

(e) AC Voltage Standard (e.g. Hewlett Packard Models 745A and 746A).

(f) Decade Voltage Divider (e.g. ESI Model RV622A).

(g) AC Source (e.g. Bradley 232).

(h) DC Source (e.g. Time Model 2003, ± 0.02%).

(j) DC Voltage Standard (e.g. Kintel 351).

(k) Thermal Probe (ambient + 20^{o}C).

(l) 1A current Source (e.g. Fluke 382A)

(m) Resistance Standard 1Ω ± 0.005% 4 terminal (e.g. Cropico RS1)

(n) Additional items: Resistor, 1k ohm ± 10% (0.125W).

Resistor, 27k ohm ± 10% (0.125W).

Resistor, 1M ohm ± 10% (0.125W).

Capacitor 1μF (non-polarised).

PART 1. SETTING UP PROCEDURES

PRELIMINARY

1. Prepare the instrument as follows:-

CAUTION:- IT IS ESSENTIAL THAT THE INSTRUMENT BE ISOLATED FROM THE MAINS SUPPLY BEFORE OUTER CASE REMOVAL, DUE TO THE UNCOVERED TERMINALS ON THE ON/OFF SWITCH.

CAUTION:- BEWARE OF GUARD POTENTIAL ON GUARD PLATE WITH INSTRUMENT CASE REMOVED.

a. Remove the 4, 2.5mm screws holding the outer case to the rear panel assembly, Fig. 4.1.

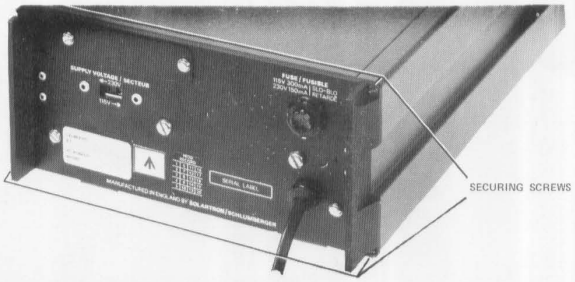


Fig. 4.1. View of Rear Panel, showing location of the 4 securing screws.

b. Select the 'V.DC' mode (This orientates the selector switch shaft with it's key flat facing upwards).

c. Remove the GUARD - Lo link (if fitted).

d. Gently ease out the pcb and rear panel assembly away from the front panel. Fig. 4.5, at rear of section, shows the location and function of each potentiometer.

e. Remove the 2 sets of Berg pins and the 4 screws attaching pcb 2 to pcb 1. Remove pcb 2.

2. Link Berg socket 2 to Berg socket 10.

3. Check that the Mains Selector in the rear panel is set to the appropriate voltage, and that the correct rated fuse is fitted.

For	230V:-	150mA	SLO BLO FUSE
	115V:-	300mA	SLO BLO FUSE

4. Apply power to the instrument and allow a sufficient warm up period.

5. Check that the rail voltages are within the limits specified over the input voltage range as follows.

For	230V:-	195.5 to 253 Volts.
	115V:-	97.75 to 126.5 Volts.

TEST BETWEEN	LIMITS OVER MAINS VARIATION	
	MINIMUM	MAXIMUM
C16 (+ve) to C18 (–ve)	+16.5V	+18.5V
C16 (–ve) to C18 (–ve)	–16.5V	–18.5V
C13 (+ve) to C18 (–ve)	+5.7V	+7.0V
C45 (+ve) to C45 (–ve)	+25V	+30V
C52 (+ve) to C52 (–ve)	+4.75V	+5.35V

REFERENCE TEMPERATURE COEFFICIENT

NOTE:- The potentiometer involved is RV6. Once set, great care must be exercised during the remainder of the procedure to prevent inadvertant adjustment of this potentiometer.

1. Select 'V.DC' mode. Remove link from Berg sockets 2 and 10 and apply –10V ± 0.1% absolute between them (negative to 10), using a DC Standard having a ½ hour stability of less than 5ppm.

2. Attach a variable resistance box (100k ohms to 1 ohm) between R96/R97 and C22 (–ve) of pcb 1. Adjust resistance box for a reading of 100.000 ± 10 bits.

3. Increase ambient temperature at D38 by 20°C (application of a Thermal Probe to D38 or by other means). Adjust RV6 and/or link LKF for 100.000 reading.

4. Allow D38 temperature to return to ambient and re-adjust resistance box for a reading of 100,000 ± 10 bits.

5. Re-apply heat of ambient + 20°C ± 4°C. Reading should change by less than ± 5 bits. Repeat adjustments until change is less than ± 5 bits. Remove the –10V supply and resistance box.

BUFFER Vos Ios

1. Select 'V.DC' mode. Short circuit Berg sockets 2 and 10. Connect voltmeter between Berg socket 2 and D18 cathode, via a 1k ohm resistor.

2. Adjust RV3 for 0 ± 20μV on voltmeter. Replace the link between Berg sockets 2 and 10 by a 27k ohm resistor.

3. Adjust RV4 for 0 ± 10μV on the voltmeter. Remove voltmeter and two resistors (27k ohm and 1k ohm).

SPOILER

1. Select 'V.DC' mode. Link Berg sockets 4 and 10.

2. Connect TR26 collector (case) via a 33k ohm resistor to TR10 collector (case) and note instrument reading.

3. Remove the resistor connection and adjust RV5 to obtain the reading noted in (2) above.

4. Remove the 33k ohm resistor and the link between Berg sockets 4 and 10.

POSITIVE REFERENCE

Select 'V.DC' mode. Apply −10V and −1V, using the DC Standard and the Decavider, to Berg sockets 2 and 10 (−ve to 10) and adjust RV7 to share the error between −10,0000V (± 2 bits) and −1.00000 (± 2 bits) readings evenly.

NOTE:- If RV7 does not have enough adjustment the links will require re-adjustment as follows:-

a. Connect −10V (± 0.02% absolute) from DC Standard to Berg sockets 2 and 10 (Common to socket 2).

b. Ensure that links LKA to LKE inclusive are open circuit and that RV7 is at maximum resistance (fully clockwise).

c. Apply −10V standard and note the reading. Look up the range which includes this reading in Table 4.1 and set links LKA to LKE accordingly.

READING RANGES		LINKS				
		A	B	C	D	E
100000	100199	1	1	1	1	1
100172	100373	1	1	1	1	0
100337	100540	1	1	1	0	1
100513	100718	1	1	1	0	0
100669	100876	1	1	0	1	1
100848	101056	1	1	0	1	0
101020	101230	1	1	0	0	1
101202	101414	1	1	0	0	0
101332	101546	1	0	1	1	1
101517	101734	1	0	1	1	0
101696	101914	1	0	1	0	1
101885	102105	1	0	1	0	0
102053	102276	1	0	0	1	1
102246	102471	1	0	0	1	0
102431	102658	1	0	0	0	1
102628	102858	1	0	0	0	0
102704	102935	0	1	1	1	1
102904	103137	0	1	1	1	0
103096	103331	0	1	1	0	1
103299	103537	0	1	1	0	0
103481	103721	0	1	0	1	1
103689	103931	0	1	0	1	0
103888	104134	0	1	0	0	1
104101	104349	0	1	0	0	0
104252	104502	0	0	1	1	1
104469	104721	0	0	1	1	0
104677	104932	0	0	1	0	1
104897	105156	0	0	1	0	0
105094	105355	0	0	0	1	1
105320	105583	0	0	0	1	0
105537	105803	0	0	0	0	1
105767	106037	0	0	0	0	0

Legend

0 = Short Circuit

Table 4.1.

d. Repeat the −10V and −1V test as detailed previously.

RE-ASSEMBLY

1. Fit pcb 2 to pcb 1, securing it by the 4 screws.

2. Fit the link between GUARD and LO terminals and insert the 2 sets of Berg pins into their sockets, ensuring they are fully engaged.

INPUT AMPLIFIER

NOTE:- The waveform at TR3 collector, using a dc coupled oscilloscope set to 1V/cm and 1ms/cm, should be a square wave; amplitude 4V ± 0.4Vpp, period 4ms ± 1ms, mark/space ratio 1 : 1 ± 10%.

1. Select 'V.DC' mode and short circuit the input terminals. Ensure that RV1 range of adjustment is greater than ± 80μV.

2. Remove the short circuit from the input terminals. Apply +100μV and −100μV alternately to the input terminals, using a dc source having an output resistance of 10k ohms.

3. Adjust RV1 for equal positive and negative readings.

4. Remove dc source and connect a 1M ohm resistor and 1μF non-polarised capacitor in parallel between the Hi and Lo terminals.

5. Adjust RV2 for a zero reading, ± 10μV. Remove resistor and capacitor.

6. Recheck the Input Amplifier zero, (short circuiting the input terminals as in operation 1 above) and the ± 10V, (using the DC Standard across the input terminals) readings limits.

   These are:- ± 10μV ± 1 bit for zero input.

   ± 10V ± 2 bits for the 10V input.

   NOTE:- If adjustment is necessary repeat operations 2 to 5 inclusive.

7. Remove the dc source.

NEGATIVE REFERENCE

1. Select 'V.DC' mode.

2. Connect 10V ± 0.02% absolute across the 6 decade Decavider, using the DC Standard.

3. Apply +10V, −10V, +1V and −1V dc in turn to the input terminals.

4. Adjust on RV8 to make the negative reading equal to the positive reading at each voltage level.

5. Share errors between RV7 and RV8 such that the:-

   ± 10V readings are ± 10.0000V ± 2 bits

   ± 1V readings are ± 1.00000V ± 2 bits

   NOTE:- Problems in meeting these limits will result if the 'ON' resistance of TR's 17, 18, 19 and 20 are not matched. See Appendix.

LINEARITY

1. Select 'V.DC' mode. With the 10V DC Standard and Decavider connected to the input terminals as in previous test, check the linearity in accordance with Table 4.2.

INPUT	READING	TOLERANCE
10V	10.0000V	± 3 bits
5V	5.0000V	± 2 bits
1.05V	1.0500V	± 2 bits
0.95V	*950.00mV	± 2 bits
1.05V	1.05000V	± 2 bits
1.15V	*1.1500V	± 2 bits
0.5	*500.00mV	± 2 bits
0.1	100.00mV	± 2 bits
0.01	10.00mV	± 2 bits
0.001	1.00mV	± 2 bits
0.0001	0.10mV	± 2 bits
0.00005	0.05mV	± 2 bits
0.00003	0.03	± 2 bits
0.00002	0.02mV	± 2 bits
0.00001	0.01mV	± 2 bits

* = Range Change

Table 4.2

2. Repeat for negative values using the same voltage source.

3. If the DMM falls outside the linearity tolerances, it is recommended that the Setting Up Procedure should be repeated.

OHMS MODE

1. Set to 'Ω' mode and short circuit the input terminals. The reading should be less than 3 bits.

2. Connect 100k ohms ± 0.01% absolute across the input terminals. Adjust RV2 (pcb 2) and/or link LKY to obtain 100.000kΩ reading.

DC ATTENUATOR

Select 'V.DC' mode and connect input terminals to 100V ± 0.01% absolute. Adjust RV1 (pcb 2) and/or link LKX to give 100.000V reading.

DC μA

Select 'μA.DC' mode and connect input to 1000μA ± 0.01% absolute current source (100k ohms from 100V is convenient). Adjust RV6 (pcb 2) to give 1000.00μA ± 10 bits reading.

DC mA

1. Select 'ma DC' mode, and open circuit terminals. Reading should be 0.00mA ±10 bits (excluding noise, which should not exceed 14 bits). Adjust RV1 as required.

Note: If adjustment of RV1 is necessary to achieve the specified reading, the INPUT AMPLIFIER checks and adjustment will have to be repeated.

2. Connect 95/950mA Current Source in series with 1Ω ±0.01% Standard Resistor to the input terminals, monitoring the voltage across the Resistor with a voltmeter calibrated to ±0.01%. accuracy (e.g. 7050 dvm).

3. Adjust the current source for a nominal 500.0mV ±10% reading on the monitor voltmeter. Adjust RV9 on pcb 2 to give the same reading of 500.00mA ±5 bits.

4. Increase the current to 950mA ±10% and check that the reading will hold for 1 minute.

5. Remove the Current Source.

AC ZERO

Switch to 'V.AC' mode. Short circuit TR1 (pcb 2) collector (case) to 0V. Adjust RV4 until the readings stop reducing. Reading must be less than 5 bits. Remove the short circuit.

AC SCALE

1. Select 'V.AC' mode. Connect the input to 1V ± 0.1% absolute 1kHz sinewave. On pcb 2, adjust RV3 and link LKZ to give 1.00000V, with at least ± 50 bit adjustment on RV3.

AC ATTENUATOR

1. Select 'V.AC' mode. Connect the input to 10V ± 0.2% absolute 1kHz sinewave. Adjust RV4 (pcb 2) to obtain 10.0000V ± 50 bits.

2. Increase the input to 100V ± 0.2 absolute 1kHz sinewave. Adjust RV5 (pcb 2) to obtain 100.000V ± 50 bits.

INTERFERENCE REJECTION

SERIES MODE

1. Connect instrument as shown in Fig. 4.2.

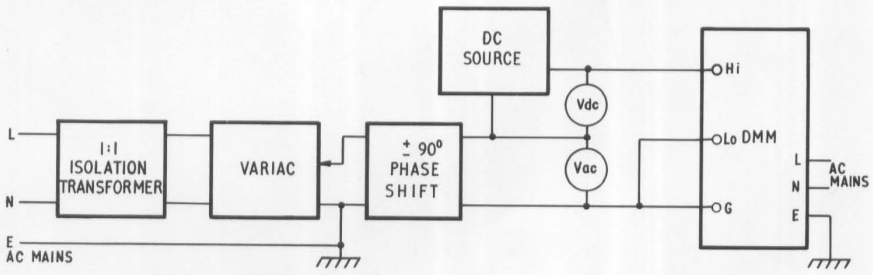


Fig. 4.2. Interference Rejection:- Series Mode Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to approximately 500mV and (V.ac) to zero. Note the instrument reading.

3. Increase (V.ac) to 1 Volt. Reading must not change by more than 1mV.

COMMON MODE

AC Rejection

1. Connect instrument as shown in Fig. 4.3.

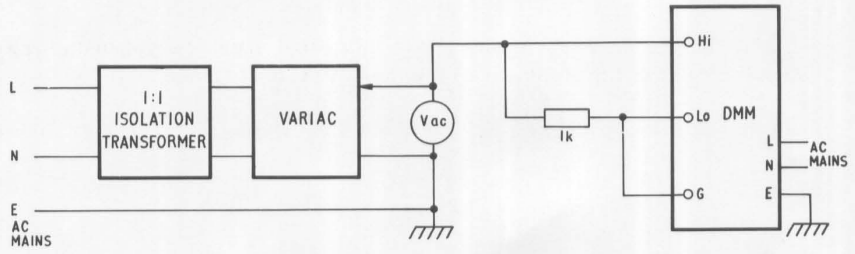


Fig. 4.3. Interference Rejection:- Common Mode (ac) Test Circuit.

2. Switch to 'V.AC' mode and set (V.ac) to 100V. Reading shall be less than 100mV.

DC Rejection

1. Connect instrument as shown in Fig. 4.4.

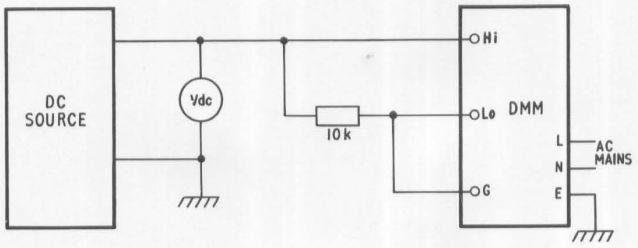


Fig. 4.4. Interference Rejection:- Common Mode (dc) Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to 500V. Reading shall be less than 5mV.

This concludes the setting up of the DMM and it should now be followed by a full calibration.

PART 2. CALIBRATION PROCEDURES

INTRODUCTION

The following calibration is basically the final calibration to which all instruments are subjected, prior to despatch from the factory.

For the greatest accuracy the DMM should be removed from its case and fitted into a Setting Up Case, Part No. 70502 before a calibration is attempted. Failing this, allowances must be made for variations in the working temperatures.

See Appendix for details of Setting Up Case.

PRELIMINARY PROCEDURE

The DMM will have to be removed from its case and fitted into the Setting Up Case (if available).

CAUTIONARY NOTES

1. IT IS ESSENTIAL THAT THE INSTRUMENT BE COMPLETELY ISOLATED FROM THE MAINS SUPPLY BEFORE REMOVING THE CASE, DUE TO THE POSITION AND UNPROTECTED NATURE OF THE ON/OFF SWITCH TERMINALS.

2. BEWARE OF THE GUARD PLATE POTENTIAL WITH INSTRUMENT CASE REMOVED.

1. Remove the 4, 2.5mm screws which secure the DMM case to the rear panel. See Fig. 4.1.

2. Remove the GUARD - Lo link (if fitted).

3. Gently ease out the rear panel and pcb assembly, away from the front panel.

4. Fit assembly into the Setting Up Case (if available), or position assembly in convenient position with the guard plate insulated if required and with easy access to the potentiometers.

5. Ensure that the correct mains selection has been made and that the correct rated fuse is fitted.

   For 230V:- 150mA SLO BLO

   115V:- 300mA SLO BLO

CALIBRATION

The calibration sequence must be carried out in the order given. Calibration should be carried out at an ambient temperature $23^{o}C \pm 1^{o}C$ after a warm-up period of approximately half an hour in the Setting-Up Case.

STANDARD SETTINGS

During the warm up period the DMM should be set to the following standard conditions.

1. Mode set to 'V.DC'.

2. Input terminals short circuited.

3. Apply power to the DMM and switch instrument ON.

CALIBRATION PROCEDURE 1

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	1MΩ/1μF	10	Adj. Bd.1/RV2	±0.00mV	2	
2	S/C	–	Adj. Bd.1/RV1	±0.00mV	0	
3	1MΩ/1μF	10	Adj. Bd.1/RV2	±0.00mV	10	
4	+0.10mV	2	Adj. Bd.1/RV1 and repeat for equal +ve and –ve readings.	0.10mV	2	
5	–0.10mV	2		–0.10mV	2	
6	S/C	–	Check	±0.00mV	2	
7	+9.5000V	0.001	Adj.Bd.1/RV7 (1)	9.5000V	2	
8	+9.5000V	0.001	Check with 1MΩ in series.	9.5000V	50	
9	–9.5000V	0.001	Adj. Bd.1/RV8 (1)	–9.5000V	3	

NOTES:-

(1) Adjust for equal reading, split any deviations equally between readings.

CALIBRATION PROCEDURE 2

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	105.000kΩ	0.001	Adj. Bd.2/RV2	105,000kΩ	5	
2	50.000kΩ	0.002	Check	50.000kΩ	9	
3	5kΩ	–	–	–	–	
4	10.5000kΩ	0.002	Check	10.5000kΩ	10	
5	5.0000kΩ	0.005	Check	5.0000kΩ	8	
6	867.829Ω	0.005	Check	867.8Ω	4	
7	1.0500kΩ	0.005	Check	1.0500kΩ	7	
8	O/C	–	Overload Check (1)	1–––––kΩ	–	
9	S/C	–	Check	0.0Ω	4	

NOTES:-

(1) Ensure that overload condition is indicated by a steady '1' being displayed and that the remaining 5 characters are blanked out.

CALIBRATION PROCEDURE 3

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	+9.5000	0.001	Check	9.5000	3	
2	+1.2000V	0.002	Check	1.2000V	2	
3	+0.9500V	0.001	Check	950.00mV	5	
4	+95.00mV	0.002	Check	95.00mV	2	
5	+10.00mV	0.02	Check	10.00mV	2	
6	−9.5000V	0.001	Check	−9.5000V	4	
7	1.2000	0.002	Check	1.2000V	2	
8	−0.95000	0.001	Check	−950.00mV	5	
9	−95.00mV	0.002	Check	−95.00mV	2	
10	−10.00mV	0.02	Check	−10.00mV	2	
11	+95.000V	0.001	Adj. Bd 2/RV1	95.000V	2	
12	+1000.00	0.005	Check	1000.00	9	
13	−120.00V	0.002	Check	−120.00V	3	

CALIBRATION PROCEDURE 4

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	1.05000MΩ	0.005	Check	1050.00kΩ	19	
2	500.00kΩ	0.005	Check	500.00kΩ	10	
3	10.0000MΩ	0.01	Check	10000.0kΩ	34	
4	5.0000MΩ	0.01	Check	5000.0kΩ	19	

CALIBRATION PROCEDURE 5

Select 'μA.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	OC	–	Check	±0.000μA	4	
2	+1.00000mA	0.005	Adj. Bd2/RV6	1000.00μA	30	
3	+9.000μA	0.005	Check	9.000μA	5	
4	+1.000μA	0.05	Check	1.000μA	4	
5	–20V	10	Overload Check	–1–––μA	–	
6	–1.00000mA	0.005	Check	–1000.00μA	30	
7	–9.000μA	0.005	Check	–9.000μA	5	
8	–1.000μA	0.05	Check	–1.000μA	4	

NOTES:-

(1) Recommend 100V source via a 100k ohm resistor.

(2) Recommend 9V source via a 1M ohm resistor.

(3) Recommend 10V source via a 1M ohm resistor.

(4) Recommend 1V source via a 1M ohm resistor.

(5) Ensure that overload is indicated by flashing '1' with the remaining 5 characters blanked out.

(6) For adjustment of this potentiometer the case must be removed.

CALIBRATION PROCEDURE 6

Select 'mA DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	O/C		Check	0.000mA	30	
2	95.00mA	0.01	Check	95.000mA	70	

CALIBRATION PROCEDURE 7

Select 'V.AC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	±bits	
1	0.95000V	0.02	At 1kHz Adjust Bd. 2/RV3	950.00mV	20	
2	1.00mV	1	At 1kHz Check	1.00mV	9	
3	S/C		Check	0.00	9	
4	500.00mV	0.02	At 1kHz Check	500.00mV	20	
5	95.00mV	0.02	At 1kHz Check	95.00mV	15	
6	0.95000V	0.02	At 40Hz Check	950.00mV	100	
7	0.95000V	0.02	At 20kHz Check	950.00mV	100	
8	0.95000V	0.02	At 10kHz Check	950.00mV	100	
9	95.00mV	0.02	At 20kHz Check	95.00mV	18	
10	9.5000V	0.02	At 1kHz Adjust Bd. 2/RV4 (1)	9.5000V	20	
11	95.000V	0.02	At 1kHz. Adjust Bd. 2/RV5 (1)	95.000V	20	
12	1.2000V	0.02	At 1kHz Check	1.2000V	20	
13	9.5000V	0.02	At 20kHz Check	9.5000V	150	
14	95.000V	0.02	At 20kHz Check	95.000V	150	
15	750.00V	0.05	At 1kHz Check	750.00V	50	
16	500.00V	0.05	At 10kHz Check	500.00V	100	
17	9.5000V	0.02	At 10kHz Check	9.5000V	150	

NOTES:

(1) For adjustment of this potentiometer the case must be removed.

This concludes the calibration of the DMM. If the instrument fails any of the prescribed tests it is suggested that the Setting Up Procedures in Section 4 be carried out, followed by a further calibration before any fault diagnosis is attempted.

The serviceable DMM should now be isolated from the supplies and refitted into its case.

NOTE:- Ensure that 'V.DC' is selected on both the switch and the front panel knob to ensure correct mating of the key flat.

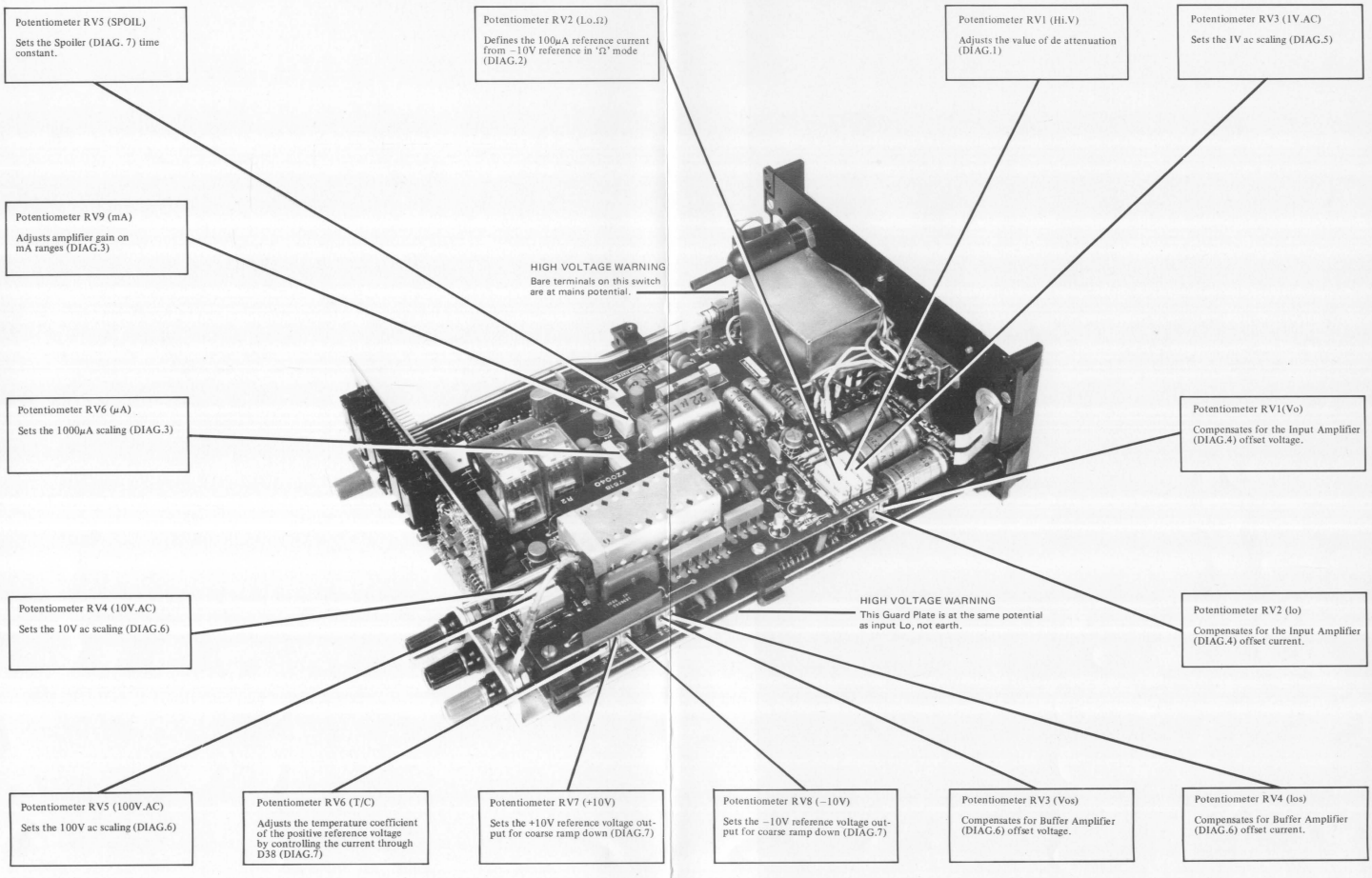


Fig. 4.5. View of PCB Assembly, identifying the Potentiometers and their Functions.

SECTION 5 Parts Lists

This section contains detailed parts lists for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts list.

COMPONENT PARTS LIST

ABBREVIATIONS

Circuit References

B	Battery
C	Capacitor (μF)
CSR	Thyristor
D	Diode
FS	Fuse
IC	Integrated Circuit
L	Inductor
LP	Lamp (including Neon)
LK	Link
M	Meter
MSP	Mains Selector Panel
PL	Plug
R	Resistor (Ω)
RL	Relay
S	Switch
SK	Socket
T	Transformer
TP	Terminal Post (or Test Point)
TR	Transistor
V	Valve
X	Other Components

Also Used:-

RNL	Non Linear Resistor (Ω)
RV	Variable Resistor (Ω)

Component Composition

FIXED RESISTORS

Carbon Composition	CACP
Carbon Film	CAFM
Cracked Carbon	CKCA
Metal Film	MEFM
Metal Oxide	MEOX
Power Wirewound	POWW
Precision Wirewound	PRWW
Temperature Sensitive	TEMP
Thick Film	TKFM
Thin Film	TNFM
Voltage Sensitive	VOLT

Component Composition (Cont'd)

VARIABLE RESISTORS

Wirewound Preset Single Turn	WWPS
Wirewound Preset Multiturn	WWPM
Wirewound Front Panel Single Turn	WWFS
Wirewound Front Panel Multiturn	WWFM
Carbon Preset Single Turn	CAPS
Carbon Preset Multiturn	CAPM
Carbon Front Panel Single Turn	CAFS
Carbon Front Panel Multiturn	CAFM
Cermet Preset Single Turn	CMPS
Cermet Preset Multiturn	CMPM
Cermet Front Panel Single Turn	CMFS
Cermet Front Panel Multiturn	CMFM

CAPACITORS

Air	AIR
Aluminium Electrolytic	ALME
Aluminium Solid	ALMS
Polycarbonate	CARB
Ceramic	CERM
Polyester Foil	ESTF
Polyester Metallised	ESTM
Glass	GLAS
Mica	MICA
Metallised Lacquer	MLAC
Paper Foil	PAPF
Paper Metallised	PAPM
PTFE	PTFE
Polypropylene Film	PYLN
Polystyrene	STYR
Tantalum Dry	TAND
Tantalum Foil	TANF
Tantalum Wet	TANW

PCB No. 1

Cct Ref.	General Description				Solartron Part No.
R1	CACP	1000	1/8W	10%	172031000
R2	CACP	470	1/8W	10%	172024700
R3	CACP	47k	1/8W	10%	172044700
R4	CACP	47k	1/8W	10%	172044700
R5	CACP	10	1/8W	10%	172011000
R6	CACP	1.5M	1/8W	10%	172061500
R7	CACP	220k	1/8W	10%	172052200
R8	CACP	22	1/8W	10%	172012200
R9	CACP	220k	1/8W	10%	172052200
R10	CACP	10k	1/8W	10%	172041000
R11	CACP	220k	1/8W	10%	172052200
R12	CACP	220k	1/8W	10%	172052200
R13	CACP	100	1/8W	10%	172021000
R14 to R19	MEOX	22k	1/4W	5%	195642200
R20	MEOX	9.1k	1/4W	5%	195639100
R21	MEOX	9.1k	1/4W	5%	195639100
R22	MEOX	100k	1/4W	5%	195651000
R23	MEOX	470	1/2W	5%	193524700
R24	CACP	3.3k	1/4W	10%	172333300
R25	CACP	3.3k	1/4W	10%	172333300
R26	CACP	22	1/8W	10%	172012200
R27	CACP	3.3k	1/4W	10%	172333300
R28	CACP	3.3k	1/4W	10%	172333300
R29	CACP	47	1/8W	10%	172014700
R30	CACP	22k	1/8W	10%	172042200
R31	CACP	100k	1/8W	10%	172051000
R32	CACP	68k	1/8W	10%	172046800
R33	CACP	33k	1/8W	10%	172043300
R34	CACP	33k	1/8W	10%	172043300
R35	CACP	4.7k	1/8W	10%	172034700
R36	CACP	3.3k	1/8W	10%	172033300
R37	CACP	22M	1/4W	10%	172372200
R38	CACP	220	1/8W	10%	172022200
R39	CACP	33k	1/8W	10%	172043300
R40	MEFM	110k	1/4W	0.5%	198251101
R41	MEFM	1M	1/4W	1%	198361002
R42	MEOX	22k	1/4W	5%	195642200
R43	MEFM	18k	1/8W	0.5%	192741802
R44	MEFM	18k	1/8W	0.5%	192741802
R45	CACP	2.2k	1/8W	10%	172032200
R46	CACP	2.2k	1/8W	10%	172032200
R47	CACP	2.2M	1/8W	10%	172062200
R48	CACP	220	1/8W	10%	172022200
R49	CACP	33k	1/8W	10%	172043300
R50	CACP	33k	1/8W	10%	172043300
R52	CACP	2.2k	1/8W	10%	172032200
R53	CACP	100k	1/8W	10%	172051000
R54	CACP	4.7k	1/8W	10%	172034700
R55	CACP	33k	1/8W	10%	172043300
R56	CACP	33k	1/8W	10%	172043300
R57	CACP	33k	1/8W	10%	172043300
R58	CACP	100k	1/8W	10%	172051000
R59	CACP	4.7k	1/8W	10%	172034700
R60	CACP	10k	1/8W	10%	172041000
R61	CACP	33k	1/8W	10%	172043300
R62	CACP	100k	1/8W	10%	172051000
R63	CACP	4.7k	1/8W	10%	172034700
R64	CACP	33k	1/8W	10%	172043300
R65	CACP	33k	1/8W	10%	172043300
R66	CACP	47k	1/8W	10%	172044700
R67	CACP	33k	1/8W	10%	172043300
R68	CACP	100k	1/8W	10%	172051000
R69	CACP	4.7k	1/8W	10%	172034700
R70	CACP	10k	1/8W	10%	172041000
R71	CACP	33k	1/8W	10%	172043300
R72	CACP	33k	1/8W	10%	172043300
R73	CACP	100k	1/8W	10%	172051000
R74	CACP	4.7k	1/8W	10%	172034700
R75	CACP	10k	1/8W	10%	172041000
R76	CACP	33k	1/8W	10%	172043300
R77	CACP	100k	1/8W	10%	172051000
R78	CACP	4.7k	1/8W	10%	172034700

Cct Ref.	General Description				Solartron Part No.
R79	CACP	10k	1/8W	10%	172041000
R80	CACP	33k	1/8W	10%	172043300
R81	CACP	33k	1/8W	10%	172043300
R82	CACP	100k	1/8W	10%	172051000
R83	CACP	4.7k	1/8W	10%	172034700
R84	CACP	10k	1/8W	10%	172041000
R85	CACP	100k	1/8W	10%	172051000
R86	CACP	4.7k	1/8W	10%	172034700
R87	MEFM	33k	1/8W	0.5%	192743302
R88	MEFM	965k	1/4W	0.5%	160400530
R89	MEFM	470	1/4W	0.5%	198224701
R90	MEFM	3.6k	1/8W	0.5%	192733602
R91	CACP	4.7k	1/8W	10%	172034700
R92	CACP	4.7k	1/8W	10%	172034700
R93	MEFM	10k	1/8W	.25%	192841002
R94	MEFM	101	1/8W	.25%	192821012
R95	PRWW	9.75k	1/4W	0.1%	169606901
R96		15.5k	1/4W	0.1%	
R97	MEFM	1.27k	1/8W	1%	160400430
R98	MEFM	649	1/8W	1%	160400420
R99	MEFM	332	1/8W	1%	160400419
R100	MEFM	169	1/8W	1%	160400418
R101	MEFM	86.6	1/8W	1%	160400417
R102 & R103	PRWW	40k	1/4W	0.05%	169607001
R104	MEFM	10k	1/8W	.25%	192841002
R105	MEFM	101	1/8W	.25%	192821012
R106	CACP	1000	1/8W	10%	172031000
R107	CACP	1000	1/8W	10%	172031000
R108	CACP	8.2k	1/8W	10%	172038200
R109	CACP	8.2k	1/8W	10%	172038200
R110	CACP	47k	1/8W	10%	172044700
R111	CACP	47k	1/8W	10%	172044700
R112	MEOX	1000	1/4W	5%	195631000
R113	CACP	33k	1/8W	10%	172043300
R114	CACP	100k	1/8W	10%	172051000
R115	CACP	33k	1/8W	10%	172043300
R116	CACP	33k	1/8W	10%	172043300
R123	CACP	10k	1/8W	10%	172041000
C1	ESTM	.22	100V	10%	225452200
C2	ESTM	.047	100V	10%	225444700
C3	TANW	330	6V	20%	265283300
C4	CERM	3.3p	200V	15%	240603300
C5	ESTM	.22	100V	10%	225452200
C6	TANW	47	6V	20%	265274700
C7	CERM	150p	500V	20%	241321500
C8	CERM	15p	500V	20%	241311500
C9	ESTM	.47	63V	10%	225154700
C10	CERM	2.2p	200V	15%	240602200
C11	ESTM	.47	63V	10%	225154700
C12	ALME	220	16V	-20% +100%	273382200
C13	ALME	2200	10V	-10% +100%	273192200
C14	ALME	470	40V	-10% +100%	273784700
C15	ALME	470	40V	-10% +100%	273784700
C16	ALME	22	40V	-10% +100%	273772200
C17	TANW	15	20V	20%	265871500
C18	TANW	15	20V	20%	265871500
C19	ESTM	0.47	63V	10%	225154700
C20	CERM	33p	500V	20%	241313300
C21	PTFE	.1	100V	2%	208950001
C22	TANW	15	20V	20%	265871500
C23	ESTM	10	63V	20%	219971000
C24	CERM	470p	500V	20%	241324700
C25	CERM	150p	500V	20%	241321500
C26	CERM	150p	500V	20%	241321500
C27	CERM	15p	500V	20%	241311500
C28	TANW	15	20V	20%	265871500

Cct Ref.	General Description				Solartron Part No.
C29	TANW	15	20V	20%	265871500
C30	CERM	33p	500V	20%	241313300
C31	CERM	15p	500V	20%	241311500
C32	CERM	3.3p	200V	15%	240603300
C33	CERM	15p	500V	20%	241311500
C34 to C38	CERM	33p	500V	20%	241313300
C39	CERM	150p	500V	20%	241321500
C40	CERM	1000p	500V	20%	241331000
C41	CERM	470p	500V	20%	241324700
C42	CERM	.047	25V	+50% -25%	241944700
C43	CERM	470p	500V	20%	241324700
C44	CERM	.047	25V	+50% -25%	241944700
C45	TANW	4.7	35V	20%	266064700
C46 to C48	CERM	1000p	500V	20%	241331000
C49	TANW	4.7	35V	20%	266064700
C50	CERM	0.01	25V	-25% +50%	241941000
C51	CERM	0.01	25V	-25% +50%	241941000
C52	TANW	15	20V	20%	265871500
C56 and C57	CERM	0.047V	25V	+50% −25%	241944700
C58	CERM	330p	500V	±20%	241323300
D1	SD3				300522160
D2	SD3				300522160
D3	IN3595				300523590
D4	IN3595				300523590
D5	Zener	12V	.4W	5%	300521480
D6	Zener	12V	.4W	5%	300521480
D7	SD3				300522160
D8	SD3				300522160
D9	SD3				300522160
D10	Zener	3.9V	.4W	5%	300521420
D11	Zener	3.9V	.4W	5%	300521420
D12	W04				300524700
D13	Zener	6.8V	.4W	5%	300522540
D14	W04				300524700
D15	Zener	9.1V	.4W	3%	300525590
D16	Zener	9.1V	.4W	3%	300525590
D17	SD3				300522160
D18	OA47				300520850
D19 to D25	SD3				300522160
D26	Zener	12V	.4W	5%	300521480
D27 to D37	SD3				300522160
D38	IN829	6.2V	1/4W	5%	300525400
D39	Zener	5.1V	.4W	5%	300521310
D40	Zener	6.8V	.4W	5%	300522540
D41	HP5082				300524910
D42	Zener	9.1V	.4W	3%	300525590
D43	Zener	9.1V	.4W	3%	300525590
D44 to D49	SD3				300522160
RV1	CMPM	1M	1/3W	10%	130661000
RV2	CMPM	20k	1/3W	10%	130642000
RV3	CMPM	1000	1/3W	10%	130631000
RV4	CMPM	20k	1/3W	10%	130642000
RV5	CMPM	50k	1/3W	10%	130645000
RV6	CMPM	100	1/3W	10%	130621000
RV7	CMPM	100	1/3W	10%	130621000
RV8	CMPM	50	1/3W	10%	130615000
TR1	40673				300555210
TR2	40673				300555210
TR3	BC107				300553320
TR4	BC107				300553320

Cct Ref.	General Description	Solartron Part No.
TR5	BD166	300555150
TR6	BC107	300553320
TR7	BCY70	300553590
TR8	BD165	300555160
TR9	BD166	300555150
TR10	BC107	300553320
TR11	BCY70	300553590
TR12	MPS-A-13	300554560
TR13	BC107	300553320
TR14	BC107	300553320
TR15	3N163	300554530
TR16	2N4303	300553160
TR17 to TR22	U1899E	300554320
TR23	WD211	300555060
TR24	U1899E	300554320
TR25	3N163	300554530
TR26	BC107	300553320
TR27	BCY70	300553590
TR28	BC107	300553320
TR29	BCY70	300553590
TR30	BC107	300553320
TR31	BCY70	300553590
TR32	BC107	300553320
TR33	BCY70	300553590
TR34	2N2369	300552390
TR35	BCY70	300553590
TR36	BC107	300553320
TR37	BCY70	300553590
TR38	2N2369	300552390
TR39 to TR42	BC107	300553320
TR43	U1899E	300554320
IC1	LM301AH	510000620
IC2	LM301AH	510000620
IC3	LM310H	510090040
IC4	LM301AH	510000620
IC5	LM301AH	510000620
IC6	LM301AH	510000620
IC7	MOS Logic	519600306
IC8	LM308A	510090080
IC9	LM308A	510090080
IC10	SN74LS00N	510002000
IC11	SN74L74N	510001110
X1	Quartz Crystal	300810300
	Vertical PV Socket	352501690
	Horizontal Receptacle	352501700
SB	Push Button Switch	379601001
	40 Way D.I.L. I.C. Socket	300584880
	Disconnect Crimp	351501070
	Disconnect Pin	355900550

PCB No. 2

Cct Ref.	General Description				Solartron Part No.
*R1	MEFM	9.98M	2W	0.1%	169606702
*R2	MEFM	100.8k	2W	0.1%	
R3	MEFM	18k	1/8W	0.5%	192741802
R4	MEFM	180	1/8W	0.5%	192721802
R5	CACP	1000	1/8W	10%	172031000
R6	PRWW	9.975k	1/3W	0.1%	160300407
R7	CACP	10k	1/8W	10%	172041000
R8	CACP	100k	1W	10%	172551000
R9	CACP	1M	1W	10%	172561000
*R10	MEFM	100k	1/2W	0.1%	
*R11	MEFM	10k	1/2W	0.1%	169606802
*R12	MEFM	990k	2W	0.1%	
R13	MEOX	2.2k	1/4W	5%	195632200
R14	CACP	100k	1W	10%	172551000
*R15	MEFM	16k	1/4W	0.5%	169606101
*R16	MEFM	16.9k	1/4W	0.5%	169606101
R17	MEFM	180	1/8W	0.5%	192721802
R18	MEFM	15k	1/8W	0.5%	192741502
R19	CACP	100k	1/8W	10%	172051000
R20	CACP	100k	1/8W	10%	172051000
R21	MEFM	5.1k	1/16W	1%	192635102
R22	MEFM	5.1k	1/16W	1%	192635102
R23	MEOX	2.2k	1/4W	5%	195632200
R24	MEOX	10k	1/4W	5%	195641000
R25	MEOX	2.2k	1/4W	5%	195632200
R26	MEOX	10k	1/4W	5%	195641000
R27	MEOX	47Ω	1/4W	5%	195624700
R28	MEOX	220	1/4W	5%	195622200
R29	MEFM	27k	1/8W	0.5%	192742702
R30	CACP	1000	1/8W	10%	172031000
R31	MEFM	27k	1/8W	0.5%	192742702
R32	MEOX	18k	1/4W	5%	195641800
R33	MEOX	18k	1/4W	5%	195641800
R34	MEOX	2.2k	1/4W	5%	195632200
R73	PRWW	9.975k	0.33W	0.1%	160300407
R74	PRWW	999	1/4W	0.1%	160300412
R75	PRWW	1Ω	1.5W	0.01%	169608702
C1	ESTF	.22	400V	20%	226152200
C2	ESTM	22	63V	20%	219972200
C3	ESTM	3.3	63V	20%	219963300
C4	ESTM	3.3	63V	20%	219963300
C5	ESTM	2.2	63V	20%	219962200
C6	CERM	33p	500V	20%	241313300
C7	CERM	100p	500V	20%	241321000
C8	CERM	100p	500V	20%	241321000
C9	CERM	470p	1500V	20%	208450090
C10	ESTM	0.047	100V	10%	225444700
C11	CERM	0.047	25V	+50% -25%	241944700
C12	CERM	0.047	25V	+50% -25%	241944700
D3 to D6	HP 5082-6221				300525380
D7	Zener	3.9V	.4W	5%	300521420
D8	Zener	3.9V	.4W	5%	300521420
D9	Zener	3.9V	.4W	5%	300521330
D10	SD3				300522160
D11	SD3				300522160
RV1	CMPM	20k	1/3W	10%	130642000
RV2	CMPM	200	1/3W	10%	130622000
RV3	CMPM	200	1/3W	10%	130622000
RV4	CMPM	500	1/3W	10%	130625000
RV5	CMPM	50	1/3W	10%	130615000
RV6	CMPM	50	1/3W	10%	130615000
RV9	CMPM	50	1/3W	10%	130615000
TR1	BCY 70				300553590
TR2	BC 107				300553320
TR3	BC 107				300553320
IC1	LM 310H				510090040
IC2	LM 301AH				510000620

*Absolute Match

Cct Ref.	General Description	Solartron Part No.
SA	Switch 5 Wafer 2 Pole 5 way	379609205
RLB	Relay* 90	301201903
RLC	Relay* 90	301201903

* Two Pole Change Over

	Washer 8 BA Small	411000040
	Vertical PV Socket	352501690
FS2	Fuse 1A Slo-Blo	360103080

PCB No. 3

Cct Ref.	General Description				Solartron Part No.
R1 to R6	CACP	1000	1/8W	10%	172031000
R7 to R12	CACP	390	1/8W	10%	172023900
R13 to R19	CACP	82	1/8W	10%	172018200
R20	CACP	100	1/8W	10%	172021000
R21 to R28	CACP	10k	1/8W	10%	172041000
R29	CACP	22	1/8W	10%	172012200
D1 to D5	5082 - 4494				300750080
TR1 to TR6	2N2906A				300554500
TR7 to TR12	BC107				300553320
TR13 to TR19	2N2222A				300555410
TR20	BC107				300553320
IC1	LED MAN 73				300730340
IC2 to IC6	LED MAN 72				300730330
	14 PIN D.I.L. SOCKET				300584680
	POST				355500980
	TRANSISTOR PAD				300584220

MAIN ASSEMBLY

Cct Ref.	General Description	Solartron Part No.
T1	Mains Transformer	309606904
	Mains Lead	480140200
	Mains Lead Retainer	354003580
	Fuse Holder	360202000
	Fuse	360103040
	Rubber Boot	16000213
MSP1	Mains Selector Switch	375000500
	Input Terminal (Black)	355100360
	Input Terminal (Green)	355100370
	Input Terminal (Red)	355100380
	Guard Link	16200102

ACCESSORIES

Cct Ref.	General Description	Solartron Part No.
	Input Lead Assy (Red)	359900090
	Input Lead Assy (Black)	359900080
	Test Prod Black	351901030
	Test Prod Red	351901040
	Crocodile Clips (2)	355901030
	Polythene Bag	810000160
	Fuse 150mA	360103040
	Fuse 300mA	360103170

SECTION 6 Specifications

This section contains a copy of the technical specification applicable to this instrument.

This instrument is designed and manufactured to a higher specification than is claimed commercially. In order that that the user may benefit as appropriate, this technical manual may relate to a superior performance. In the event of contradictions between specifications, no additional claims are made for the instrument above that claimed in the current data sheet.

General

Display

Type:	7 Bar Red Light emitting diodes
Scale Length:	109,999 max.
Polarity Indication:	Displayed for negative dc inputs
Overload Indication:	DC/AC/μA/mA, flashing 1, Ω steady 1
Annunciator:	mV, V, μA/mA, Ω, kΩ
Ranging:	Automatic, redundant leading zeros are blanked.

Environment

Working Temperature Range	0 to +45°C
Storage Temperature Range	−30 to +70°C
Maximum Relative Humidity	70% at 40°C

Power Supply

Voltage:	115V/230V + 10% −15%		
Frequency:	50Hz ±1% or 60Hz ±1%		
Consumption:	12VA		
Fuses:	230V	150mA	Slo Blo
	115V	300mA	Slo Blo

Size

Width:	216mm	(8.5in)
Height:	89mm	(3.5in)
Depth:	280mm	(11in)
Weight:	2.73kg	(6 lb)

Technical Specification

◇Manufacturing calibration temp. 23°C.
Specification valid for calibration at 20 to 25°C.
Temperature corrections need be applied only when operating beyond the temperature limits quoted under Limits of Error.

DC voltage (V DC)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp coeff. per °C ± [% rdg. + % f.s.]		Input Resistance
1V	10μV	0.004	0.002	0.006	0.002	0.007	0.002	0.001	0.0002	> 1000MΩ
10V	100μV	0.004	0.002	0.006	0.002	0.007	0.002	0.001		> 1000MΩ
100V	1mV	0.005	0.002	0.01	0.003	0.01	0.003	0.002	0.0002	10.1MΩ
1kV	10mV	0.008	0.002	0.01	0.003	0.012	0.003	0.002		10.1MΩ

Full Scale = Nominal Range + 10% (except 1kV range where f.s. = Nominal Range)

Overload Immunity 1000V dc

AC voltage (V AC)

Nominal Range	Input Sensitivity	Limits of Error◇ 40Hz to 20kHz□ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Input Impedance
1V	10μV	0.1	0.01	0.1	0.015	0.1	0.015	0.005	0.0004	1MΩ/100pF
10V	100μV	0.2	0.01	0.2	0.015	0.2	0.015	0.015	0.0004	1MΩ/100pF
100V	1mV	0.15	0.01	0.2	0.015	0.2	0.015	0.015	0.0004	1MΩ/100pF
750V*	10mV	0.15	0.01	0.2	0.015	0.2	0.015	0.015	0.0005	1MΩ/100pF

*500V max. above 1kHz

Overload Immunity 1100V pk

Full Scale = Nominal Range + 10% (except 750V where f.s. = Nominal Range)

□**Typical limits for other frequency bands:**
10Hz to 40Hz: ± 1.0% rdg. ± 0.1% f.s.
20kHz to 50kHz: ± 1.0% rdg. ± 0.1% f.s.
50kHz to 100kHz: ± 4.0% rdg. ± 0.3% f.s.

Resistance (Ω)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Current Thro' R
10kΩ	100mΩ	0.008	0.004	0.015	0.005	0.02	0.005	0.005	0.0002	100μA
100kΩ	1Ω	0.006	0.003	0.015	0.004	0.02	0.004	0.005		100μA
1MΩ	10Ω	0.015	0.004	0.025	0.005	0.03	0.005	0.005	0.0002	1μA
10MΩ	100Ω	0.03	0.005	0.05	0.005	0.05	0.005	0.005		1μA

Maximum dissipation in unknown: 1mW Full Scale = Nominal Range + 10% Overload Immunity 200V pk

DC current (μA/mA DC)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Input Resistance
100μA	1nA	0.03	0.005	0.04	0.005	0.04	0.005	0.005	0.0002	< 5Ω
1mA	10nA	0.03	0.005	0.04	0.005	0.04	0.005	0.005		< 5Ω
100mA	1μA	0.05	0.04	0.05	0.05	0.05	0.05	0.005	0.002	< 2Ω
1A	10μA	0.05	0.005	0.05	0.005	0.05	0.005	0.005		< 2Ω

Full Scale = Nominal Range + 10%

7054 only: external current shunt for 100mA & 1A ranges

Overload Immunity Ranges 1 & 2 10mA
Ranges 3 & 4 1.1A

Common Mode Rejection

Measured with an imbalance of 1kΩ in the input leads
Maximum Common Mode Voltage: 500V dc or peak ac

DC Measurement:	Rejection of dc > 120dB
	Rejection of 50/60Hz ± 1% > 120dB
AC Measurement:	Rejection of dc > 120dB
	Rejection of 50/60Hz ± 1% > 40dB

Series Mode Rejection

Ratio of peak interference to 1 digit reading error, produced

DC Measurements:	Rejection of 50/60Hz ± 1% > 60dB

APPENDIX

This section contains specialised selection procedures and/or test equipment to facilitate servicing.

CONTENTS

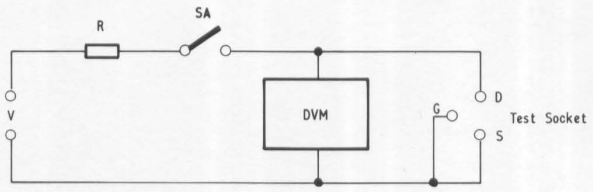
FET SELECTION PROCEDURE

PURPOSE

To select four FET's type U1899E with Ron matched to within 1Ω at a drain-source current of 100μA.

TEST PROCEDURE

The following test procedure should be carried out using the test circuit shown below or Solartron Test Equipment TG1100/1.



TEST CIRCUIT

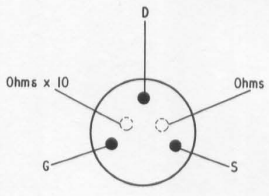
$$\left.\begin{array}{l} V = 10V \\ R = 100k \end{array}\right\} \quad \frac{V}{R} = 100\mu A \pm 0.2\%$$

(a) Devices to be tested should be allowed to settle to the ambient temperature of the chamber in which the matching operation is to be done.
This temperature should be $23^{o}C \pm 1^{o}C$.

(b) Place the device under test in the test socket using tweezers or pliers to ensure that its temperature is not raised by handling.

(c) Press switch SA and note DVM reading.
Use the relation 1mV = 10Ω to calculate the Ron value.

(d) Mark the top of the device with two coloured dots of paint as shown in following view employing the standard colour code.
Ron to be given to nearest whole number, e.g.



TOP VIEW

45.6Ω	YELLOW-BLUE
46.3Ω	YELLOW-BLUE
46.5Ω	YELLOW-VIOLET

(e) Select sets of four devices, each with the same colour code.

COLOUR CODE

0	Black
1	Brown
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Grey
9	White

SETTING-UP CASE 70502

INTRODUCTION

In order to achieve the greatest accuracy during a calibration it is essential that the operating temperatures affecting circuit components are as near as possible to those experienced within the instrument case during normal operation.

The Setting-Up Case 70502 enhances the calibration accuracy by allowing access for adjustments whilst the instrument is functioning under normal working conditions.

GENERAL DESCRIPTION

The Setting-Up Case is basically a normal instrument case with holes drilled in convenient positions allowing access to the potentiometers. Fig. A1 shows the side view of the Case with the access holes and the relevant potentiometers.

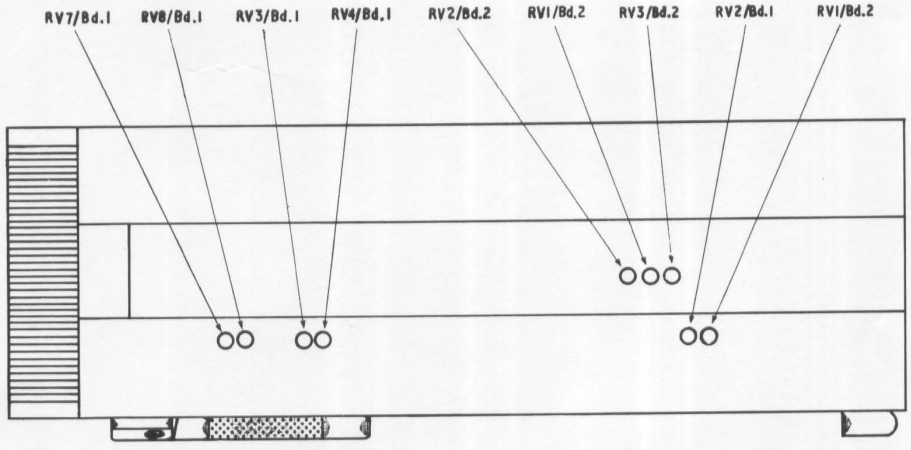


Fig. A.1. View of Setting-Up Case showing potentiometer access holes.

PART 2 DIGITAL MULTIMETER 7140

DIGITAL MULTIMETER 7140

Part No. 71400030

Issue 2 December 1977

Schlumberger

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TECHNICAL MANUAL

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CONTENTS

SECTION 1 General

INTRODUCTION

The 7140 Digital Multimeter (DMM) combines the advantages of a compact and versatile multimeter with the precision and convenience of a digital instrument. Automatic range selection and polarity decision give rapid readings. The complete absence of range switching enables the user to concentrate on the task in hand and apart from selecting the actual measurement mode required all other measurement decisions are undertaken automatically, so reducing the risk of damage to the user's equipment, as well as to the DMM.

The DMM covers the following measurement modes, all auto-ranging.

DC VOLTAGE

10μV - 1000V

AC VOLTAGE

10μV – 700V

RESISTANCE

100mΩ - 11MΩ

DC CURRENT

1nA - 1.1A

With a scale length of 109.99.

Model 7140 also incorporates an automatic over-range indication, automatic overload protection and automatic blanking of unused digits.

Model 7144 incorporates a digital output in parallel BCD form for use with printers and other output devices.

SECTION 2 Operation

This section provides all the necessary instructions concerning preliminary adjustments and operating procedures required to put the instrument into everyday use.

PRELIMINARY ADJUSTMENTS

Before using the instrument for the first time the following preliminary adjustments should be carried out:

(a) Check that the voltage selection switch on the rear panel is in the correct position.

(b) Check that the correct fuse is fitted as follows:-

230V	150mA	Slo-Blo	1¼" x ¼"
115V	300mA	Slo-Blo	1¼" x ¼"

(c) Connect a suitable connector to the input mains lead as follows:-

Brown	-	Line (Live)
Blue	-	Neutral
Yellow/Green	-	Earth

This earth connection is essential for stability of readings and user safety

(d) Plug into the mains supply and switch the instrument ON.

OPERATION

The operation of this instrument under most conditions will be found to be self-evident. The only operator decision required is the selection of the measurement mode required.

During operation, the following factors should be borne in mind:-

1. Since the instrument will automatically change ranges to suit the applied input potential, care should be taken to note the decimal point position in combination with the unit indicators.

2. In the event of an unintentional voltage or current overload, the offending potential should be removed as soon as possible since continuous overload may eventually cause damage to the instrument.

3. Due to the high input impedance of the input amplifier, the display readings will be random when the instrument is left with its input terminals as follows:-

   (a) Open circuited on 'V.DC' and 'V.AC' modes.

   (b) Short circuited on 'μA' and 'mA' modes.

   Random readings can cause the range relay to switch on and off which can be prevented by short circuiting the input terminals in the case of (a) and open circuiting them in the case of (b).

4. In the 'Ω' mode, open circuited input terminals produce an overload condition i.e. a steady '1' being displayed. Short circuited input terminals produce a nominal zero condition.

5. When measuring voltages on the lowest range and resistance on the highest range of the DMM, pick-up on the input leads may become a problem. If this occurs it is recommended that the leads be kept as short as possible and/or screened.

SECTION 3 Servicing

This section provides detailed servicing information for the instrument. Setting-up procedures and calibration are covered in Section 4.

INTRODUCTION

This Servicing Section is based on the functional block system of circuit diagrams, whereby components are grouped together to form a functional entity. A large scale block diagram is used to describe the overall operation of the Digital Multimeter (DMM). This diagram is then sub-divided to produce blocked circuit diagrams.

Information regarding circuit descriptions, component locations, printed circuit board layouts and any specific cautionary notes concerning components or testing procedures are arranged to be fully visible with the appropriate circuit diagram. Full calibration and setting up procedures are located in Section 4.

PRESENTATION OF INFORMATION

A brief glance through this section will reveal that the section is sub-divided into three major sub-sections, each of which deals with a major function in the DMM. Located within each section are block type circuit diagrams, always folding out clear to the right, with a functional description of each on the left hand text page. The pcb layout diagrams are arranged to fold out clear to the left, allowing cross reference between diagram and component location.

Referring to any of these diagrams, it can be seen that the major functional signal pathways are shown as bold lines, whilst those of a minor or control function are shown with thinner lines. The arrows indicate the direction of functional flow, which in the majority of cases will be from left to right of the diagram. Most feedback paths however, will flow from right to left.

These rules, although generally followed, are not rigidly adhered to where observance may cause ambiguity or is extravagant of space.

COMPONENT LOCATION

Diagrams of the printed circuit boards associated with each circuit diagram and photographs illustrating the method of access are reproduced in a manner enabling them to be examined in conjunction with the diagrams. By this method the physical position of any component can be quickly established.

COMPONENT NUMBERING

Each printed circuit has its own component numbering. This means that on a circuit diagram more than one component may be shown with the same component number. When this occurs care must be taken to ensure that the correct part is identified if it is required to replace the component. For instance, in the 7140 there are several pcb's, all of which include a component numbered R1.

The correct item must be identified from the parts list by reference to the pcb or assembly on which it is mounted.

POWER RAIL NOTATION

The power rails are shown as short detached bars with the nominal voltage annotated. On any one pcb, all bars annotated with the same voltage are electrically connected together and correspond to the appropriate rail notation shown on the power supplies circuit diagram, referenced 10.

The 0V rail in some cases is associated with the signal paths, annotated SIGNAL 0V and followed by a reference number 1 to 5 inclusive, thereby identifying the decoupling components used for that particular group of components. All identically referenced zero volt lines are electrically connected together at the 0V STAR POINT on pcb 1 (C18 –ve).

It must be remembered that the voltages shown are approximate, being proportional to the load taken through the appropriate decoupling resistors. A voltage reading which is inconsistant with the value given on the diagram should not, therefore, be taken as a symptom of unserviceability without reference to other indications.

ELECTRICAL CONNECTIONS

Electrical connections used are mainly of the Berg pin and socket type. Two plugs and sockets are employed using Berg pin/socket combinations. These are clearly identified, with all the remaining Berg pin/socket connections bearing only a number.

Transformer connections used are of the disconnect pin type.

SPLIT PADS

The split pads provide a means of adjusting circuit resistance and also for isolating various parts of the circuit during fault diagnosis.

They are short circuited by running solder across the gap and open circuited by removing the solder. Care should be taken not to apply excessive heat during these operations.

FUNCTIONAL DESCRIPTION

The Model 7140 Digital Multimeter (DMM) may be looked upon as an instrument which divides down into three major functional areas. These are shown as coloured areas in the adjacent KEY DIAGRAM.

This diagram should be looked upon as a pictorial index as within each of these coloured areas are further blocks, each referenced with a number which refers to a specific block/circuit diagram within each section of this manual.

It is important when using these diagrams that the information should be looked at from a functional view-point before dealing with any actual detailed servicing. That is to say, deduce what could be the problem before actually looking at specific circuit details.

With reference to the KEY DIAGRAM, the input signal is applied to an ANALOGUE signal processing section. The primary function of this block is to scale the input signal into a form suitable for use by the DIGITAL (A/D Converter) section.

The input signal in all cases is converted into a dc signal. Since the A/D Converter can only handle signals within the range 0-11V directly, the analogue section provides a 100/1 attenuation on the higher ranges.

The scaled analogue input is then converted into a digital form by means of the triple ramp technique of integration (for a detailed explanation, refer to Section 3B), the result of which is displayed on a light emitting diode (LED) display.

The third major functional block provides the power supplies to operate the whole instrument. This block also provides timing pulses to relate the measurement to the incoming mains supply frequency in order to overcome ac interference.

GENERAL NOTE:-

The numbers in each of the blocks shown below refer to the appropriate block and circuit diagrams contained in this section.

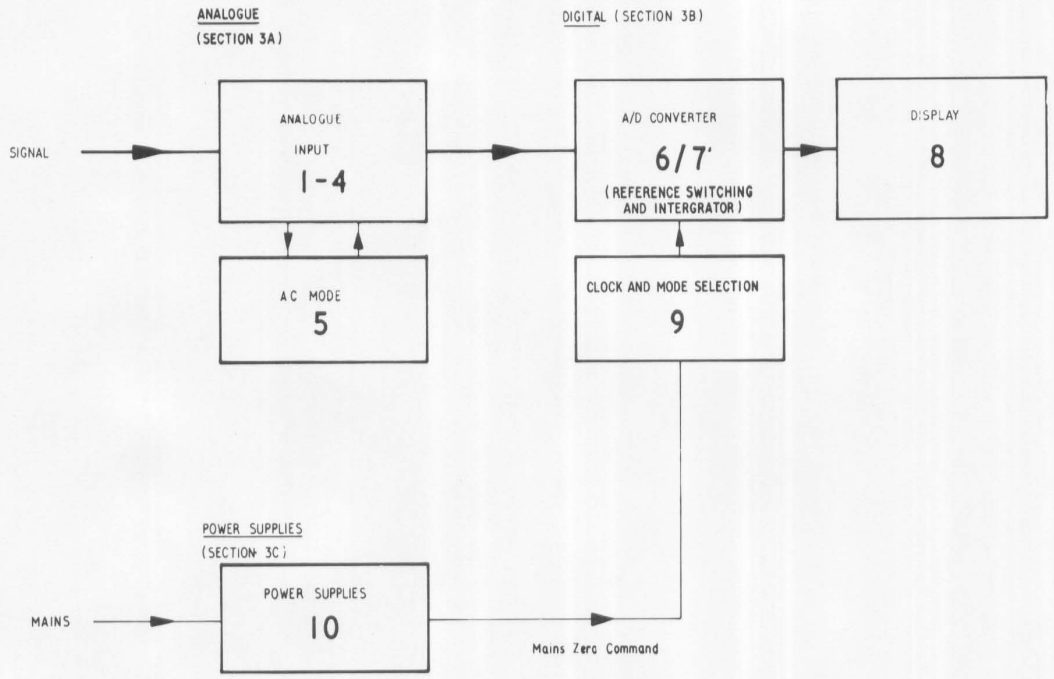


Fig. 3.1. Key Diagram (Pictorial Index).

SUB SECTION 3a Analogue

This sub-section deals with the ANALOGUE section of the instrument whose primary function is to convert the input signal into an acceptable form suitable for digital conversion by the DIGITAL section (SUB-SECTION 3B - DIGITAL).

SIGNAL CONVERSION

INTRODUCTION

The purpose of these sections of circuitry is to convert the incoming signal into dc suitable for conversion by the A/D Converter in the DIGITAL section of the instrument.

DC MEASUREMENT

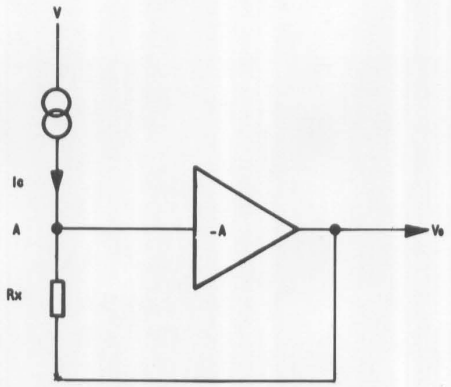
In this mode of operation, since the applied signal is already dc, the circuitry serves to scale the input to within the upper 11V limit acceptable to the A/D Converter input.

The INPUT AMPLIFIER is arranged in a series feedback configuration to provide a very high input impedance to the applied signal on the unattenuated ranges (0-11V).

The Analogue Input circuit in the 'V.DC' mode is shown on DIAGRAM 1.

RESISTANCE MEASUREMENT

The resistance measuring mode, 'Ω', is shown on DIAGRAM 2. Consider the following simplified diagram.



Point A is a 'virtual earth' input to a very high gain amplifier (INPUT AMPLIFIER). In order that the current flowing into and out of point A is balanced, the output of the amplifier Vo must rise to develope a potential drop across the applied unknown resistance Rx such that the constant current Ic derived from the reference voltage all flows through Rx. The final value of Vo when the circuit balances will be proportional to Rx and it is this output which is used by the A/D Converter for conversion to units of resistance.

CURRENT MEASUREMENT

Following from the above description of resistance measurement, it can be seen that if we make Rx a known value (RV6/R6 on DIAGRAM 3), the output of the amplifier Vo will be proportional to the unknown applied current.

AC MEASUREMENT

The section of circuitry used for converting the applied input to dc is shown separately on DIAGRAM 5.

The applied signal passes through a separate INPUT ATTENUATOR network and, via the AC AMPLIFIER buffer stage and SCALING RESISTORS, to the SUMMING JUNCTION. This point acts as a 'virtual earth' to the INPUT AMPLIFIER which follows. The output of this amplifier passes through the RECTIFIER SYSTEM which then divides the amplifier output into positive and negative half cycles by rectifier action. The positive half cycle output is filtered by the LOW PASS FILTER to form the equivalent dc input to the A/D Converter.

Since the rectified output would produce the mean value of the applied input, provision is made (RV3) to scale the signal input such that the final displayed reading is the rms (root mean square) as opposed to mean value of the applied signal. It should be remembered that this scaling action will only be valid when the input wave form is sinusoidal.

TEST WAVEFORMS

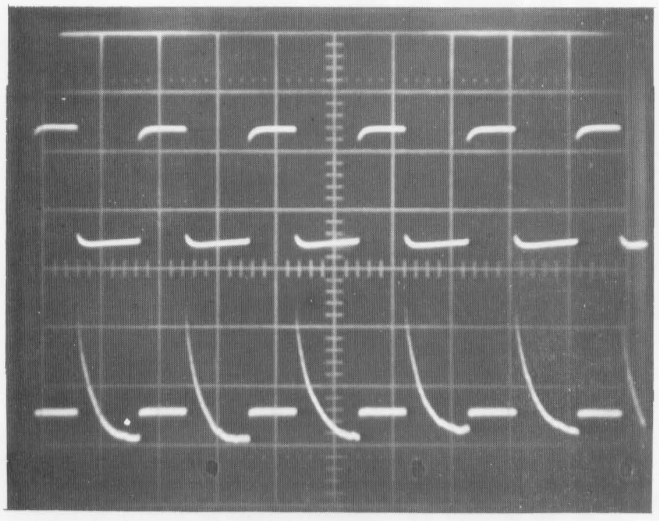
FRAME 3A - 1

UPPER TRACE

A typical output waveform produced by the CHOPPER DRIVE (DIAGRAM 4) at TR4 collector. The output at TR3 collector is an inverted form of this trace.

LOWER TRACE

A typical output waveform produced by the DEMODULATOR (DIAGRAM 4) at the junction of C5 and R11.



Time/cm:- 2ms.

Volts/cm:- 500mV.

Frame 3A-1 Chopper/Demodulator waveforms.

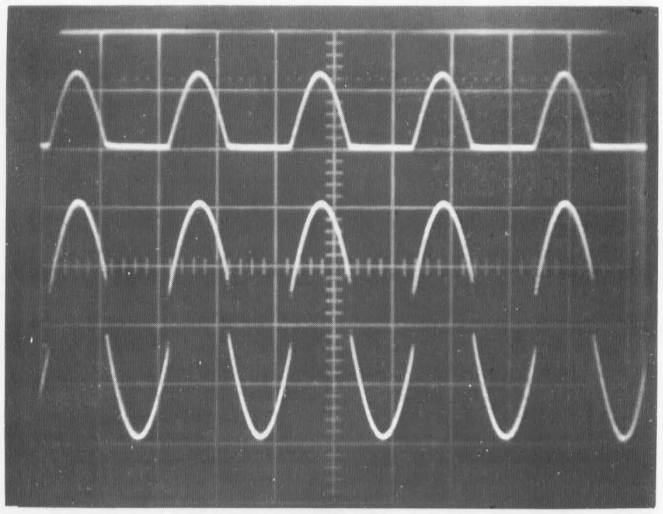
FRAME 3A - 2

UPPER TRACE

A typical output waveform produced at diode D3 cathode, the output from block RECTIFIER SYSTEM (DIAGRAM 5) used to provide dc to the A/D Converter for operation on ac V mode.

LOWER TRACE

A typical output waveform provided by the complementary common base stage formed by TR1/2 in block RECTIFIER SYSTEM (DIAGRAM 5) and used to drive both halves of the diode feedback loop. The sharp transitions about the zero of the output waveform overcome possible non-linear rectification, due to diode characteristics up to about 0.7V.



Time/cm:- 1ms.

Volts/cm:- 1V.

Frame 3A-2 Rectifier System waveforms.

DC MODE

In this mode of operation the correct attenuation is applied by the Auto Ranging function of the instrument.

DC ATTENUATOR/RESISTOR

The attenuation available on 'V.DC' is decided by relay RLB as follows:-

RLB energised:- 100/1 attenuation

RLB de-energised:- no attenuation

INPUT AMPLIFIER

This acts as a buffer between the voltmeter input and the Integrator (DIAGRAM 7).

OHMS MODE

In this mode of operation, the −10.000V output from the Inverter (REFERENCE SWITCHING, DIAGRAM 6) is used to provide a constant potential which, in conjunction with the DC Attenuator/ Resistor, produces the appropriate test current (100μA or 1μA). The test current whilst flowing through the unknown resistance, produces a potential drop which is proportional to the value of unknown resistance. Refer to diagram 6 for further details of the −10.000V voltage source.

DC ATTENUATOR/RESISTOR

This resistance network is normally used as the DC Attenuator. When the 'Ω' mode is selected the network, in conjunction with relay RLB, decides the value of test current as follows:-

RLB energised:- 1μA nominal

RLB de-energised:- 100μA nominal

INPUT AMPLIFIER

This is used in operational amplifier configuration with the unknown resistor as the feedback resistor.

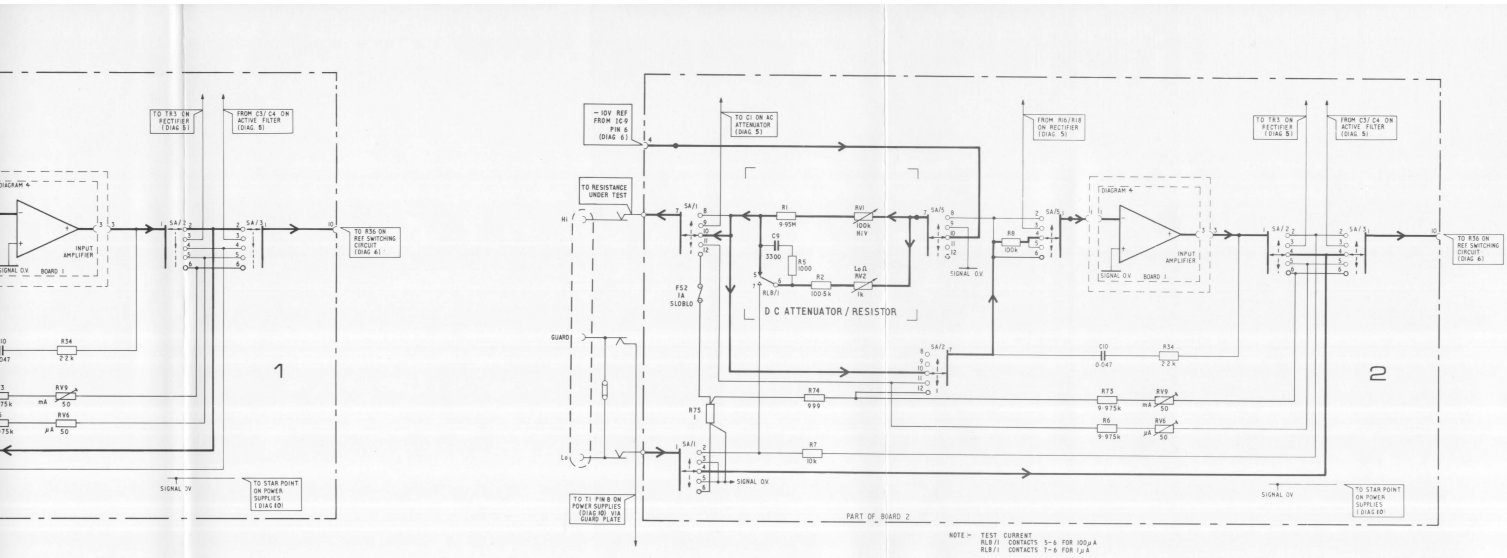
CURRENT MODE

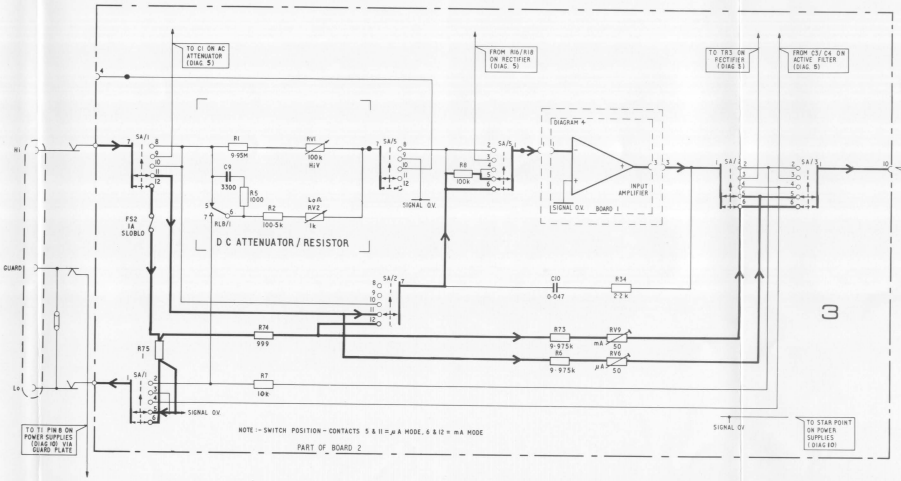
In this mode of operation the unknown current flows through one of two resistances R6, R73 (depending on whether μA or mA is selected,) producing a potential drop across it which is proportional to the unknown current.

INPUT AMPLIFIER

This is used in operational amplifier configuration. In the μA mode current is fed to the virtual earth. In the mA mode the amplifier is voltage fed, the voltage being that developed across R75. The amplifier gain is increased to x10.

Fuse FS2 protects the mA circuit against excess current



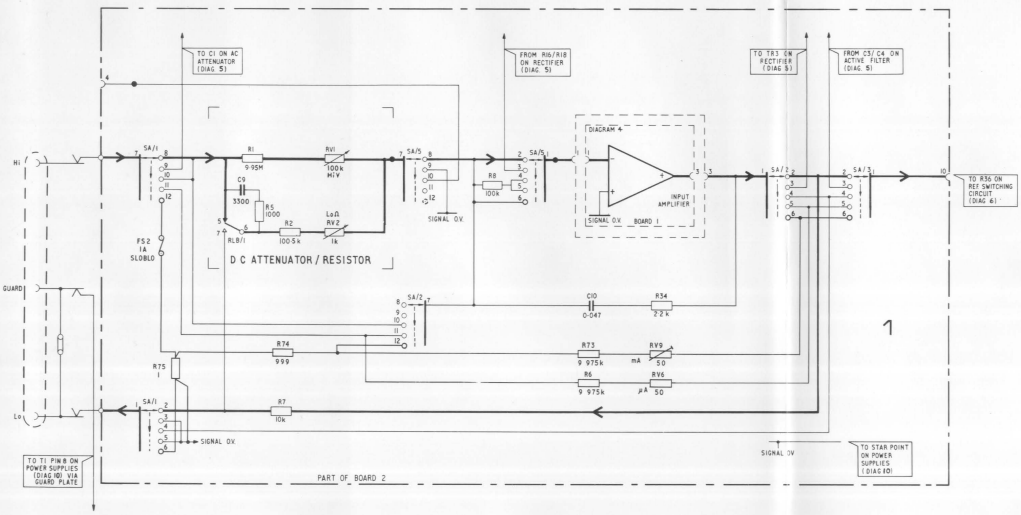


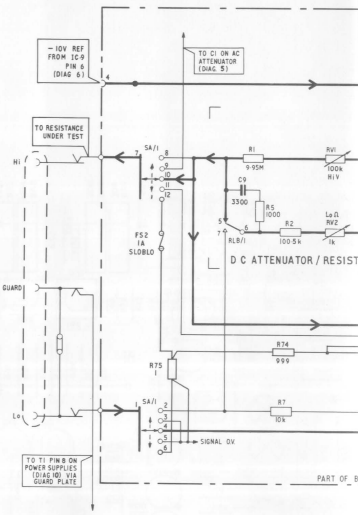
1 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN DC MODE)*

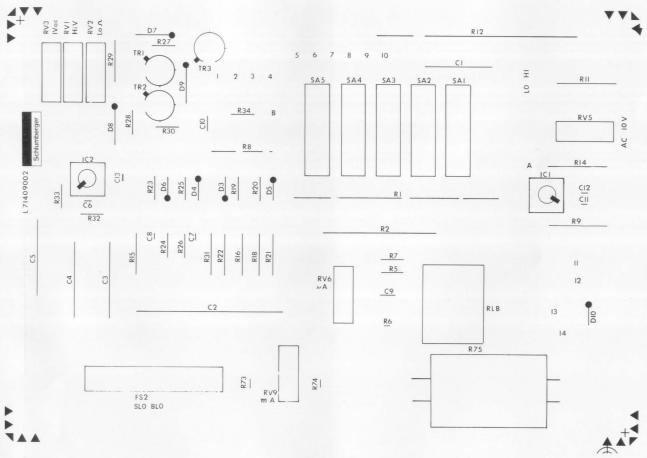
2 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN OHMS MODE)*

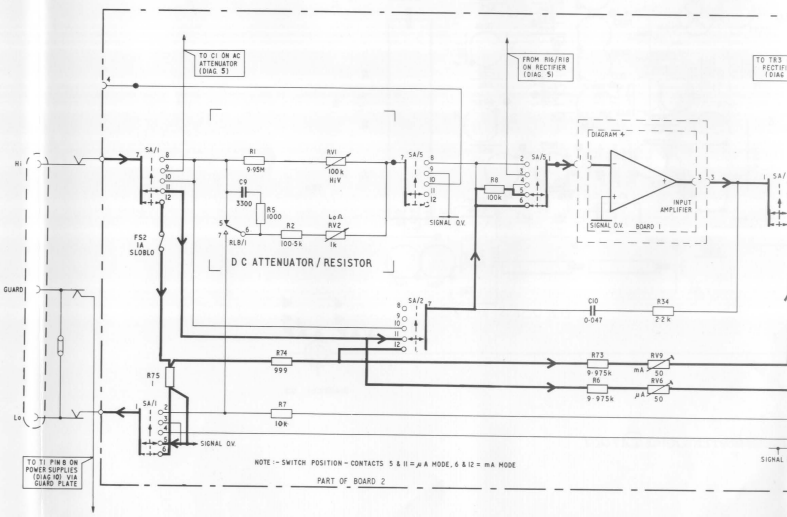
2a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*

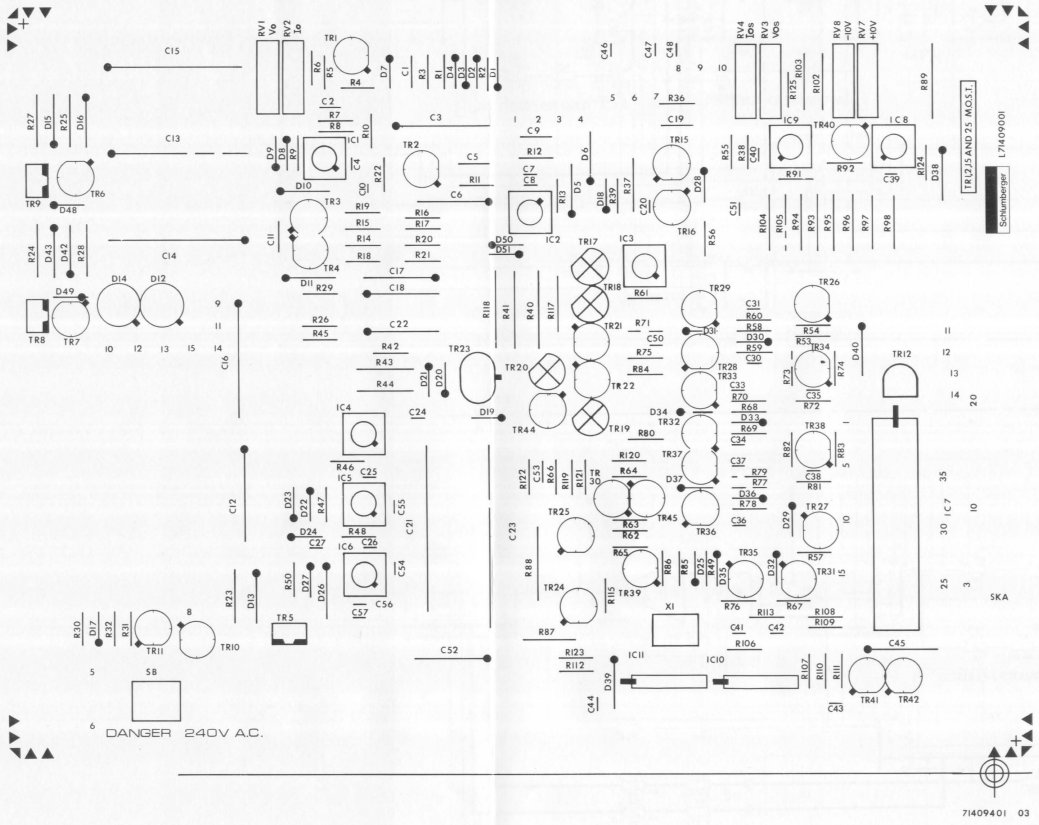
3 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN CURRENT MODE)*


TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG. 5)
TO TR3 ON RECTIFIER (DIAG 5)
FROM C5/C4 ON ACTIVE FILTER (DIAG. 5)
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V.
BOARD 1
TO R36 ON REF SWITCHING CIRCUIT (DIAG 6)
Hi
Lo
GUARD
FS2 1A SLOBLO
D C ATTENUATOR / RESISTOR
R1 9·95M
RV1 100k HiV
C9 3300
R5 1000
R2 100·5k
RV2 1k
R8 100k
C10 0·047
R34 2·2k
R74 999
R75
R73 9·975k
RV9 mA 50
R6 9·975k
RV6 µA 50
R7 10k
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
TO STAR POINT ON POWER SUPPLIES (DIAG 10)
PART OF BOARD 2
1


– 10V REF FROM IC9 PIN 6 (DIAG 6)
TO C1 ON AC ATTENUATOR (DIAG. 5)
TO RESISTANCE UNDER TEST
Hi
Lo
GUARD
FS2 1A SLOBLO
D C ATTENUATOR / RESIST
R1 9·95M
RV1 100k HiV
C9 3300
R5 1000
R2 100·5k
RV2 1k
R74 999
R75
R7 10k
SIGNAL O.V.
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
PART OF B


RV3 Hi Ω
RV1 Hi V
RV2 Lo Ω
D7
R27
TR1
TR3
TR2
R29
D9
R28
R30
C10
R34
B
R8
Schlumberger
IC2
C13
C6
R32
R33
D8
R23
D6
R25
D4
D3
R19
R20
D5
L 7140/002
SA5
SA4
SA3
SA2
SA1
R12
C1
LO HI
R11
RV5
AC 10 V
A
R14
IC1
C12
C11
R9
R1
R2
R7
R5
C9
R6
RV6 µA
RLB
D10
R75
C8
R24
R26
C7
R31
R22
R16
R18
R21
C5
C4
C3
C2
R15
FS2 SLO BLO
R73
RV9 mA
R74
2a


TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG 5)
TO TR3 RECTIFI (DIAG
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V.
BOARD 1
Hi
Lo
GUARD
FS2 1A SLOBLO
D C ATTENUATOR / RESISTOR
R1 9·95M
RV1 100k HiV
C9 3300
R5 1000
R2 100·5k
RV2 1k
R8 100k
C10 0·047
R34 2·2k
R74 999
R75
R73 9·975k
RV9 mA 50
R6 9·975k
RV6 µA 50
R7 10k
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
NOTE :– SWITCH POSITION – CONTACTS 5 & 11 = µA MODE, 6 & 12 = mA MODE
PART OF BOARD 2
SIGNAL



3a *PCB 1 COMPONENT AND COPPER TRACK LAYOUT*

INPUT AMPLIFIER

PROTECTION NETWORK

D1 and D2 protect the CHOPPER AMPLIFIER during overload conditions. D3/D4 in conjunction with D5/D6 limits the OUTPUT AMPLIFIER output to within ± 12V.

LOW-PASS FILTER

R3, R4 and C1 form a low-pass filter which removes the high frequency components (> 100Hz) from the dc channel and prevents spikes from the CHOPPER (Modulator) circuitry reaching the input terminals.

CHOPPER DRIVE

A 275Hz emitter-coupled Multivibrator TR3/4 for driving the CHOPPER and DEMODULATOR.

A small proportion of the anti-phase output is applied via RV2 to minimise chopper-spikes produced by TR1 in the CHOPPER (Modulator) circuitry.

(Refer to Section 4 - Setting Up Procedure for details on the adjustment of RV2).

CHOPPER (MODULATOR)

The filtered output from the LOW PASS FILTER is 'chopped up' by alternately shorting the signal to earth via TR1 to form an ac type signal. The chopping frequency is determined by the in-phase output of the CHOPPER DRIVE multivibrator.

Anti-phase chopper drive is applied to G2 of TR1 to minimise chopper spikes.

RV1 (Vo) provides a small dc voltage to the Chopper output, compensating for small offsets.

CHOPPER AMPLIFIER

IC1, whose gain and frequency response are defined by C3, C4, R8 and R9, amplifies the input (chopped) waveform produced by the CHOPPER (Modulator). The ac gain is 10,000 and the dc gain is unity.

DEMODULATOR

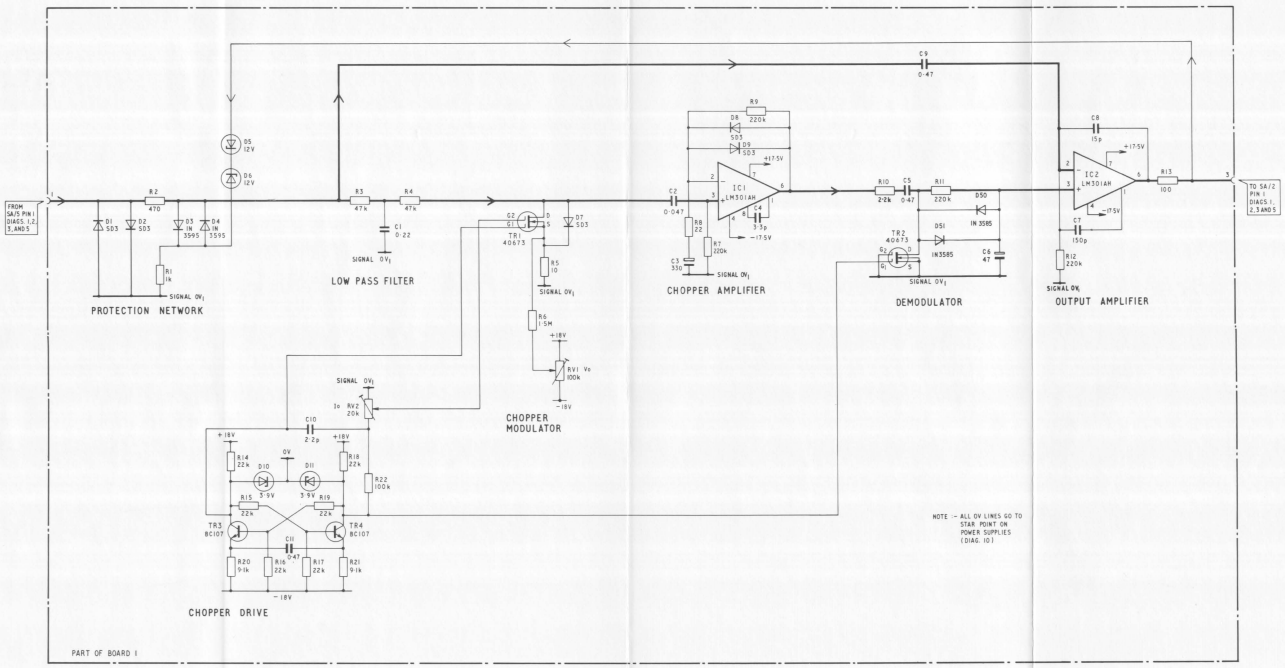
The output from the CHOPPER AMPLIFIER is fed via C5 to TR2 where it is dc restored. The ac component is removed by filter R11 and C6, leaving the dc component only.

OUTPUT AMPLIFIER

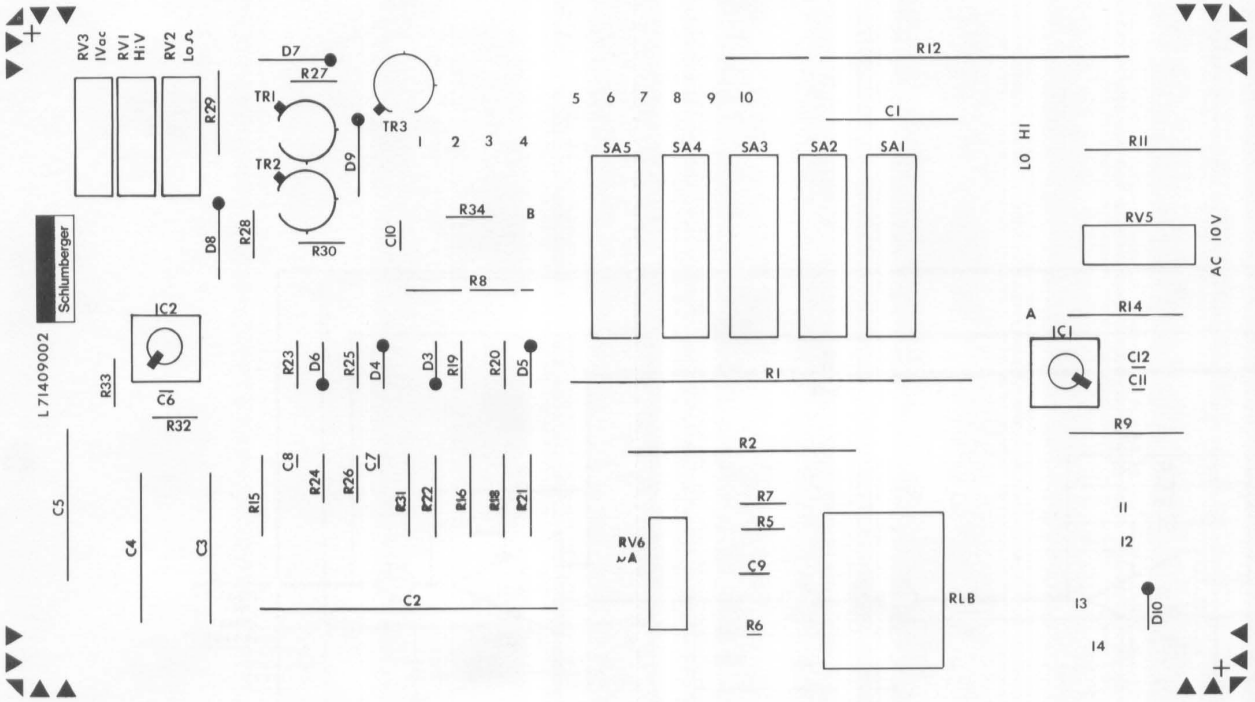
The ac component (> 2Hz) of the input voltage is coupled directly via R12/C9 to the inverting input of the amplifier while the dc component on C6 (DEMODULATOR) is added into the non-inverting input.

The output is applied to the PROTECTION NETWORK which limits the over-all amplifier output to within ± 12V.

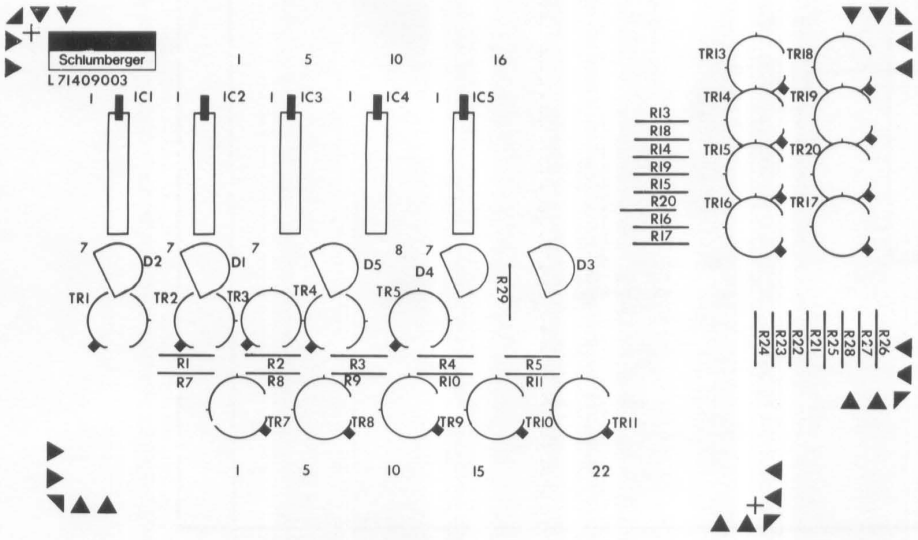
◄DIAGRAM 3a PCB 1 COMPONENT AND COPPER TRACK LAYOUT



4 INPUT AMPLIFIER CIRCUIT DIAGRAM



4a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*



4b *PCB 3 COMPONENT AND COPPER TRACK LAYOUT*

AC MODE

INPUT ATTENUATOR

On the 10V, 100V and 750V ranges, relay RLB is energised to attenuate the input signal by a factor of 100. The input impedance is 1MΩ whether the attenuator is energised or not.

AC AMPLIFIER

This is a voltage follower stage, isolating the input from the SCALING RESISTORS. R14 in conjunction with IC1 provides overload protection.

SCALING RESISTORS

The applied input plus the feedback signals via R16/R18 in the RECTIFIER SYSTEM are summed at the 'virtual earth' of the INPUT AMPLIFIER. RV3 scales the input signal so that the final displayed value on the LED module represents the rms (root-mean-square) value of the applied input assuming a pure sine-wave shape.

RECTIFIER SYSTEM

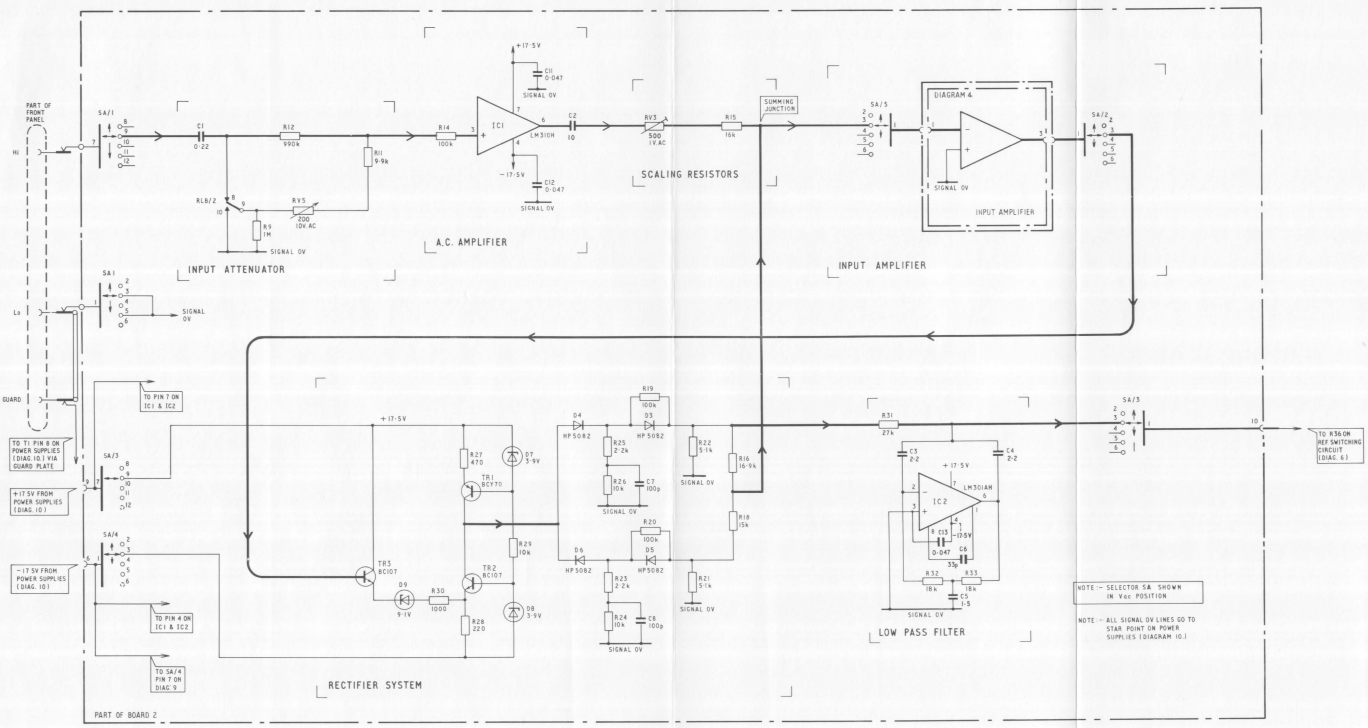
The output of the INPUT AMPLIFIER (DIAGRAM 4) drives the complementary common base stage formed by TR1/2. Positive half-cycles are fed back to the 'virtual earth' via D4/D3 and precision resistor R16. Negative half-cycles are fed back via D6/D5 and R18. Only the positive half-cycles are taken for digital conversion.

R25/R26/C7 and R23/R24/C8 are shaping networks which improve frequency response at low signal levels.

LOW PASS FILTER

IC2 is connected as a low-pass active filter to remove high frequency components from the rectified ac signal. The filter has a nominal cut-off frequency of 4.5Hz and provides 60dB per decade attenuation.

◄ *DIAGRAMS 4a & 4b PCB 2 & 3 COMPONENT AND COPPER TRACK LAYOUTS*



5 *AC MODE CIRCUIT DIAGRAM*

SUB SECTION 3b Digital

This sub-section deals with the DIGITAL section of the instrument whose primary function is to convert the dc analogue input into digital form.

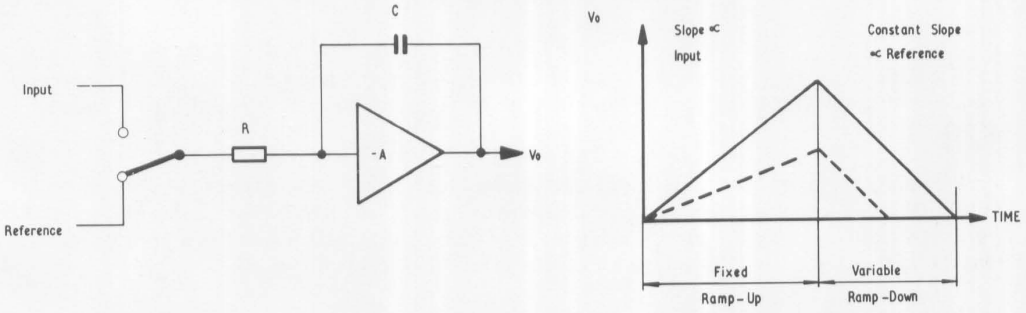
TRIPLE RAMP DIGITAL CONVERSION

INTRODUCTION

The triple ramp technique of analogue to digital conversion may be considered as a refined version of the well known dual ramp technique with the addition of a third ramp. This third ramp (known as fine ramp-down) acts like a 'vernier' upon the usual ramp-down period.

BASIC PRINCIPLES OF OPERATION

Examination of the following simplified cirucit diagram serves to illustrate the principles used to perform analogue to digital conversion in this instrument.



BASIC DUAL-RAMP SYSTEM

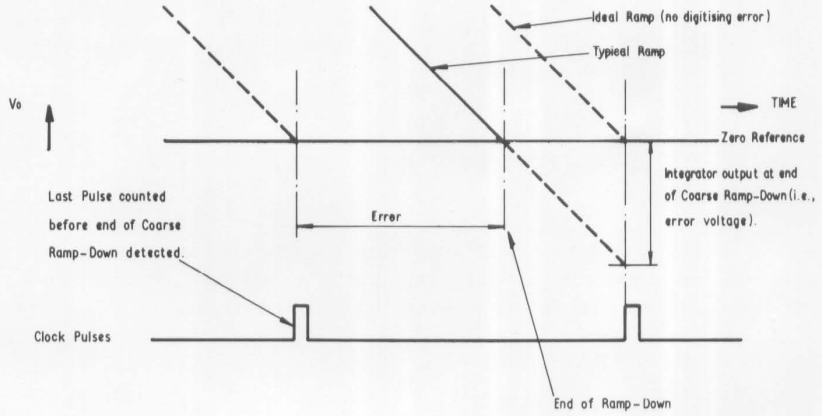
When the integrator is connected to the input its output 'ramps-up' at a rate which is proportional to the value of the input. After a fixed time the switch changes over and connects the reference in place of the input. It is so arranged that the reference voltage is of opposite polarity to that of the input, so that the integrator output now 'ramps-down' at a defined rate which is determined by the value of the reference.

If the ramp-up period is made constant by using a clock pulse generator to gate the input switch, the number of pulses produced during the 'ramp-down' period, the length of which is controlled by the slope of the reference voltage, will be directly proportional to the applied input.

Since both ramp-up and ramp-down periods are related to a common timebase, any variations of clock frequency do not affect the reading.

In the DMM, the reference voltage used during this 'ramp-down' period (known as 'coarse ramp-down') is actually 10V, so each ramp-down pulse with a 'full-house' counter length of 10,000 will represent 1mV. The total number of pulses collected between the end of ramp-up and the point where the integrator output was driven to zero is a direct measure of the applied input voltage to within 1mV.

Looking at a greatly magnified view of the integrator output waveform at the point where the integrator output passed through zero, it can be seen that there is an inherent digitising error within the system, the magnitude of which can be 1mV.



If we allow the integrator output to continue beyond zero until the next clock pulse, the integrator capacitor will be charged to a level representing the difference between 1mV and the true measured input.

By adding two extra less significant decades to the counter, the minimum decade would represent 10μV. If we complement* the counter and then re-organise it such that it counts down to zero when driven by further clock pulses, by changing the ramp-down rate, the final count overall could represent the applied input when the integrator output again passes through zero.

In the DMM, this second ramp-down reference voltage is 100mV so that each new clock pulse will represent 10μV. In order to drive the integrator output to zero, the new ramp-down reference polarity is made opposite to the coarse ramp-down polarity. This third ramp is known as 'fine ramp-down'.

It can be seen that the final measurement could, in theory, be within 10μV of the applied input.

* COMPLEMENTING

The action of complementing a number within a counter can be followed by referring to the following example.

We have a hypothetical counter capable of holding a total count of 100 pulses. If we count say 60 input pulses, still required to 'fill-up' the counter will be 100-60 i.e. 40. It is this number which is defined as the complement of the number 60 in this example.

MEASUREMENT CYCLE DRIVES

INTRODUCTION

All stages of analogue to digital conversion are controlled by IC7-board 1, whose outputs turn on or off appropriate FET switches to select the appropriate sections of circuitry required at each stage of a measurement cycle.

ELECTRICAL ARRANGEMENT

There are eight cycle control drive outputs as follows:-

IC7-pin 11	Drift Correct
pin 12	Earth Clamp
pin 13	Spoiler
pin 14	Neg. Fine Reference
pin 15	Pos. Fine Reference
pin 16	Pos. Coarse Reference
pin 17	Neg. Coarse Reference
pin 18	Input Switch

During a typical measurement cycle, each of these pins will assume the states shown in Table 3B-1. The Pause periods 1-4 are for internal use within the integrated circuit to allow time for internal re-organisation of the counter, range selection and other tidying up operations required. The duration of these periods will change depending upon the range, length of ramp-down, spoiler time etc. so differing pause periods should not be interpreted as indications of faulty operation.

TABLE 3B - 1 CONTROL CYCLE SEQUENCE

L = low $\leqslant$ - 16V H = high $\geqslant$ + 8V

IC7 - Board 1

Period	11	12	13	14	15	16	17	18
Drift Correct	L	L	H	H	H	H	H	L
Pause 1	H	L	H	H	H	H	H	L
Ramp-Up	H	H	H	H	H	H	H	L
Spoiler Period	H	H	L	H	H	H	H	L
Pause 2	H	L	H	H	H	H	H	L
Coarse Ramp	H	L	H	H	H	H*	L*	H
Pause 3	H	L	H	H	H	H	H	L
Fine Ramp	H	L	H	L*	H*	H	H	H
Pause 4	H	L	H	H	H	H	H	L

Levels marked* will be inverted when the applied signal input is negative (with respect to the - terminal on the front panel).

AUTO-RANGING

INTRODUCTION

The DMM is fully auto-ranging for all modes of operation. Range switching is divided into two parts, basic range selection and/or attenuator switching.

RANGE SELECTION

Each of the ranges is coded with a letter, the actual range depicted by each being dependent upon the measurement mode selected (refer Tables 3B - 2 to 4).

The basic ranges are coded A, B and C and progress in decade steps with A the highest. A, B or C followed by the letter R indicates the basic range together with the 100/1 attenuator stage, making a range selection with a full scale reading 100 times greater than that for the basic range alone.

TABLE 3B-2 VOLTAGE MEASUREMENT CODING

Nominal Range	Range of Current Displayed	Range Coding	
1000V	1099.9 to 100.0V	AR	AR
100V	109.99 to 10.00V	BR	BR
10V	10.999 to 1.000V	A	CR
1V	1.0999 to 1.0000V 999.9 to 100.0mV	B	B
100mV	109.99 to 0.00mV	C	C

TABLE 3B - 3 RESISTANCE MEASUREMENT CODING

Nominal Range Ω	Range of Resistance Displayed	Range Coding
10M	10999 to 1000k	AR
1M	1099.9 to 100.0k	BR
100k	109.99 to 10.00k	A
10k	10.999 to 1.000k	B
1k	1.0999 to 1.0000kΩ 999.9 to 0.0Ω	C

TABLE 3B - 4 CURRENT MEASUREMENT CODING

Nominal Range	Range of Current Displayed	Range Coding
1000μA	1099.9 to 100.0μA	A
μA mode 100μA	109.99 to 10.00μA	B
10μA	10.999 to 0.000μA	C
1000μA	1099.9 to 100.0mA	A
mA mode 100mA	109.99 to 10.00mA	B
10mA	10.999 to 0.000mA	C

Ranging up or ranging down occurs just after the fine ramp-down period in the measurement cycle, and unless a range change decision occurs, the range in use will remain constant for the remainder of the cycle.

RANGE-UP SEQUENCE

A range-up decision will occur if the total count at the end of fine ramp-down in the counter equals or exceeds 1.1 times that count which corresponds to the nominal full-scale count for the particular range in use. Take for example the 1V range, a range-up decision occurs if the measured voltage is 1.1 volts or higher, making 1.0999V the highest voltage which will not cause a range-up decision.

RANGE-DOWN SEQUENCE

A range-down decision will occur if the total count in the counter after a measurement falls below 0.1 times that which corresponds to nominal full-scale count except when the particular range in use is the lowest for the mode of operation. In this instance, operation will be maintained on that range for all readings down to zero. Therefore for all but the lowest of a group of ranges 0.1000 times the nominal full-scale value is the lowest reading which will not cause a range-down decision.

RANGE SWITCHING (DIAGRAM 7)

The input signal to the INTEGRATOR is rescaled by changing the value of the Integrator Input Resistor. The three ranges (A, B and C), effective resistances and scaling factors are as follows:-

RANGE	INTEGRATOR INPUT RESISTOR	SCALING FACTOR
A	1MΩ (R41)	1:1
B	100kΩ (R41//R40 ≃ 100kΩ)	1:10
C	10kΩ (R41//R118 ≃ 10kΩ)	1:100

By this method the dynamic range of the INTEGRATOR may be 0 – 11V, 0 – 1.1V or 0 – 0.11V respectively.

For inputs above 11V dc or 1.1V ac the attenuator relay, RLB, provides 100:1 attenuation on dc and ac ranging.

IC7 - PCB No. 1 (MOS - LS1) INTEGRATED CIRCUIT

This 40 - lead dual-in-line ceramic package contains the digital circuitry used to control the measurement cycle, count and gate clock pulses, provide signals to drive the LED display and to rescale the Integrator during auto-ranging.

Details of all pin connections and functions are on the Clock and Mode Selection diagram, referenced 9. Where inputs from, and outputs to IC7 occur on other circuits, these are identified by the effected IC7 terminal number shown enclosed in a square.

WARNING

Before attempting to remove this integrated circuit, ensure that all power supplies are switched off.

MOS Integrated Circuits are prone to damage by static charges. It is therefore advisable to ensure that all items likely to come into contact with MOS ICs and/or the circuits in which they are employed are bonded together and are earthed. Affected ICs are notified on their pcbs.

SELECTED FET'S TR17 - 20 (PCB No. 1)

Whenever any one of these components is replaced, it is essential that a component with the same colour coding is used or alternatively, replace the whole set.

NOTE. Reference should be made to the selection procedure detailed in the APPENDIX section of this manual.

DISPLAY

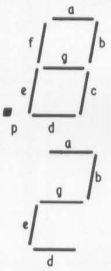
INTRODUCTION

The type of display used in this instrument is a light emitting diode (LED) 7-bar segment, time-shared type arranged to display 5 digits and a polarity sign.

7-bar SEGMENT FORMAT

Each of the possible digits, 0 to 9, is displayed using the universally accepted 7-bar segment format. In order to display a digit, a specific group of bars, each comprising a light emitting diode, is energised.

Each bar has been referenced with a letter a-g, and are arranged in the form of a figure 8 as shown below.

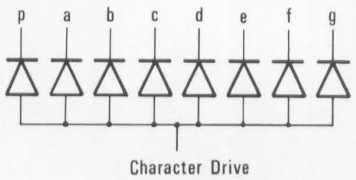


For example, suppose we wish to display the digit 2. In this case, bars a, b, d, e and g would be energised, all other bars being left de-energised.

The actual bars used to represent each digit are shown on DIAGRAM 8.

GENERAL ORGANISATION OF DISPLAY

The display used can display up to 5 characters, each of which comprises a 'diode tree' as shown below. The most significant digit can only display a one and/or a minus.



Each diode of a 'tree' corresponds to a specific bar as detailed above.

NOTE: The decimal point for each character is positioned to the left and will be energised whenever the 'p' bar is called for at the same time as the appropriate character.

In the DMM, each of the 5 possible characters is energised via the appropriate CHARACTER DRIVER (DIAGRAM 8) in sequence. In order that a particular digit may be displayed, the appropriate 7-BAR SEGMENT DRIVERS (DIAGRAM 8) are energised. For a group of diodes to light, both the segment and character drives must be present at the same time but since only one character drive will be present at any one time only one character will ever be on. It should be noted that the 1st character is incomplete, the surplus segments of which are arranged as the UNITS ANNUNCIATOR DISPLAY (DIAGRAM 8).

The polarity window will only display a negative sign, absence of display signifying a positive potential applied to the instrument. When 'V.AC' or 'Ω' is selected, no sign is displayed.

LOGIC ELEMENTS

NAND GATES (DIAGRAM 9)

Elements IC10a and b are logic elements performing a NAND function (positive logic) for which the following truth tables apply:

IC10a Pin No.	1	2	3
	H	H	L
	L	H	H
	H	L	H
	L	L	H
IC10b Pin No.	**4**	**5**	**6**
	H	H	L
	L	H	H
	H	L	H
	L	L	H

Logic Levels

H = -11V to - 14.5V

L = -16.5V to - 17.5V

D - TYPE BISTABLE (DIAGRAM 9)

Elements IC11 a and b are logic bistables (Flip-flops) performing a D-type function (positive logic) for which the following rules apply:

1. Whenever the CK (Clock) input goes high (positive logic), the Q output assumes the same state as that present on the D input.

2. Whenever the CK input is low, the D input level has no effect.

3. The $\overline{Q}$ output is always the complement of the Q output.

VOLTAGE LEVELS

Care should be taken when investigating this section of circuitry not to short any of the logic element connections to the 0V rails, since this action could apply a minimum level of -12V to the element and almost certainly damage it. It is recommended that the −18V rail should be used as a return path for test equipment and make appropriate adjustments to indicated readings.

TEST WAVEFORMS

FRAMES 3B-1/2

UPPER TRACE

This shows a typical input waveform at the INTEGRATOR (DIAGRAM 7) 'virtual earth' input.

LOWER TRACE

A typical ramp-up waveform produced at the input of the X100 AMPLIFIER (DIAGRAM 7) at C21/R46. The small insert shows a typical fine ramp-down. Note that the coarse ramp-down cycle is shorter than that shown in the main trace for illustration purposes only.

FRAMES 3B - 3/4

UPPER TRACES

These traces illustrate typical CHARACTER DRIVER (DIAGRAM 8) outputs. The outputs are taken from the collector of TR9 instead of the 'floating' collector of TR3, providing a well defined pulse.

LOWER TRACES

These traces illustrate typical 7-BAR SEGMENT DRIVER (DIAGRAM 8) outputs. The outputs are taken from the 'a' bar output, the collector of TR13, and are as follows.

Trace 3B-3 shows the 'a' bar segment, aligned underneath the 3rd character driver output, in a de-energised state. This depicts the missing 'a' bar of the figure 4 in this example.

Trace 3B-4 shows the 'a' bar segment in the energised state, in this example the top of the figure 3.

NOTES:-

1. The traces 3B-3/4 were taken with the BCD Output Module, and its inherent pull-up effect on the SEGMENT DRIVERS, fitted. Under this condition the trace of any bar not selected is pulled up. If tested without this pull-up effect, the position of the non-selected bar trace is indeterminate.

2. Due to the internal organisation of IC7, multiplexing of the Character and Segment Drivers produces a Six Character waveform, although only five characters are displayed on the DMM.

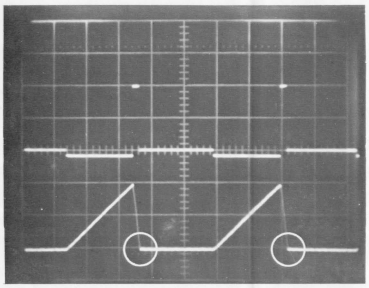
FRAME 3B-5

UPPER TRACE

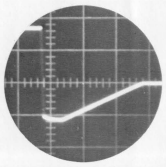
Typical output waveform at IC7-pin 19 of clock input phase ϕ 1 - refer CLOCK DRIVERS (DIAGRAM 9).

LOWER TRACE

This is the clock input at IC7-pin 20 in phase ϕ 2.



Frame 3B-1 Typical Integrator waveforms.

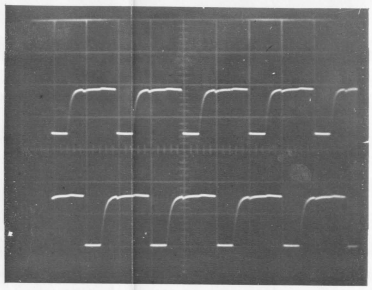


Time/cm:- 50ms.

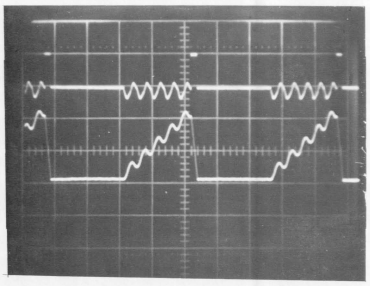
Volts/cm:- 5V.

Time/cm:- 5μs.

Volts/cm:- 20V.



Frame 3B-5 Typical Clock waveforms.



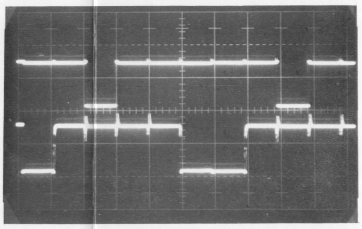
Time/cm:- 50ms.

Volts/cm:- 10V.

Frame 3B-2 Typical Integrator waveforms with ac interference.

Time/cm:- 200μs.

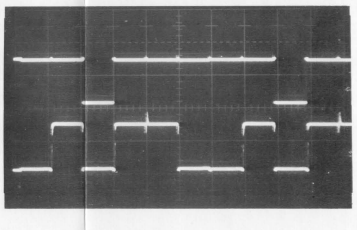
Volts/cm:- 5V.



Frame 3B-3 3rd Character with 'a' Segment de-energised (e.g. numeral 4).

Time/cm:- 200μs

Volts/cm:- 5V.



Frame 3B-4 3rd Character with 'a' Segment energised (e.g. numeral 3).

REFERENCE SWITCHING

REFERENCE VOLTAGE SOURCE

IC8 is connected as a non-inverting amplifier amplifying the voltage of reference zener D38 to give +10V, adjusted by means of R97 and R98 (Links LKA and LKB) and RV7 to give correct calibration. The output is +10.000V for use as a positive coarse reference. R93/R94 form a potential divider to provide +100mV for use as positive fine reference.

INVERTER

IC9 is connected as an inverter to produce - 10.000V from the REFERENCE VOLTAGE SOURCE. RV8 is adjusted to compensate for resistor tolerance and any dc offset. R104/R105 form a potential divider to provide - 100mV for use as negative fine reference.

EARTH CLAMP

During ramp-up, IC7-pin 12 goes high, thus via TR26 allowing TR15 to conduct to apply the unknown input signal to the A/D Converter. Similarly, TR16 is turned off thus unclamping the INPUT BUFFER AMPLIFIER from signal earth. At the end of ramp-up, IC7-pin 12 goes low, thus turning off TR15 and reclamping the INPUT BUFFER AMPLIFIER to earth via TR16.

INPUT BUFFER AMPLIFIER

A buffer stage providing input isolation to the INTEGRATOR (DIAGRAM 7). RV3 is provided for trimming out any internal voltage offset of IC3 while RV4 adjusts the input current compensation.

INPUT SWITCH DRIVER and INPUT SWITCH

During ramp-up, IC7-pin 18 goes low, applying the unknown input signal to the INTEGRATOR (DIAGRAM 7). TR17 is chosen such that the FET switches TR18 or TR19 in the COARSE REFERENCE SWITCHES and TR17 are of equal impedance to the INTEGRATOR (DIAGRAM 7) during both ramp-up and the appropriate coarse ramp-down period.

(Refer to the FET Selection Procedure in the APPENDIX of this manual for details of selection).

NEG. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a positive input signal during ramp-up, IC7-pin 17 goes low during the coarse ramp-down period. This turns on TR19 applying -10.000V as a negative reference input to discharge the level (proportional to the applied input signal) stored on the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

NEG. FINE REFERENCE SWITCH

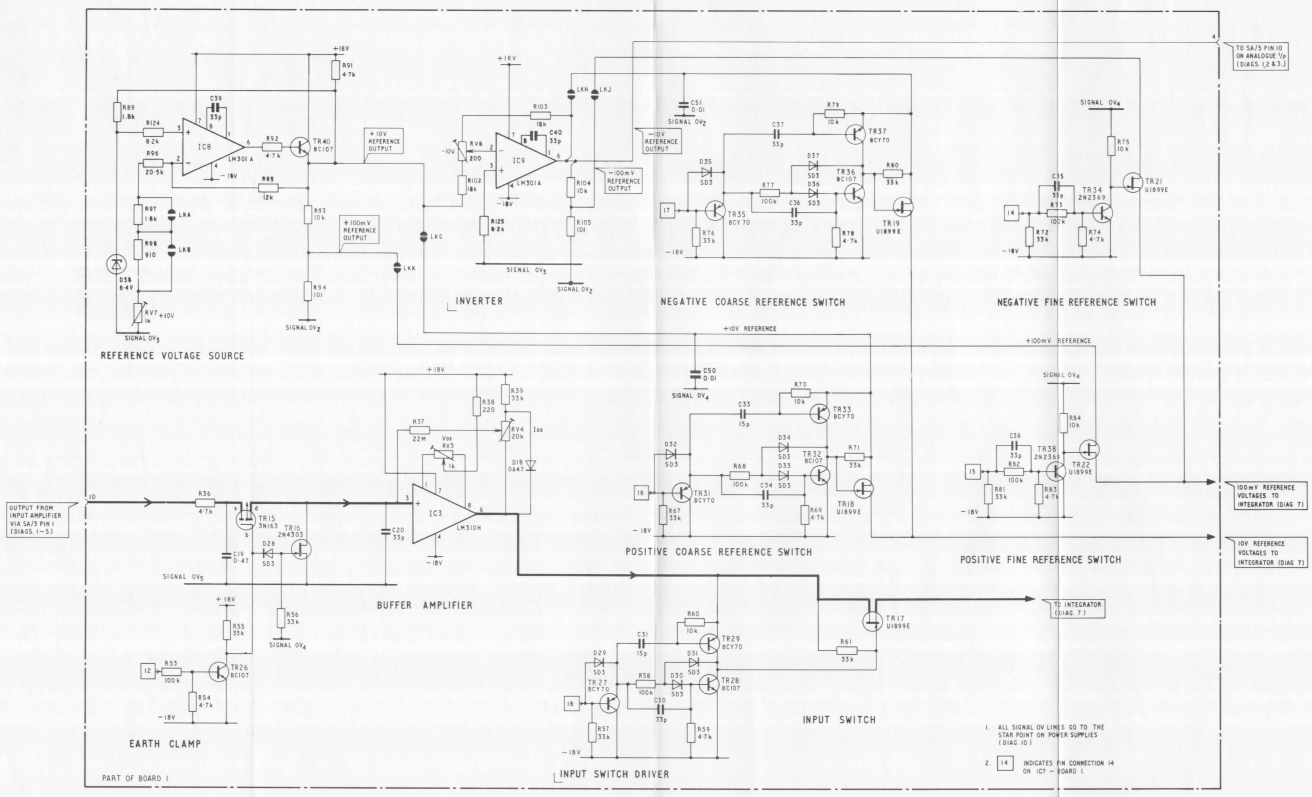
If the input signal was negative during ramp-up, IC7-pin 14 goes low, turning on TR21 during the fine ramp-down period to apply - 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).

POS. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a negative input signal during ramp-up, IC7-pin 16 goes low during the coarse ramp-down period. This turns on TR18 applying +10.000V as a positive reference input to discharge the level (proportional to the applied input signal) stored in the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

POS. FINE REFERENCE SWITCH

If the input signal was positive during ramp-up, IC7-pin 15 goes low, turning on TR22 during the fine ramp-down period to apply + 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).



6 *REFERENCE SWITCHING CIRCUIT DIAGRAM*

INTEGRATOR

INTEGRATOR

IC4 is connected as an operational integrator. The signal input is applied to one side of a differential stage formed by TR23. The other input is a dc level stored in the DRIFT CORRECT circuitry by C23. This maintains the 'virtual earth' of the integrator at 0V with respect to the output of the INPUT BUFFER AMPLIFIER (DIAGRAM 6) and therefore eliminates drift.

X100 AMPLIFIER

The X100 amplifier stage is to enable the COMPARATOR to detect very low integrator outputs, thus accurately defining the end of each ramp-down period.

COMPARATOR

The output of the X100 AMPLIFIER is compared with earth; for a positive input, the output of IC6 will be negative; similarly for a negative input, the output will be positive. The purpose of the comparator is to detect when the input changes from one polarity to the other i.e. when the INTEGRATOR output passes through zero signifying the end of coarse or fine ramp-down as appropriate. The state of this output after completion of ramp-up determines the polarity of the applied coarse and fine reference drives used during the remainder of the measurement cycle. An output of $<+0.5V$ corresponds to positive polarity. A level $> +10V$ corresponds to negative polarity.

DRIFT CORRECT

Between the end of fine ramp-down and the start of the next ramp-up, IC7-pin 11 goes low, turns on TR25 and charges up C23 to the level of the combined offset errors of the INTEGRATOR and INPUT BUFFER AMPLIFIER (DIAGRAM 6) so that during the ramp-up and ramp-down periods, these offsets are compensated for.

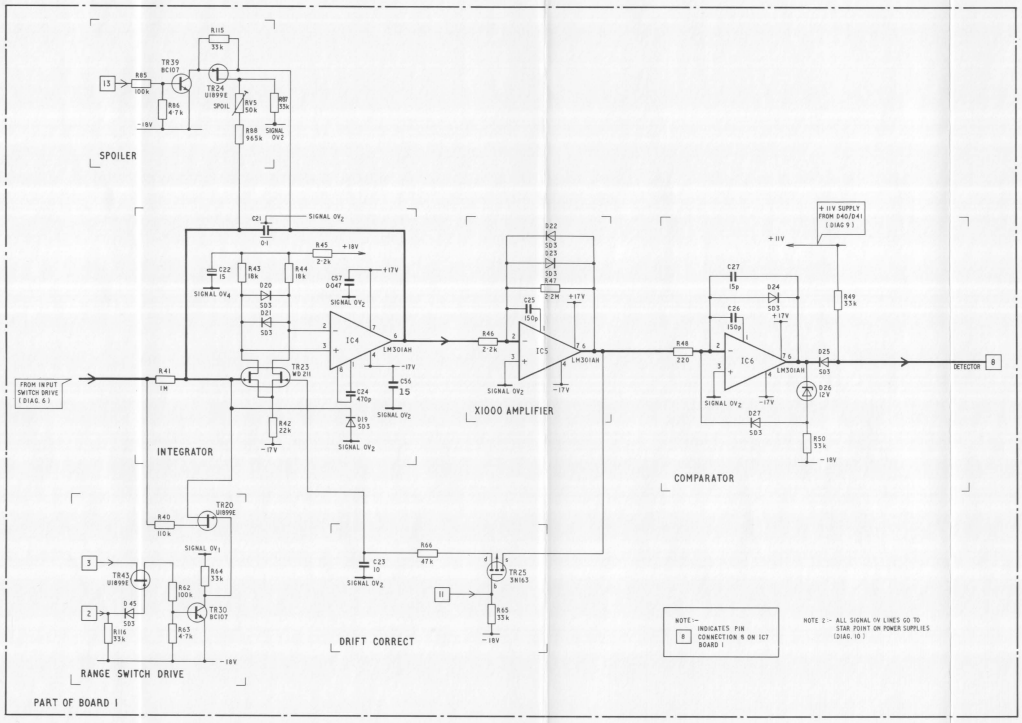
SPOILER

At the end of ramp-up, IC7-pin 13 goes low, TR24 conducts to allow a small proportion of the INTEGRATOR output to be applied to TR23 to hold the charge on C21 until a "mains zero crossing" occurs, thus enhancing series mode rejection.

RANGE SWITCH DRIVE

When IC7 pin 3 goes low, TR30 is turned off. TR44 is turned on selecting an Integrator resistor value of 100kΩ (R40//R41).

When IC7 pin 2 goes low, TR45 is turned off. TR20 is turned on selecting an Integrator resistor value of 10kΩ (R118//R41).



7 INTEGRATOR CIRCUIT DIAGRAM

DISPLAY

7-BAR SEGMENT DRIVERS

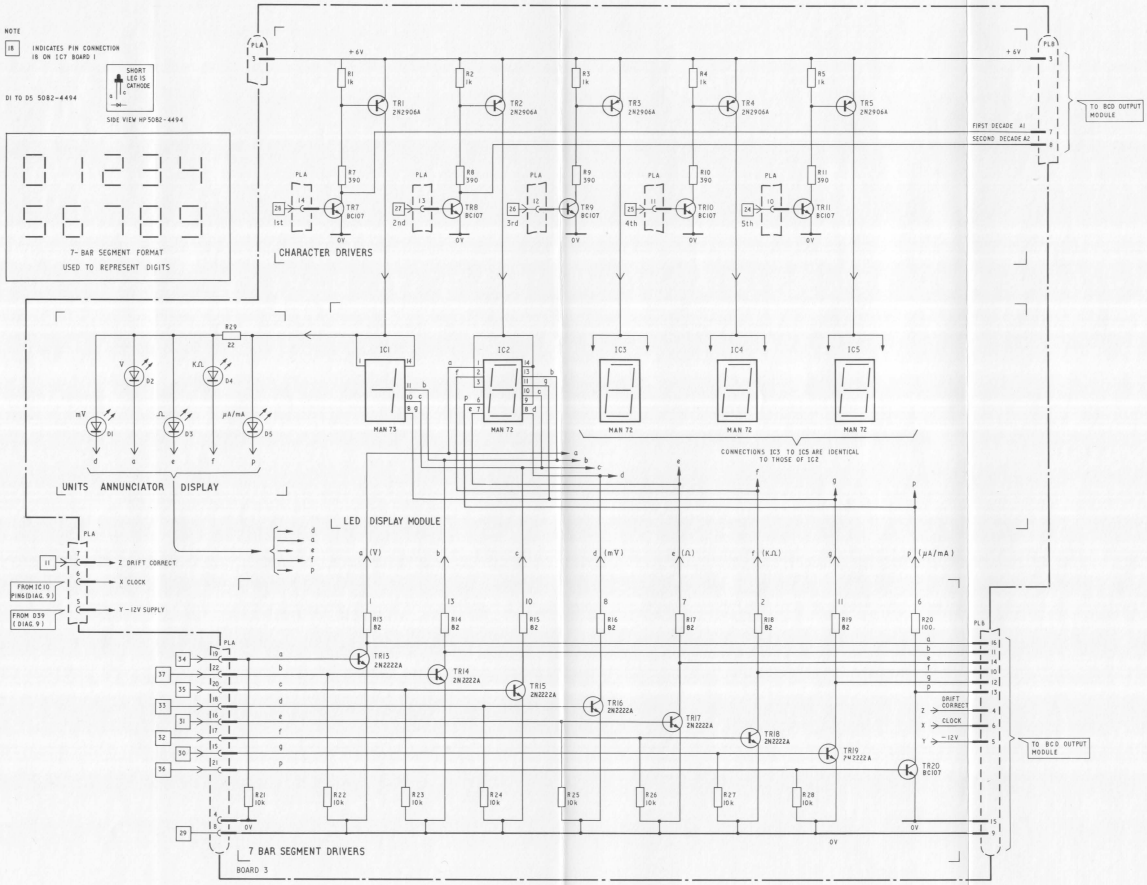
When the relevant output of IC7 goes Hi, the appropriate segment in the display will be lit up, provided that particular character has been selected. For example if IC7 pin 30 goes Hi all the 'g' bars will be selected instantaneously. Since only one CHARACTER DRIVER can be selected at any one time, only the 'g' bar on the selected character will be lit up.

CHARACTER DRIVERS

The characters are displayed serially commencing with the most significant. Whenever the appropriate character input goes Hi all the selected segments within that character will be energised and will light up.

UNITS ANNUNCIATOR DISPLAY

Whenever IC7 pin 28 goes Hi together with any bar segment driver representing a Unit Annunciator (d, a, e, f and p), the affected indicator will light up (mV, V, Ω, kΩ and μA respectively).



8 *DISPLAY CIRCUIT DIAGRAM*

CLOCK AND MODE SELECTION

CLOCK OSCILLATOR

A stable Ceramic Resonator controlled oscillator producing a source of timing pulses at 404kHz.

DIVIDE BY 4

A binary divider stage dividing the input signal by a factor of 4. The resultant output frequency of each output is 101kHz. Reference should be made to the text for details of the phase relationship between each output.

CLOCK DRIVERS

The input clock pulse train (101kHz) drives TR41 and TR42 on and off, forming output pulses between +11V and −18V (maximum amplitude = 28.5V) which are of sufficient amplitude to drive the clock inputs of IC7 (MOS – LSI circuits).

A second output is taken from the emitter of TR42 to provide clock pulses for the BCD Output Module.

MODE SELECTION SWITCH

At each switch position, the appropriate input of IC7 will be held low thus selecting the appropriate mode. When VDC is selected, all the mode inputs go high and the DC mode is assumed.

RELAY DRIVE

Whenever IC7-pin 38 goes high, relay RLB is energised. Diode D10 (Bd. 2) provides a discharge path for the relay coil back emf when the relay is turned off.

IC7 (MOS - LSI) INTEGRATED CIRCUIT

IC7 is illustrated with its function identities and the diagram numbers on which these functions are effected.

The logic used by IC7 is as follows.

Positive Logic:-	Bar Drivers	Negative Logic:-	The remaining functions except the following:-
	IC Drivers (Characters)		Detector
	Top Range		Line Frequency
			Clock (ϕ_1 and ϕ_2)
			Supply Rails

Supply Rail voltages are:-

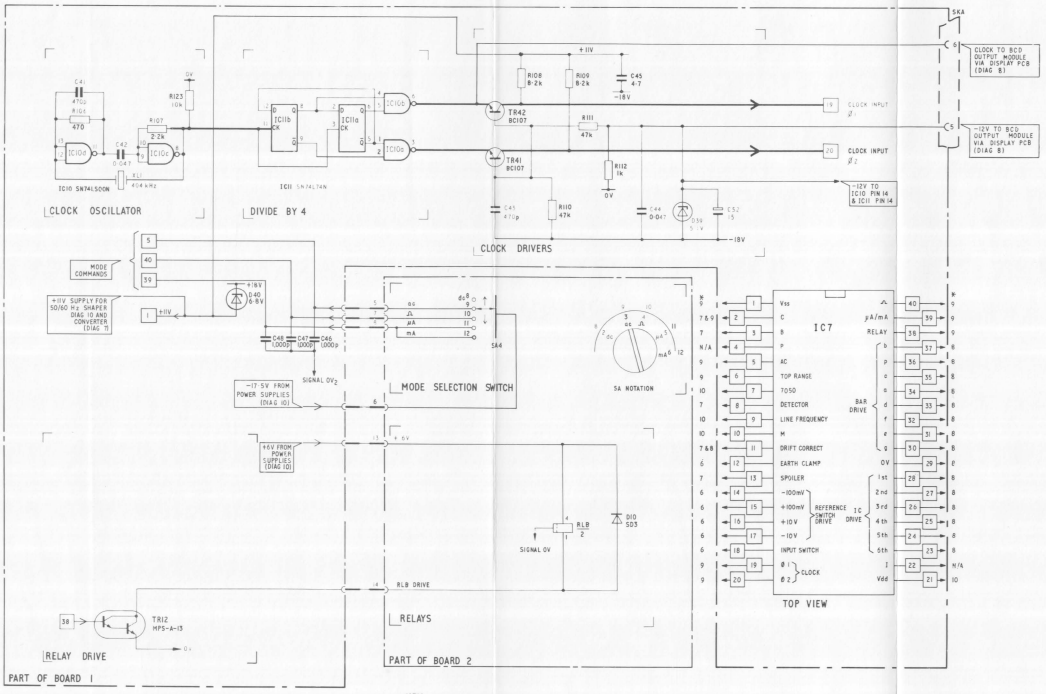
Vss = 11V Nominal

Vdd = −18V Nominal

Vee = 0V

NOTES:-

1. Terminals marked N/A are not used and must not be connected to any other part of the circuitry.
2. Before attempting to remove this MOS Integrated Circuit ensure that all power supplies are switched off and that the necessary anti-static charge measures are taken. See warning on page 3b-5.



NOTES:—
1. RELAY CONTACTS ARE SHOWN ON DIAGRAMS
   5 AC MODE RLB2, RLC1
   1-3 ANALOGUE INPUT RLB 1
   9 MODE SELECTION RLC2
2. [2] INDICATES PIN CONNECTION 2 ON IC7 BOARD 1.
3. ALL 0V AND SIGNAL 0V LINES GO TO STAR POINT ON POWER SUPPLIES (DIAG 10)
4. NUMBERS UNDER M DENOTE DIAGRAMS WHICH ARE AFFECTED

9 *CLOCK AND MODE SELECTION CIRCUIT DIAGRAM*

SUB SECTION 3c Power Supplies

This sub-section deals with the POWER SUPPLIES section of the instrument whose primary function is to provide all the internal dc levels required to operate the instrument.

POWER SUPPLIES

GENERAL ARRANGEMENT

This section of circuitry provides all the dc voltage levels required to operate the instrument.

0V Rails.

Within the instrument, the common return paths (0V rails) are carefully separated to reduce interference. Care should be taken not to short these rails together other than where shown.

Split Pads LKL and LKM (pcb No. 1)

These pads enable the user to isolate the stabilised supplies from the associated section of circuitry. Since these pads are continuations of the printed circuit copper work, care should be taken not to overheat these connections causing the track to lift away from the board.

50/60Hz SHAPER

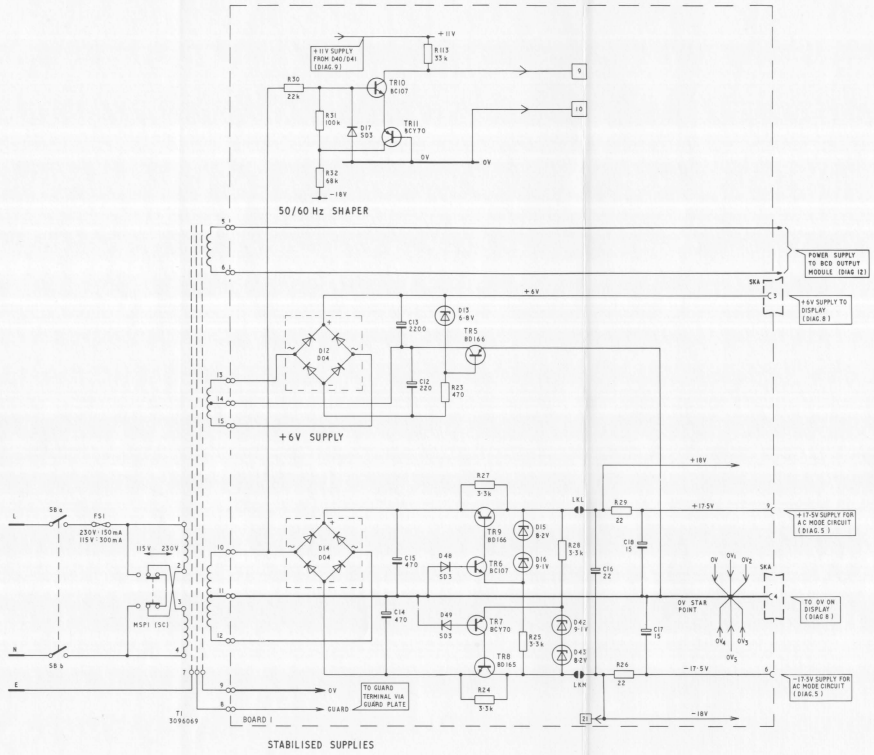
A small proportion of the incoming mains frequency is sampled; the signal is clipped and is used by IC7 (MOS-LS1 circuit) to provide mains zero timing reference points.

VOLTAGE RAIL USAGE

The following table gives the nominal rail voltages provided and the circuit diagrams on which they appear.

+18V	4, 6, 7, 9
−18V	4, 6, 7, 9, 10
+17.5V	4, 5
−17.5V	4, 5, 9
+6V	8, 9

A nominal 10V rms output is available from transformer T1, terminals 5 and 6 for use on the BCD Output Module.



10 *POWER SUPPLIES CIRCUIT DIAGRAM*

SECTION 4 Setting Up & Calibration

INTRODUCTION

This section provides a comprehensive setting-up and calibration procedure which may be necessary after a rectification and/or component replacement on the Digital Multimeter.

It is divided into two parts as follows.

1. Setting-Up Procedures

   These involve partial strip down of the instrument in order to effect initial adjustments of the circuit parameters.

2. Calibration Procedures

   The final adjustments to provide an instrument performance which is compatible with the specification published in Section 6 of this manual.

   For a normal calibration only Part 2 of this section needs to be carried out. Where an instrument fails a calibration, or has had a rectification and/or component replacement, it is advisable to carry out the full procedure detailed in this section.

NOTE:- It is essential when carrying out Part 1 or 2, that the procedure be completed, and carried out in the order given.

TEST EQUIPMENT

The test equipment used must have an accuracy uncertainty equal to or better than that shown in the calibration test tables.

The following test equipment should be available to perform the following procedures correctly.

(a) Variac.

(b) Digital Voltmeter (e.g. Type 7040).

(c) Oscilloscope Type 1740 or A100.

(d) Decade Resistance Standard (e.g. ESI Model RS624).

(e) AC Voltage Standard (e.g. Hewlett Packard Models 745A and 746A).

(f) Decade Voltage Divider (e.g. ESI Model RV622A).

(g) AC Source (e.g. Bradley 232).

(h) DC Source (e.g. Time Model 2003, ± 0.02%).

(j) DC Voltage Standard (e.g. Kintel 351).

(k) 1A current Source (e.g. Fluke 382A)

(l) Resistance Standard. 1Ω ± 0.005% 4 terminal (e.g. Cropico RS1)

(m) Additional items:- Resistor, 1k ohm ± 10% (0.125W).

Resistor, 27k ohm ± 10% (0.125W).

Resistor, 1M ohm ± 10% (0.125W).

Capacitor 1μF (non-polarised).

PART 1. SETTING UP PROCEDURES

PRELIMINARY

1. Prepare the instrument as follows:-

CAUTION:- IT IS ESSENTIAL THAT THE INSTRUMENT BE ISOLATED FROM THE MAINS SUPPLY BEFORE OUTER CASE REMOVAL, DUE TO THE UNCOVERED TERMINALS ON THE ON/OFF SWITCH.

CAUTION:- BEWARE OF GUARD POTENTIAL ON GUARD PLATE WITH INSTRUMENT CASE REMOVED.

a. Remove the 4, 2.5mm screws holding the outer case to the rear panel assembly, Fig. 4.1.

Fig. 4.1. View of Rear Panel, showing location of the 4 securing screws.

b. Select the 'V.DC' mode (This orientates the selector switch shaft with it's key flat facing upwards).

c. Remove the GUARD - Lo link (if fitted).

d. Gently ease out the pcb and rear panel assembly away from the front panel. Fig. 4.5, at rear of section, shows the location and function of each potentiometer.

e. Remove the 2 sets of Berg pins and the 4 screws attaching pcb 2 to pcb 1. Remove pcb 2.

2. Link Berg socket 2 to Berg socket 10.

3. Check that the Mains Selector in the rear panel is set to the appropriate voltage, and that the correct rated fuse is fitted.

For	230V:-	150mA	SLO BLO FUSE
	115V:-	300mA	SLO BLO FUSE

4. Apply power to the instrument and allow a sufficient warm up period.

5. Check that the rail voltages are within the limits specified over the input voltage range as follows.

For	230V:-	195.5 to 253 Volts.
	115V:-	97.75 to 126.5 Volts.

TEST BETWEEN	LIMITS OVER MAINS VARIATION	
	MINIMUM	MAXIMUM
C16 (+ve) to C18 (–ve)	+16.0V	+18V
C16 (–ve) to C18 (–ve)	–16.0V	–18V
C13 (+ve) to C18 (–ve)	+5.7V	+7.0V
C45 (+ve) to C45 (–ve)	+25V	+30V
C52 (+ve) to C52 (–ve)	+4.75V	+5.35V

BUFFER Vos Ios

1. Select 'V.DC' mode. Short circuit Berg sockets 2 and 10. Connect voltmeter between Berg socket 2 and D18 cathode, via a 1k ohm resistor.

2. Adjust RV3 for 0 ± 20μV on voltmeter. Replace the link between Berg sockets 2 and 10 by a 27k ohm resistor.

3. Adjust RV4 for 0 ± 10μV on the voltmeter. Remove voltmeter and two resistors (27k ohm and 1k ohm).

POSITIVE REFERENCE

Select 'V.DC' mode. Using the DC Standard and the Decavider, apply –10V, –1V and –100mV in turn to Berg sockets 2 and 10 (–ve to socket 10), adjusting RV7 to share the error between the three voltage levels evenly as follows:-

–10.000V ± 2 bits

–1.0000V ± 2 bits

–100.00mV ± 2 bits

NOTE:- If RV7 does not have enough adjustment, the links LKA and LKB will require re-adjustment as follows:-

a. Connect –10V (± 0.02% absolute) from DC Standard to Berg sockets 2 and 10 (–ve to socket 10).

b. Ensure that links LKA and LKB are open circuit and that RV7 is at maximum resistance (fully clockwise).

c. Apply –10V standard and note the reading. Look up the range which includes this reading in Table 4.1 and set links LKA and LKB accordingly.

READING RANGES		LINKS	
		A	B
10000	10142	1	1
10129	10283	1	0
10266	10433	0	1
10417	10599	0	0

Legend
0 = Short Circuit

Table 4.1

d. Repeat the –10V, –1V and –100mV test as detailed previously.

RE-ASSEMBLY

1. Fit pcb 2 to pcb 1, securing it by the 4 screws.

2. Fit the link between GUARD and LO terminals and insert the 2 sets of Berg pins into their sockets, ensuring they are fully engaged.

INPUT AMPLIFIER

NOTE:- The waveform at TR3 collector, using a dc coupled oscilloscope set to 1V/cm and 1ms/cm, should be a square wave; amplitude 4V ± 0.4Vpp, period 4ms ± 1ms, mark/space ratio 1 : 1 ± 10%.

1. Select 'V.DC' mode and short circuit the input terminals. Ensure that RV1 range of adjustment is greater than ± 80μV.

2. Remove the short circuit from the input terminals. Apply +100μV and −100μV alternately to the input terminals, using a dc source having an output resistance of 10k ohms.

3. Adjust RV1 for equal positive and negative readings.

4. Remove dc source and connect a 1M ohm resistor and 1μF non-polarised capacitor in parallel between the Hi and Lo terminals.

5. Adjust RV2 for a zero reading, ± 10μV. Remove resistor and capacitor.

6. Repeat tests 2 to 5 inclusive until the errors are within the limits:-

Input:-	+100μV/−100μV	Reading:-	0.10mV ± 1 bit
Input:-	1MΩ//1μF	Reading:-	0.00mV ± 10 bits

NOTE:- If adjustment is necessary repeat operations 2 to 5 inclusive.

7. Remove the dc source.

NEGATIVE REFERENCE

1. Select 'V.DC' mode.

2. Connect 10V ± 0.02% absolute across the 6 decade Decavider, using the DC Standard.

3. Apply +10V, −10V, +1V, −1V, +100mV and −100mV dc in turn to the input terminals.

4. Adjust on RV8 to make the negative reading equal to the positive reading at each voltage level.

5. Share errors between RV7 and RV8 such that the:-

± 10V Inputs read	± 10.000 ± 2 bits
± 1V Inputs read	± 1.0000 ± 2 bits
± 100mV Inputs read	± 100.00 ± 2 bits

NOTE:- Problems in meeting these limits will result if the 'ON' resistance of TR's 17, 18, 19 and 20 are not matched. See Appendix.

LINEARITY

1. Select 'V.DC' mode. With the 10V DC Standard and Decavider connected to the input terminals as in previous test, check the linearity in accordance with Table 4.2.

INPUT	READING	TOLERANCE
10.0	10.000V	± 3 bits
5.0	5.000V	± 2 bits
1.05	1.050V	± 1 bit
	RANGE CHANGE	
0.95	950.0mV	± 2 bits
1.05	1.0500V	± 2 bits
	RANGE CHANGE	
1.15	1.150V	± 1 bit
	RANGE CHANGE	
0.5	500.00mV	± 2 bits
	RANGE CHANGE	
0.095	95.00mV	± 2 bits
0.01	10.00mV	± 2 bits
0.001	1.00mV	± 2 bits
0.0001	0.10mV	± 2 bits
0.00005	0.05mV	± 2 bits
0.00003	0.03mV	± 2 bits
0.00002	0.02mV	± 2 bits
0.00001	0.01mV	± 2 bits

Table 4.2

2. Repeat for negative values using the same voltage source.

3. If the DMM falls outside the linearity tolerances, it is recommended that the Setting Up Procedure should be repeated.

OHMS MODE

1. Set to 'Ω' mode and short circuit the input terminals. The reading should be 0 ± 3 bits.

2. Connect 100k ohms ± 0.01% absolute across the input terminals. Adjust RV2 (pcb 2) to obtain 100.00kΩ reading.

DC ATTENUATOR

Select 'V.DC' mode and connect input terminals to 100V ± 0.01% absolute. Adjust RV1 (pcb 2) to give 100.00V reading.

DC μA

Select 'μA.DC' mode and connect input to 1000μA ± 0.01% absolute current source (100k ohms from 100V is convenient). Adjust RV6 (pcb 2) to give 1000.0μA ± 1 bit reading.

DC mA

1. Select 'mA DC' mode, and open circuit terminals. Reading should be 0.000mA ±10 bits (excluding noise, which should not exceed 14 bits). Adjust RV1 as required.

   Note: If adjustment of RV1 is necessary to achieve the specified reading, the INPUT AMPLIFIER checks and adjustment will have to be repeated.

2. Connect 95/950mA Current Source in series with 1Ω ±0.01% Standard Resistor to the input terminals, monitoring the voltage across the Resistor with a voltmeter calibrated to ±0.01% accuracy (e.g. 7050 dvm).

3. Adjust the current source for a nominal 500.0mV ±10% reading on the monitor voltmeter. Adjust RV9 on pcb 2 to give the same reading of 500.0mA ±1 bit.

4. Increase the current to 950mA ±10% and check that the reading will hold for 1 minute.

5. Remove the Current Source.

AC ZERO

Switch to 'V.AC' mode. Short circuit TR1 (pcb 2) collector (case) to 0V. Adjust RV4 until the readings stop reducing. Reading must be less than 5 bits. Remove the short circuit.

AC SCALE

1. Select 'V.AC' mode. Connect the input 1V ± 0.1% absolute 1kHz sinewave. On pcb 2, adjust RV3 to give 1.0000V ± 5 bits.

AC ATTENUATOR

1. Select 'V.AC' mode. Connect the input to 10V ± 0.2% absolute 1kHz sinewave. Adjust RV5 (pcb 2) to obtain 10.000V ± 5 bits.

INTERFERENCE REJECTION

SERIES MODE

1. Connect instrument as shown in Fig. 4.2.

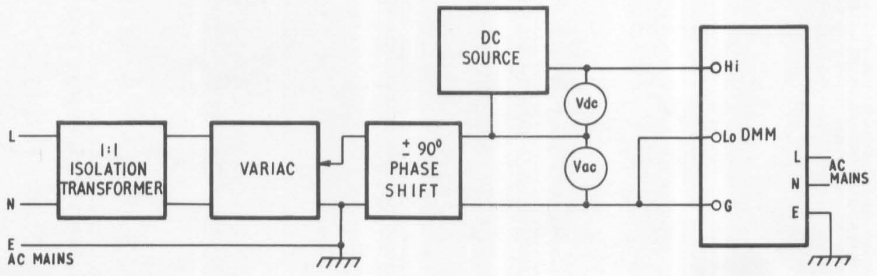


Fig. 4.2. Interference Rejection:- Series Mode Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to approximately 500mV and (V.ac) to zero. Note the instrument reading.

3. Increase (V.ac) to 1 Volt. Reading must not change by more than 1mV.

COMMON MODE

AC Rejection

1. Connect instrument as shown in Fig. 4.3.

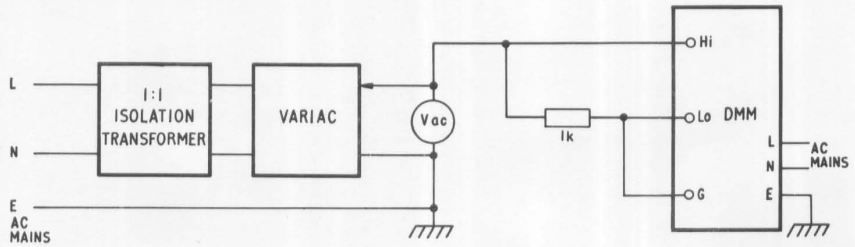


Fig. 4.3. Interference Rejection:- Common Mode (ac) Test Circuit.

2. Switch to 'V.AC' mode and set (V.ac) to 100V. Reading shall be less than 100mV.

DC Rejection

1. Connect instrument as shown in Fig. 4.4.

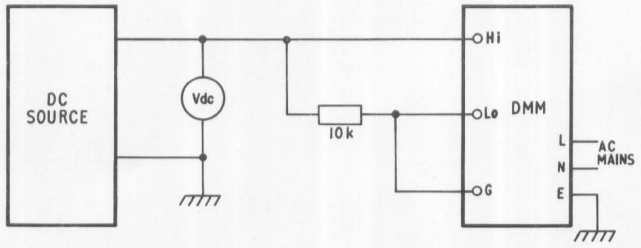


Fig. 4.4. Interference Rejection:- Common Mode (dc) Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to 500V. Reading shall be less than 5mV.

This concludes the setting up of the DMM and it should now be followed by a full calibration.

PART 2. CALIBRATION PROCEDURES

INTRODUCTION

The following calibration is basically the final calibration to which all instruments are subjected, prior to despatch from the factory.

For the greatest accuracy the DMM should be removed from its case and fitted into a Setting Up Case, Part No. 70502 before a calibration is attempted. Failing this, allowances must be made for variations in the working temperatures.

See Appendix for details of Setting Up Case.

PRELIMINARY PROCEDURE

The DMM will have to be removed from its case and fitted into the Setting Up Case (if available).

CAUTIONARY NOTES

1. IT IS ESSENTIAL THAT THE INSTRUMENT BE COMPLETELY ISOLATED FROM THE MAINS SUPPLY BEFORE REMOVING THE CASE, DUE TO THE POSITION AND UNPROTECTED NATURE OF THE ON/OFF SWITCH TERMINALS.

2. BEWARE OF THE GUARD PLATE POTENTIAL WITH INSTRUMENT CASE REMOVED.

1. Remove the 4, 2.5mm screws which secure the DMM case to the rear panel. See Fig. 4.1.

2. Remove the GUARD - Lo link (if fitted).

3. Gently ease out the rear panel and pcb assembly, away from the front panel.

4. Fit assembly into the Setting Up Case (if available), or position assembly in convenient position with the guard plate insulated if required and with easy access to the potentiometers.

5. Ensure that the correct mains selection has been made and that the correct rated fuse is fitted.

   For 230V:- 150mA SLO BLO

   115V:- 300mA SLO BLO

CALIBRATION

The calibration sequence must be carried out in the order given. Calibration should be carried out at an ambient temperature 23°C ± 1°C after a warm-up period of approximately half an hour in the Setting-Up Case.

STANDARD SETTINGS

During the warm up period the DMM should be set to the following standard conditions.

1. Mode set to 'V.DC'.

2. Input terminals short circuited.

3. Apply power to the DMM and switch instrument ON.

CALIBRATION PROCEDURE 1

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	± %		VALUE	± bits	
1	1MΩ//1μF	10	Adj. Bd.1/RV2.	± 0.00mV	2	
2	S/C	–	Adj. Bd.1/RV1.	± 0.00mV	0	
3	1MΩ//1μF	10	Adj. Bd.1/RV2.	± 0.00mV	10	
4	+0.10mV	2	Adj. Bd.1/RV1 and repeat for equal +ve and –ve readings.	0.10mV	2	
5	–0.10mV	2		–0.10mV	2	
6	S/C	–	Check.	± 0.00mV	2	
7	+9.500V	0.004	Adj. Bd.1/RV7. (1)	9.500V	1	
8	+9.500V	0.004	Check, with 1MΩ in series.	9.500V	5	
9	–9.500V	0.004	Adj. Bd.1/RV8. (1)	–9.500V	2	

NOTES:-

(1) Adjust for equal reading, split any deviations equally between readings.

CALIBRATION PROCEDURE 2

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	± %		VALUE	± bits	
1	105.00kΩ	0.01	Adj Bd 2/RV2	105.00kΩ	1	
2	50.00kΩ	0.01	Check	50.00kΩ	2	
3	5.000kΩ	0.01	Check	5.000kΩ	3	
4	10.500kΩ	0.01	Check	10.500kΩ	4	
5	867.8Ω	0.01	Check	867.8Ω	5	
6	1.0500kΩ	0.01	Check	1.0500kΩ	6	
7	O/C	–	Overload Check (1)	1–––– kΩ	–	
8	S/C	–	Check	0.0Ω	3	

NOTES:-

(1) Ensure that overload condition is indicated by a steady '1' being displayed and that the remaining 4 characters are blanked out.

CALIBRATION PROCEDURE 3

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	± %		VALUE	± bits	
1	+9.500V	0.004	Check.	9.500V	2	
2	+1.200V	0.004	Check.	1.200V	1	
3	+0.9500V	0.004	Check.	950.0mV	2	
4	+120.0mV	0.004	Check.	120.0mV	1	
5	+10.00mV	0.02	Check.	10.00mV	2	
6	+95.00mV	0.004	Check.	95.00mV	3	
7	−9.500V	0.004	Check.	−9.500V	2	
8	−1.200V	0.004	Check.	−1.200V	1	
9	−0.9500V	0.004	Check.	−950.0mV	2	
10	−120.0mV	0.004	Check.	−120.0mV	1	
11	−10.00mV	0.02	Check.	−10.00mV	2	
12	−95.00mV	0.004	Check.	−95.00mV	3	
13	+95.00V	0.004	Adj. Bd.2/RV1.	95.00V	2	
14	+1000.0V	0.005	Check.	1000.0V	5	
15	−120.0V	0.004	Check.	−120.0V	1.5	

CALIBRATION PROCEDURE 4

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	± %		VALUE	± bits	
1	500.0kΩ	0.01	Check	500.0kΩ	2	
2	1.0500MΩ	0.01	Check	1050.0kΩ	4	
3	10.000MΩ	0.05	Check	1000kΩ	10	
4	5.000MΩ	0.05	Check	5000kΩ	7	

CALIBRATION PROCEDURE 5

Select 'μA.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	± %		VALUE	± bits	
1	O/C	–	Check.	0.000μA	2	
2	+1.0000mA (1)	0.01	Adj.Bd.2/RV6 (5)	1000.0μA	4	
3	+9.000μA (2)	0.001	Check.	9.000μA	5	
4	+1.000μA (3)	0.05	Check.	1.000μA	2	
5	–20V	10	Overload check. (4)	–1----μA	–	
6	–1.0000mA (1)	0.01	Check.	–1000.0μA	4	
7	–9.000μA (2)	0.01	Check.	–9.000μA	5	
8	–1.000μA (4)	0.05	Check.	–1.000μA	2	

NOTES:-

(1) Recommend 100V source via a 100k ohm resistor.

(2) Recommend 9V source via a 1M ohm resistor.

(3) Recommend 1V source via a 1M ohm resistor.

(4) Ensure that overload is indicated by flashing '1' with the remaining 5 characters blanked out.

(5) For adjustment of this potentiometer the case must be removed.

CALIBRATION PROCEDURE 6

Select 'mADC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULTS
	VALUE	±%		VALUE	± bits	
1	O/C	–	Check	±0.000mA	30	
2	95.00mA	0.01	Check	95.00mA	7	

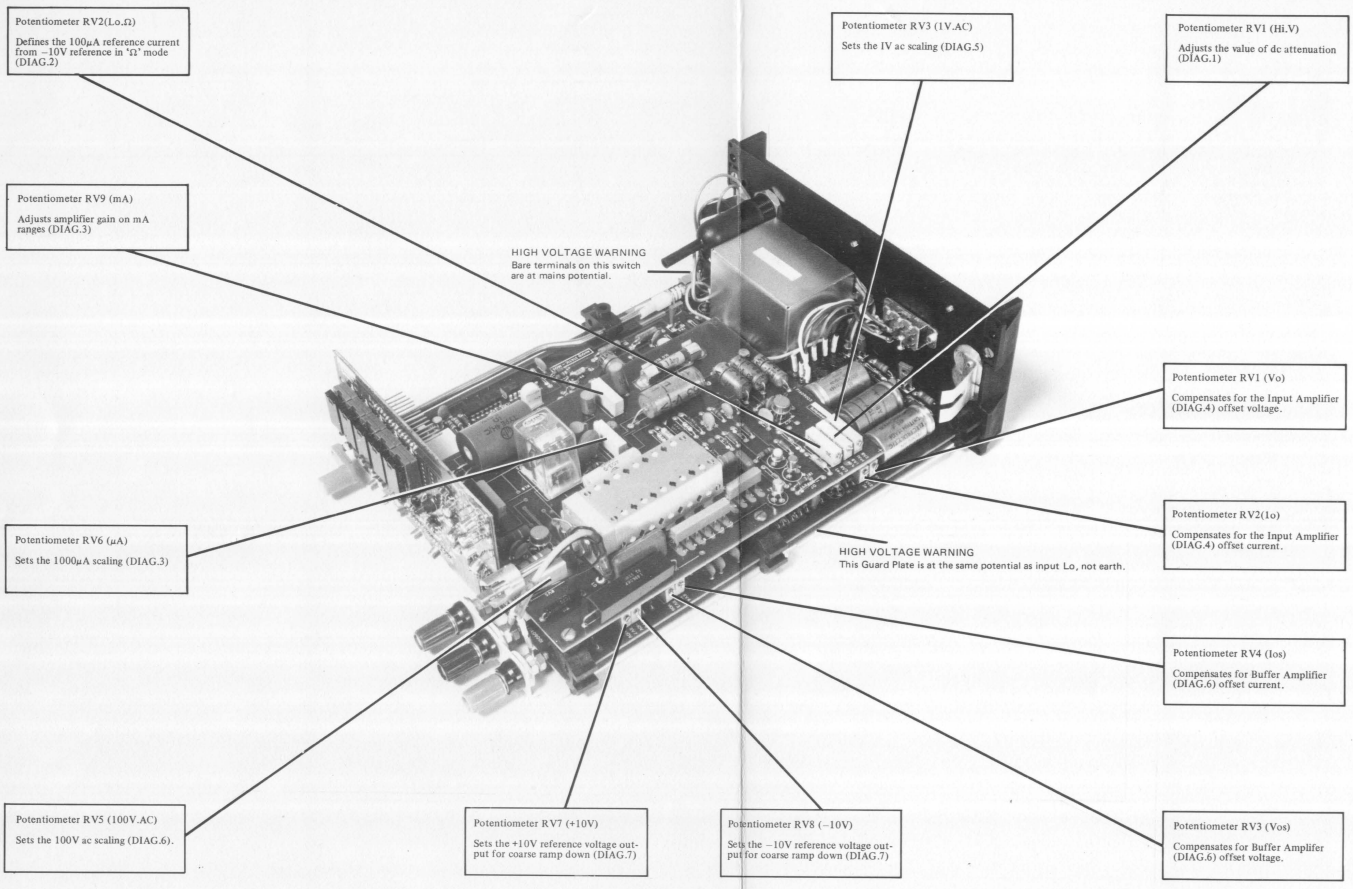


Fig. 4.5. View of PCB Assembly, identifying the Potentiometers and their Functions.

CALIBRATION PROCEDURE 7

Select 'VAC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	±bits	
1	0.9500V	0.02	At 1kHz Adjust Bd.2/RV3	950.0mV	3	
2	1.00mV	1	At 1kHz Adjust Bd.1/RV4	1.00mV	2	
3	S/C	–	Check	0.00	7	
4	500.0mV	0.02	At 1kHz Check	500.0mV	6	
5	95.00mV	0.02	At 1kHz Check	95.00mV	10	
6	0.9500V	0.05	At 40kHz Check	950.0mV	12	
7	0.9500V	0.05	At 20kHz Check	950.0mV	12	
8	0.9500V	0.02	At 10kHz Check	950.0mV	12	
9	95.00mV	0.02	At 10kHz Check	95.00mV	15	
10	9.500V	0.02	At 1kHz Adjust Bd.2/RV5	9.500V	2	
11	95.00V	0.02	At 1kHz Check	95.00V	10	
12	1.200V	0.02	At 1kHz Check	1.200V	6	
13	9.500V	0.02	At 10kHz Check	9.500V	18	
14	95.00V	0.02	At 10kHz Check	95.00V	15	
15	750.00V	0.05	At 1kHz Check	750.00V	12	
16	500.0V	0.05	At 10kHz Check	500.0V	10	
17	9.500V	0.02	At 20kHz Check	9.500V	18	

NOTES:-

(1) For adjustment of this potentiometer the case must be removed.

This concludes the calibration of the DMM. If the instrument fails any of the prescribed tests it is suggested that the Setting Up Procedures in Section 4 be carried out, followed by a further calibration before any fault diagnosis is attempted.

The serviceable DMM should now be isolated from the supplies and refitted into its case.

NOTE:- Ensure that 'V.DC' is selected on both the switch and the front panel knob to ensure correct mating of the key flat.

SECTION 5 Parts Lists

This section contains detailed parts lists for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts list.

COMPONENT PARTS LIST ABBREVIATIONS

CIRCUIT REFERENCES

AE	Aerial
B	Battery
C	Capacitor (μF)
CSR	Thyristor
D	Diode
FS	Fuse
IC	Integrated Circuit
L	Inductor
LP	Lamp (including Neon)
LK	Link
M	Motor
ME	Meter
MSP	Mains Selector Panel
PL	Plug
R	Resistor (Ω)
RE	Recording Instrument
RL	Relay
S	Switch
SK	Socket
T	Transformer
TP	Terminal Post (or Test Point)
TR	Transistor
V	Valve
X	Other Components

Also Used:-

RNL	Non Linear Resistor (Ω)
RV	Variable Resistor (Ω)

COMPONENT TYPES

Fixed Resistors		Variable Resistors		Capacitors	
Carbon Composition	CACP	Carbon Front Panel Multiturn	CAFM	Air	AIR
Carbon Film	CAFM	Carbon Front Panel Single Turn	CAFS	Aluminium Electrolytic	ALME
Cracked Carbon	CKCA	Carbon Preset Multiturn	CAPM	Aluminium Solid	ALMS
Metal Film	MEFM	Carbon Preset Single Turn	CAPS	Polycarbonate	CARB
Metal Oxide	MEOX	Cermet Front Panel Multiturn	CMFM	Ceramic	CERM
Power Wirewound	POWW	Cermet Front Panel Single Turn	CMFS	Polyester Foil	ESTF
Precision Wirewound	PRWW	Cermet Preset Multiturn	CMPM	Polyester Metallised	ESTM
Temperature Sensitive	TEMP	Cermet Preset Single Turn	CMPS	Glass	GLAS
Thick Film	TKFM	Wirewound Front Panel Multiturn	WWFM	Mica	MICA
Thin Film	TNFM	Wirewound Front Panel Single Turn	WWFS	Metallised Lacquer	MLAC
Voltage Sensitive	VOLT	Wirewound Preset Multiturn	WWPM	Paper Foil	PAPF
		Wirewound Preset Single Turn	WWPS	Paper Metallised	PAPM
				PTFE	PTFE
				Polypropylene Film	PYLN
				Polystyrene	STYR
				Tantalum Dry	TAND
				Tantalum Foil	TANF
				Tantalum Wet	TANW

PCB No. 1

Cct Ref	General Description				Solartron Part No.
R1	CACP	1000	1/8W	10%	172031000
R2	CACP	470	1/8W	10%	172024700
R3	CACP	47k	1/8W	10%	172044700
R4	CACP	47k	1/8W	10%	172044700
R5	CACP	10	1/8W	10%	172011000
R6	CACP	1.5M	1/8W	10%	172061500
R7	CACP	220k	1/8W	10%	172052200
R8	CACP	22	1/8W	10%	172012200
R9	CACP	220k	1/8W	10%	172052200
R10	CACP	2.2k	1/8W	10%	172032200
R11	CACP	220k	1/8W	10%	172052200
R12	CACP	220k	1/8W	10%	172052200
R13	CACP	100	1/8W	10%	172021000
R14 to R19	MEOX	22k	1/4W	5%	195642200
R20	MEOX	9.1k	1/4W	5%	195639100
R21	MEOX	9.1k	1/4W	5%	195639100
R22	MEOX	100k	1/4W	5%	195651000
R23	MEOX	470	1/2W	5%	193524700
R24	CACP	3.3k	1/4W	10%	172333300
R25	CACP	3.3k	1/4W	10%	172333300
R26	CACP	22	1/8W	10%	172012200
R27	CACP	3.3k	1/4W	10%	172333300
R28	CACP	3.3k	1/4W	10%	172333300
R29	CACP	47	1/8W	10%	172014700
R30	CACP	22k	1/8W	10%	172042200
R31	CACP	100k	1/8W	10%	172051000
R32	CACP	68k	1/8W	10%	172046800
R36	CACP	4.7k	1/8W	10%	172034700
R37	CACP	22M	1/4W	10%	172372200
R38	CACP	220	1/8W	10%	172022200
R39	CACP	33k	1/8W	10%	172043300
R40	MEFM	110k	1/4W	0.5%	198251101
R41	MEFM	1M	1/4W	1%	198361002
R42	MEOX	22k	1/4W	5%	195642200
R43	MEFM	18k	1/8W	0.5%	192741802
R44	MEFM	18k	1/8W	0.5%	192741802
R45	CACP	2.2k	1/8W	10%	172032200
R46	CACP	2.2k	1/8W	10%	172032200
R47	CACP	220k	1/8W	10%	172052200
R48	CACP	220	1/8W	10%	172022200
R49	CACP	33k	1/8W	10%	172043300
R50	CACP	33k	1/8W	10%	172043300
R53	CACP	100k	1/8W	10%	172051000
R54	CACP	4.7k	1/8W	10%	172034700
R55	CACP	33k	1/8W	10%	172043300
R56	CACP	33k	1/8W	10%	172043300
R57	CACP	33k	1/8W	10%	172043300
R58	CACP	100k	1/8W	10%	172051000
R59	CACP	4.7k	1/8W	10%	172034700
R60	CACP	10k	1/8W	10%	172041000
R61	CACP	33k	1/8W	10%	172043300
R62	CACP	100k	1/8W	10%	172051000
R63	CACP	4.7k	1/8W	10%	172034700
R64	CACP	33k	1/8W	10%	172043300
R65	CACP	33k	1/8W	10%	172043300
R66	CACP	1M	1/8W	10%	172061000
R67	CACP	33k	1/8W	10%	172043300
R68	CACP	100k	1/8W	10%	172051000
R69	CACP	4.7k	1/8W	10%	172034700
R70	CACP	10k	1/8W	10%	172041000
R71	CACP	33k	1/8W	10%	172043300
R72	CACP	33k	1/8W	10%	172043300
R73	CACP	100k	1/8W	10%	172051000
R74	CACP	4.7k	1/8W	10%	172034700
R75	CACP	10k	1/8W	10%	172041000
R76	CACP	33k	1/8W	10%	172043300
R77	CACP	100k	1/8W	10%	172051000
R78	CACP	4.7k	1/8W	10%	172034700

Cct Ref.	General Description				Solartron Part No.
R79	CACP	10k	1/8W	10%	172041000
R80	CACP	33k	1/8W	10%	172043300
R81	CACP	33k	1/8W	10%	172043300
R82	CACP	100k	1/8W	10%	172051000
R83	CACP	4.7k	1/8W	10%	172034700
R84	CACP	10k	1/8W	10%	172041000
R85	CACP	100k	1/8W	10%	172051000
R86	CACP	4.7k	1/8W	10%	172034700
R87	MEFM	33k	1/8W	0.5%	192743302
R88	MEFM	990k	1/4W	0.25%	160400488
R89	MEFM	1.8k	1/4W	0.5%	198231801
R91	CACP	4.7k	1/8W	10%	172034700
R92	CACP	4.7k	1/8W	10%	172034700
R93	MEFM	10k	1/8W	.25%	192841002
R94	MEFM	101	1/8W	.25%	192821012
R95	MEFM	12k	1/10W	0.5%	169607901
R96	MEFM	20.5k	1/10W	0.5%	169607901
R97	MEFM	1.8k	1/8W	1%	192731801
R98	MEFM	910	1/8W	1%	192729101
R102	MEFM	18k	1/10W	0.5%	169607301
R103	MEFM	18k	1/10W	0.5%	169607301
R104	MEFM	10k	1/8W	.25%	192841002
R105	MEFM	101	1/8W	.25%	192821012
R106	CACP	470	1/8W	10%	172024700
R107	CACP	2.2k	1/8W	10%	172032200
R108	CACP	8.2k	1/8W	10%	172038200
R109	CACP	8.2k	1/8W	10%	172038200
R110	CACP	47k	1/8W	10%	172044700
R111	CACP	47k	1/8W	10%	172044700
R112	MEOX	1000	1/4W	5%	195631000
R113	CACP	33k	1/8W	10%	172043300
R115	CACP	33k	1/8W	10%	172043300
R117	MEFM	100	1/4W	0.5%	192721002
R118	MEFM	10k	1/4W	0.5%	198241001
R119	CACP	33k	1/8W	10%	172043300
R120	CACP	100k	1/8W	10%	172051000
R121	CACP	4.7k	1/8W	10%	172034700
R122	CACP	10k	1/8W	10%	172041000
R123	CACP	10k	1/8W	10%	172041000
R124	CACP	8.2k	1/8W	10%	172038200
R125	CACP	8.2k	1/8W	10%	172038200
C1	ESTM	.22	100V	10%	225452200
C2	ESTM	.047	100V	10%	225444700
C3	TANW	330	6V	10%	265183300
C4	CERM	3.3p	200V	15%	240603300
C5	ESTM	0.47	63V	10%	225154700
C6	TANW	47	6V	20%	265274700
C7	CERM	150p	500V	20%	241321500
C8	CERM	15p	500V	20%	241311500
C9	ESTM	.47	63V	10%	225154700
C10	CERM	2.2p	200V	15%	240602200
C11	ESTM	.47	63V	10%	225154700
C12	ALME	220	16V	-20% +100%	273382200
C13	ALME	2200	10V	-10% +100%	273192200
C14	ALME	470	40V	-10% +100%	273784700
C15	ALME	470	40V	-10% +100%	273784700
C16	ALME	22	40V	-10% +100%	273772200
C17	TANW	15	20V	20%	265871500
C18	TANW	15	20V	20%	265871500
C19	ESTM	0.47	63V	10%	225154700
C20	CERM	33p	500V	20%	241313300
C21	PTFE	.1	100V	2%	208950001
C22	TANW	15	20V	20%	265871500
C23	ESTM	4.7	63V	20%	219964700
C24	CERM	470p	500V	20%	241324700

Cct Ref.	General Description				Solartron Part No.
C25	CERM	150p	500V	20%	241321500
C26	CERM	150p	500V	20%	241321500
C27	CERM	15p	500V	20%	241311500
C30	CERM	33p	500V	20%	241313300
C31	CERM	15p	500V	20%	241311500
C33	CERM	15p	500V	20%	241311500
C34 to C40	CERM	33p	500V	20%	241313300
C41	CERM	100p	500V	20%	241321000
C42	CERM	.047	25V	+50% -25%	241944700
C43	CERM	470p	500V	20%	241324700
C44	CERM	.047	25V	+50% -25%	241944700
C45	TANW	4.7	35V	20%	266064700
C46 to C48	CERM	1000p	500V	20%	241331000
C50	CERM	0.01	25V	-25% +50%	241941000
C51	CERM	0.01	25V	—25% +50%	241941000
C52	TANW	15	20V	20%	265871500
C53	ESTM	0.033	100V	10%	225443300
C54	CERM	3.3p	200V	15%	240603300
C55	CERM	3.3p	200V	15%	240603300
C56	TANW	15	20V	±20%	265871500
C57	CERM	0.047	25V	+50% —25%	241944700
D1	SD3				300522160
D2	SD3				300522160
D3	IN3595				300523590
D4	IN3595				300523590
D5	Zener	12V	.4W	5%	300521480
D6	Zener	12V	.4W	5%	300521480
D7	SD3				300522160
D8	SD3				300522160
D9	SD3				300522160
D10	Zener	3.9V	.4W	5%	300521420
D11	Zener	3.9V	.4W	5%	300521420
D12	W04				300524700
D13	Zener	6.8V	.4W	5%	300522540
D14	W04				300524700
D15	Zener	8.2V	.4W	5%	300521330
D16	Zener	9.1V	.4W	3%	300525590
D17	SD3				300522160
D18	OA47				300520850
D19 to D25	SD3				300522160
D26	Zener	12V	.4W	5%	300521480
D27 to D37	SD3				300522160
D38	Zener	6.4V	1/4W	5%	300525050
D39	Zener	5.1V	.4W	5%	300521310
D40	Zener	6.8V	.4W	5%	300522540
D41	HP5082				300524910
D42	Zener	9.1V	.4W	3%	300525590
D43	Zener	8.2V	.4W	5%	300521330
D48	SD3				300522160
D49	SD3				300522160
D50	IN3595				300523590
D51	IN3595				300523590
RV1	CMPM	1M	1/3W	10%	130661000
RV2	CMPM	20k	1/3W	10%	130642000
RV3	CMPM	1000	1/3W	10%	130631000
RV4	CMPM	20k	1/3W	10%	130642000
RV7	CMPM	1k	1/3W	10%	130631000
RV8	CMPM	200	1/3W	10%	130622000

Cct Ref.	General Description	Solartron Part No.
TR1	40673	300555210
TR2	40673	300555210
TR3	BC107	300553320
TR4	BC107	300553320
TR5	BD166	300555150
TR6	BC107	300553320
TR7	BCY70	300553590
TR8	BD165	300555160
TR9	BD166	300555150
TR10	BC107	300553320
TR11	BCY70	300553590
TR12	MPS-A-13	300554560
TR13	BC107	300553320
TR14	BC107	300553320
TR15	3N163	300554530
TR16	2N4303	300553160
TR17 to TR22	U1899E	300554320
TR23	WD211	300555060
TR24	U1899E	300554320
TR25	3N163	300554530
TR26	BC107	300553320
TR27	BCY70	300553590
TR28	BC107	300553320
TR29	BCY70	300553590
TR30	BC107	300553320
TR31	BCY70	300553590
TR32	BC107	300553320
TR33	BCY70	300553590
TR34	2N2369	300552390
TR35	BCY70	300553590
TR36	BC107	300553320
TR37	BCY70	300553590
TR38	2N2369	300552390
TR39 to TR42	BC107	300553320
TR44	U1899E	300554320
TR45	BC107	300553320
IC1	LM301AH	510000620
IC2	LM301AH	510000620
IC3	LM310H	510090040
IC4	LM301AH	510000620
IC5	LM301AH	510000620
IC6	LM301AH	510000620
IC7	MOS Logic	519600304
IC8	LM301AH	510000620
IC9	LM301AH	510000620
IC10	SN74LS00N	510002000
IC11	SN74L74N	510001110
X1	Ceramic Resonator	301900101
	Vertical P.V. Socket	352501690
	Horizontal Receptacle	352501700
SB	Push Button Switch	379601001
	40 Way D.I.L. I.C. Socket	300584880
	Disconnect Crimp	351501070
	Disconnect Pin	355900550

PCB No. 2

Cct Ref.	General Description				Solartron Part No.
*R1	MEFM	9.95M	2W	0.25%	169603802
*R2	MEFM	100.5k	1W	0.25%	169603802
R5	CACP	1000	1/8W	10%	172031000
R6	PRWW	9.975k	1/3W	0.1%	160300407
R7	CACP	10k	1/8W	10%	172041000
R8	CACP	100k	1W	10%	172551000
R9	CACP	1M	1W	10%	172561000
*R11	MEFM	9.9k	1/4W	0.5%	169606201
*R12	MEFM	990k	1/4W	0.5%	169606201
R14	CACP	100k	1W	10%	172551000
*R15	MEFM	16k	1/4W	0.5%	169606101
*R16	MEFM	16.9k	1/4W	0.5%	169606101
R18	MEFM	15k	1/8W	0.5%	192741502
R19	CACP	100k	1/8W	10%	172051000
R20	CACP	100k	1/8W	10%	172051000
R21	MEFM	5.1k	1/16W	1%	192635102
R22	MEFM	5.1k	1/16W	1%	192635102
R23	MEOX	2.2k	1/4W	5%	195632200
R24	MEOX	10k	1/4W	5%	195641000
R25	MEOX	2.2k	1/4W	5%	195632200
R26	MEOX	10k	1/4W	5%	195641000
R27	MEOX	47u	1/4w	5%	195624700
R28	MEOX	220	1/4W	5%	195622200
R29	MEFM	10k	1/8W	0.5%	192741002
R30	CACP	1000	1/8W	10%	172031000
R31	MEFM	27k	1/8W	0.5%	192742702
R32	MEOX	18k	1/4W	5%	195641800
R33	MEOX	18k	1/4W	5%	195641800
R34	MEOX	2.2k	1/4W	5%	195632200
R73	PRWW	9.975k	0.33W	0.1%	160300407
R74	PRWW	999	1/4W	0.1%	160300412
R75	PRWW	1Ω	1.5W	0.01%	169608702
C1	ESTF	.22	400V	20%	226152200
C2	ESTM	10	63V	20%	219971000
C3	ESTM	2.2	63V	20%	219962200
C4	ESTM	2.2	63V	20%	219962200
C5	ESTM	1.5	63V	20%	219961500
C6	CERM	33p	500V	20%	241313300
C7	CERM	100p	500V	20%	241321000
C8	CERM	100p	500V	20%	241321000
C9	CERM	3300p	2kV	+40% −20%	208450137
C10	ESTM	0.047	100V	10%	225444700
C11	CERM	0.047	25V	+50% -25%	241944700
C12	CERM	0.047	25V	+50% -25%	241944700
C13	CERM	0.047	25V	+50% −25%	241944700
D3 to D6	HP 5082-6221				300525380
D7	Zener	3.9V	.4W	5%	300521420
D8	Zener	3.9V	.4W	5%	300521420
D9	Zener	9.1V	.4W	5%	300521340
D10	SD3				300522160
D11	SD3				300522160
RV1	CMPM	100k	1/3W	10%	130651000
RV2	CMPM	1k	1/3W	10%	130631000
RV3	CMPM	500	1/3W	10%	130625000
RV5	CMPM	200	1/3W	10%	130622000
RV6	CMPM	50	1/3W	10%	130615000
RV9	CMPM	50	1/3W	10%	130615000
TR1	BCY 70				300553590
TR2	BC 107				300553320
TR3	BC 107				300553320
IC1	LM 310H				510090040
IC2	LM 301AH				510000620

*Absolute Match

Cct Ref.	General Description	Solartron Part No.
SA	Switch 5 wafer 2 Pole 5 way	379609205
RLB	Relay* 90	301201903

* Two Pole Change Over

Washer 8 BA Small	411000040
Vertical P.V. Socket	352501690
FS2 Fuse 1A Slo-Blo	360103080

PCB No. 3

Cct Ref.	General Description				Solartron Part No.
R1 to R5	CACP	1000	1/8W	10%	172031000
R7 to R11	CACP	390	1/8W	10%	172023900
R13 to R19	CACP	82	1/8W	10%	172018200
R20	CACP	100	1/8W	10%	172021000
R21 to R28	CACP	10k	1/8W	10%	172041000
R29	CACP	22	1/8W	10%	172012200
D1 to D5	5082 - 4494				300750080
TR1 to TR5	2N2906A				300554500
TR7 to TR12	BC 107				300553320
TR13 to TR19	2N2222A				300555410
TR20	BC107				300553320
IC1	LED MAN 73				300730340
IC2 to IC5	LED MAN 72				300730330
	14 PIN D.I.L. SOCKET				300584680
	POST				355500980
	TRANSISTOR PAD				300584220

MAIN ASSEMBLY

Cct Ref.	General Description	Solartron Part No.
T1	Mains Transformer	309606904
	Mains Lead	480140200
	Mains Lead Retainer	354003580
	Fuse Holder	360202000
	Fuse	360103040
	Rubber Boot	16000213
MSP1	Mains Selector Switch	375000500
	Input Terminal (Black)	355100360
	Input Terminal (Green)	355100370
	Input Terminal (Red)	355100380
	Guard Link	16200102

ACCESSORIES

Cct Ref.	General Description	Solartron Part No.
	Input Lead Assy (Red)	359900090
	Input Lead Assy (Black)	359900080
	Test Prod Black	351901030
	Test Prod Red	351901040
	Crocodile Clips (2)	355901030
	Polythene Bag	810000160
	Fuse 150mA	360103040
	Fuse 300mA	360103170

SECTION 6 -Specifications

This section contains a copy of the technical specification applicable to this instrument.

This instrument is designed and manufactured to a higher specification than is claimed commercially. In order that the user may benefit as appropriate, this technical manual may relate to a superior performance. In the event of contradictions between specifications, no additional claims are made for the instrument above that claimed in the current data sheet.

General

Display

Type:	7 Bar Red Light emitting diodes
Scale Length:	10.999 max.
Polarity Indication:	Displayed for negative dc inputs
Overload Indication:	DC/AC/μA/mA/flashing 1, Ω, kΩ steady 1
Annunciator:	mV, V, μA/mA, Ω, kΩ
Ranging:	Automatic, redundant leading zeros are blanked.

Environment

Working Temperature Range	0 to + 45^{O}C
Storage Temperature Range	−30 to +70^{O}C
Maximum Relative Humidity	70% at 40^{O}C

Power Supply

Voltage:	115V/230V + 10%−15%		
Frequency:	50Hz ± 1% or 60Hz ± 1%		
Consumption:	12VA		
Fuses:	230V	150mA	Slo Blo
	115V	300mA	Slo Blo

Size

Width:	216mm	(8.5in)
Height:	89mm	(3.5in)
Depth:	280mm	(11ins)
Weight:	2.73kg	(6 lbs)

Technical Specification

◇Manufacturing calibration temp. 23°C.
Specification valid for calibration at 20 to 25°C.
Temperature corrections need be applied only when operating beyond the temperature limits quoted under Limits of Error.

DC voltage (V DC)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Input Resistance
100mV	10μV	0.02	0.02	0.02	0.02	0.02	0.02	0.004	0.002	>1000MΩ
1V	100μV	0.01	0.01	0.02	0.01	0.02	0.01	0.004		>1000MΩ
10V	1mV	0.01	0.01	0.02	0.01	0.02	0.01	0.004		>1000MΩ
100V	10mV	0.02	0.01	0.03	0.01	0.03	0.01	0.007		10.1MΩ
1kV	100mV	0.05	0.01	0.05	0.01	0.05	0.01	0.007		10.1MΩ

Full Scale = Nominal Range + 10% (except 1kV range where f.s. = Nominal Range) Overload Immunity 1000V dc

AC Voltage (V AC)

Nominal Range	Input Sensitivity	Limits of Error◇ 40Hz to 20kHz□ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Input Impedance
100mV	10μV	0.1	0.08	0.15	0.1	0.15	0.1	0.006	0.004	1MΩ/100pF
1V	100μV	0.1	0.03	0.15	0.04	0.15	0.04	0.006		1MΩ/100pF
10V	1mV	0.2	0.06	0.2	0.06	0.2	0.06	0.015	0.004	1MΩ/100pF
100V	10mV	0.2	0.02	0.2	0.04	0.2	0.04	0.015		1MΩ/100pF
750V*	100mV	0.2	0.02	0.2	0.04	0.2	0.04	0.015		1MΩ/100pF

*500V max. above 1kHz

Full Scale = Nominal Range + 10% (except 750V where f.s. = Nominal Range) Overload Immunity 1100V pk

□**Typical limits for other frequency bands**
20Hz to 40Hz: ± 0.5% rdg ± 0.4% f.s.
20kHz to 50kHz: ± 0.5% rdg ± 0.4% f.s.
50kHz to 100kHz: ± 2.0% rdg ± 0.5% f.s.

Resistance (Ω)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Current thro' R
1kΩ	100mΩ	0.04	0.03	0.05	0.03	0.05	0.03	0.003	0.002	100μA
10kΩ	1Ω	0.04	0.01	0.05	0.01	0.05	0.01	0.003		100μA
100kΩ	10Ω	0.02	0.01	0.05	0.01	0.05	0.01	0.003		100μA
1MΩ	100Ω	0.04	0.01	0.05	0.01	0.05	0.01	0.005		1μA
10MΩ	1kΩ	0.1	0.02	0.15	0.02	0.15	0.02	0.005		1μA

Maximum dissipation in unknown: 1mW Full Scale = Nominal Range + 10% Overload Immunity 200V pk

DC current (μA/mA DC)

Nominal Range	Input Sensitivity	Limits of Error◇ 24 hrs ± 1°C ± [% rdg. + % f.s.]		6 mnths ± 5°C ± [% rdg. + % f.s.]		1 year ± 5°C ± [% rdg. + % f.s.]		Temp. coeff. per °C ± [% rdg. + % f.s.]		Input Resistance
10μA	1nA	0.04	0.03	0.05	0.03	0.05	0.03	0.005	0.002	< 5Ω
100μA	10nA	0.04	0.01	0.05	0.01	0.05	0.01	0.005		< 5Ω
1mA	100nA	0.04	0.01	0.05	0.01	0.05	0.01	0.005		< 5Ω
10mA	1μA	0.04	0.3	0.05	0.4	0.05	0.4	0.005	0.02	< 2Ω
100mA	10μA	0.04	0.04	0.05	0.05	0.05	0.05	0.005		< 2Ω
1A	100μA	0.04	0.05	0.05	0.05	0.05	0.05	0.005		< 2Ω

Full Scale = Nominal Range + 10% 7144 only: external current shunts for 10mA, 100mA & 1A ranges

Overload Immunity Ranges 1 to 3 10mA
Ranges 4 to 6 1.1A

Common Mode Rejection

Measured with an imbalance of 1kΩ in the input leads

Maximum Common Mode Voltage:	500V dc or peak ac	
DC Measurement:	Rejection of dc	>120dB
	Rejection of 50/60Hz ± 1%	>120dB
AC Measurement:	Rejection of dc	>120dB
	Rejection of 50/60Hz ± 1%	>40dB

Minimum input isolation resistance to earth	100MΩ
Maximum input capacitance to earth	1000pF

Series Mode Rejection

DC Measurement:	Rejection of 50/60Hz ± 1% >60dB

Figure quoted relates to peak interference and peak reading errors.

Accessories

Short linking	–		16200102
Test Probe	–	Red	351901040
Test Probe	–	Black	351901030
Crocodile Clip	–	(2 off)	355901030
Input Lead	–	(Red)	359900090
Input Lead	–	(Black)	359900080
Spare fuses		150mA	360103040
		300mA	360103170

Optional Accessories

Rack mounting kit	70501

Servicing

Servicing of the 7140 or 7144 should not be attempted without reference to the technical manual. Users unfamiliar with MOS components should not remove the instrument from its case.

Optional Servicing Accessories

Setting up case	70502
Board extender	70503
Servicing Manual	7140 0030

APPENDIX

This section contains specialised selection procedures and/or test equipment to facilitate servicing.

CONTENTS

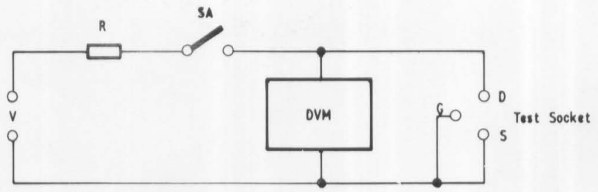
FET SELECTION PROCEDURE

PURPOSE

To select four FET's type U1899E with R_{on} matched to within 1Ω at a drain-source current of 100μA.

TEST PROCEDURE

The following test procedure should be carried out using the test circuit shown below or Solartron Test Equipment TG1100/1.



TEST CIRCUIT

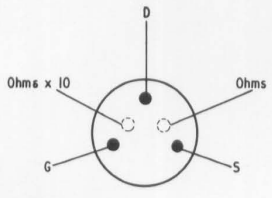
$$\left.\begin{array}{l} V = 10V \\ R = 100k \end{array}\right\} \quad \frac{V}{R} = 100\mu A \pm 0.2\%$$

(a) Devices to be tested should be allowed to settle to the ambient temperature of the chamber in which the matching operation is to be done.
This temperature should be $23^{o}C \pm 1^{o}C$.

(b) Place the device under test in the test socket using tweezers or pliers to ensure that its temperature is not raised by handling.

(c) Press switch SA and note DVM reading.
Use the relation 1mV = 10Ω to calculate the R_{on} value.

(d) Mark the top of the device with two coloured dots of paint as shown in following view employing the standard colour code.
R_{on} to be given to nearest whole number, e.g.



TOP VIEW

45.6Ω	YELLOW-BLUE
46.3Ω	YELLOW-BLUE
46.5Ω	YELLOW-VIOLET

(e) Select sets of four devices, each with the same colour code.

COLOUR CODE

0	Black
1	Brown
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Grey
9	White

SETTING-UP CASE 70502

INTRODUCTION

In order to achieve the greatest accuracy during a calibration it is essential that the operating temperatures affecting circuit components are as near as possible to those experienced within the instrument case during normal operation.

The Setting-Up Case 70502 enhances the calibration accuracy by allowing access for adjustments whilst the instrument is functioning under normal working conditions.

GENERAL DESCRIPTION

The Setting-Up Case is basically a normal instrument case with holes drilled in convenient positions allowing access to the potentiometers. Fig. A1 shows the side view of the Case with the access holes and the relevant potentiometers.

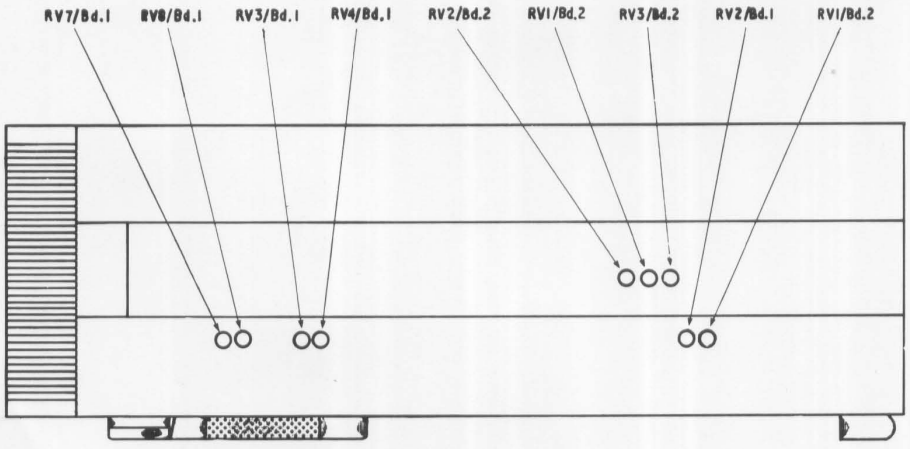
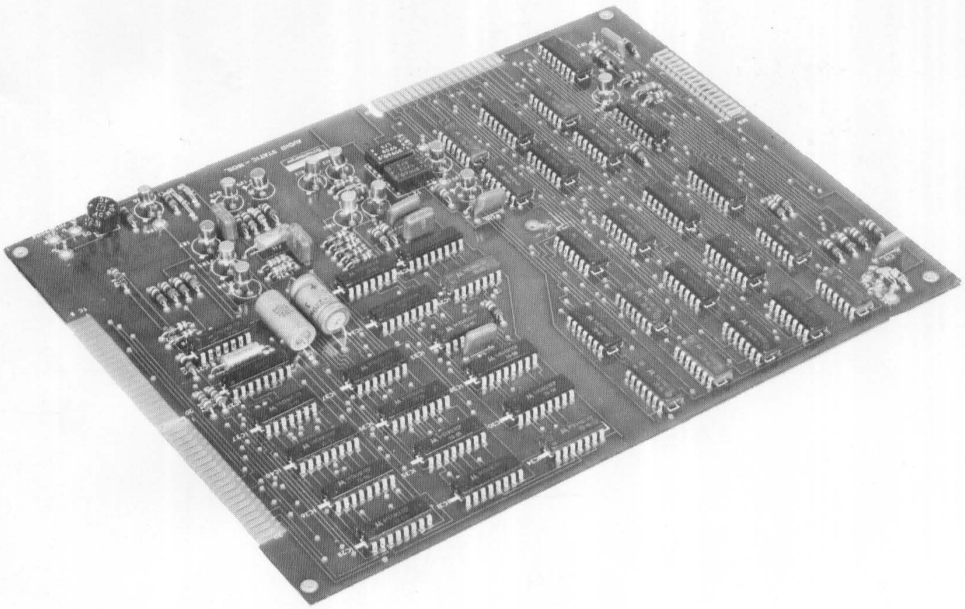


Fig. A.1. View of Setting-Up Case showing potentiometer access holes.

PART 3 BCD OUTPUT MODULE FOR 7054/7144

PART 3

BCD OUTPUT MODULE FOR 7054/7144



Part No. 70540030

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TECHNICAL MANUAL

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CONTENTS

SECTION 1 General

INTRODUCTION

The 7054/7144 BCD Output Module is used on the 7054 and 7144 DMM, the difference in their scale lengths being catered for by a set of links on the Module pcb. A common pcb is used for both types of instrument, Solartron Part Number 70509004.

The BCD Output Module provides an isolated parallel BCD output from the 7054/7144 DMM, consisting of the magnitude, and the range (in BCD code). The DMM mode is manually selected and is therefore not programmable.

The BCD Output Module operates in the normal sample/print command closed loop mode, generally associated with a system incorporating a Recorder (Teleprinter, Typewriter, etc.) and its Drive Unit, or similar devices which provide the necessary TTL compatible input/output. The following equipment is recommended for use with the 7054/7144 DMM.

SOLARTRON A290 RECORDER DRIVE UNIT

Provides a simple recording system, the RDU controlling the DMM and driving the desired recording device.

SOLARTRON A226 PROGRAMMER

Provides the facilities of a 10 channel scanning system with high and low limit detection. Can also be supplemented by the A290 RDU.

The Module provides complete isolation between the DMM and the peripheral, and removal of the BCD Output Module from the DMM has no significant affect on the latter's performance.

Fig. 1.1 shows the physical location of the BCD Output Module on the 7144 DMM.

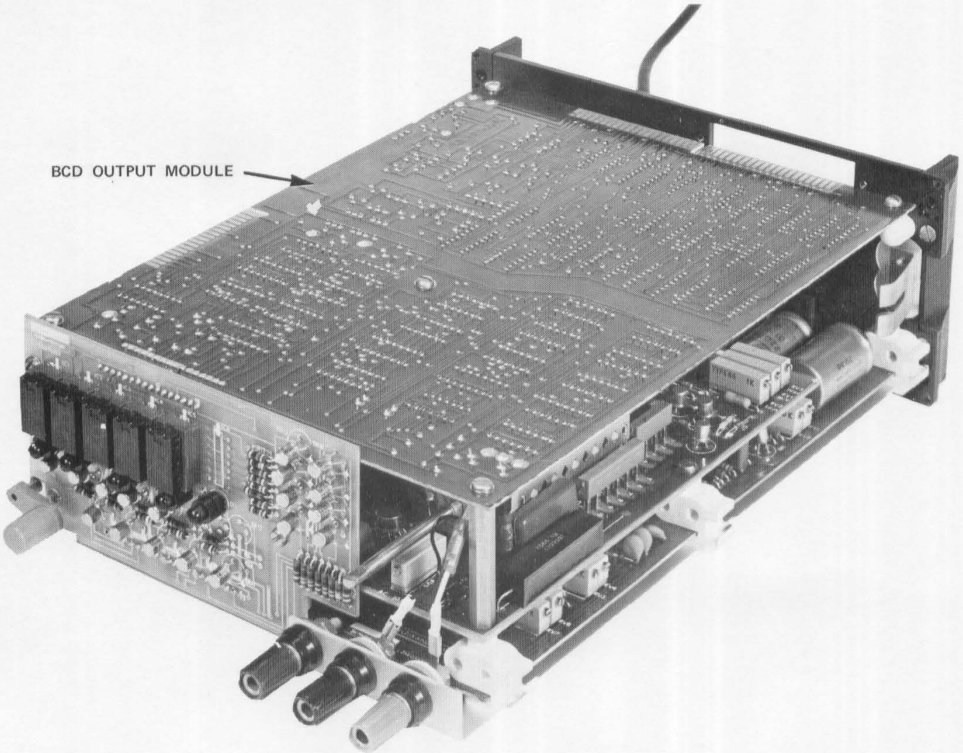


Fig. 1.1 View of the 7144 DMM with case removed.

SECTION 2 Operation

This section provides all the necessary instructions concerning preliminary checks and operating procedures required when the BCD Output Module is to be used.

PRELIMINARY CHECKS

Before using the instrument the following checks are necessary:-

CAUTION:- IT IS ESSENTIAL THAT THE INSTRUMENT BE ISOLATED FROM THE MAINS SUPPLY BEFORE OUTER CASE REMOVAL, DUE TO UNCOVERED TERMINALS ON THE ON/OFF SWITCH.

BEWARE OF GUARD POTENTIAL ON GUARD PLATE WITH INSTRUMENT CASE REMOVED.

(a) Remove the DMM case and check that the BCD Output Module is correctly linked for the type of DMM used. Fig. 2.1 shows the location of the links and the floating section power connections.

LINK 1 :- For 7054

LINK 2 :- For 7144

(b) Check for correct earth connections.

NOTE:- The 0V(E) for the BCD output is normally connected internally by a wire to the 7054/7144 mains earth. If a mains earth is not used on the 7054/7144, or if the wire has been removed, the 0V(E) connection may be made at the peripheral end to avoid an earth loop.

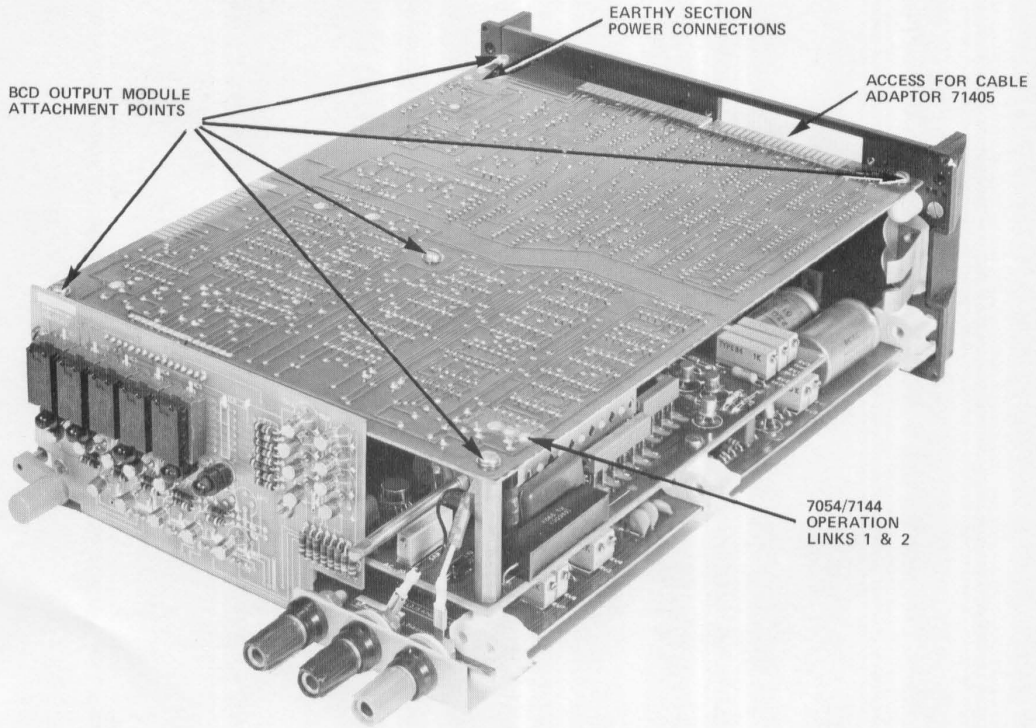


Fig. 2.1 View of 7144 showing location of the Operation Links 1 & 2 and the Earthy Section power supply connections.

(c) Refit the DMM case and connect the system using a suitable cable. This may be a cable made by the customer to suit the system being used or, if the system has been developed for use with the Solartron Master Series DVM, either of the following Cable Adaptors can be used.

70505 Cable Adaptor for the 7054 DMM

71405 Cable Adaptor for the 7144 DMM

See Diagram 13 for details of cable socket interconnections on the Cable Adaptors.

OPERATION

The operation of the BCD Output Module is dependent on the operation of the DMM (see relevant section of the manual), and on the operation of the peripheral and its interface. For those, reference to their Operating Manuals will be required.

The recording rate of the system is governed by the slowest unit and, should the peripheral interface be run at a rate exceeding the BCD Output Module capabilities, updating will cease. See Section 6 for relative pulse widths and rates.

SECTION 3 Servicing

This section provides detailed servicing information for the BCD Output Module.

INTRODUCTION

The Servicing Section is based on the functional block system of circuit diagrams, whereby components are grouped together to form a functional entity.

The BCD Output Module is divided into two main functional blocks as shown in Fig. 3.1.

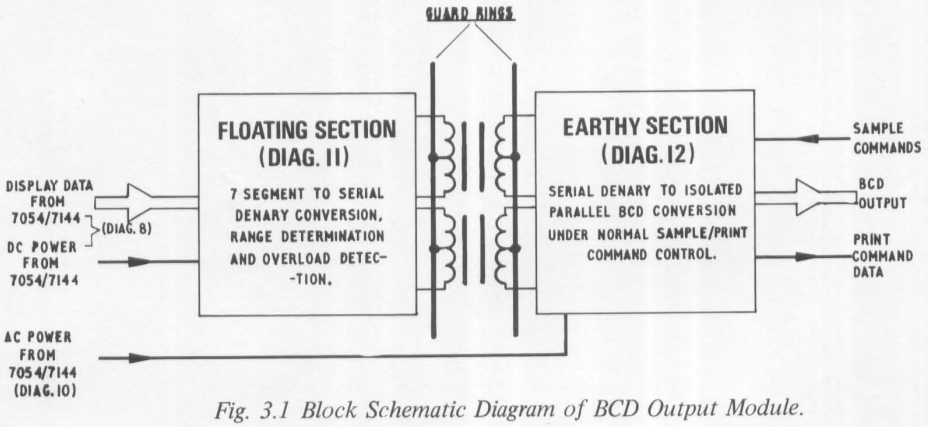


Fig. 3.1 Block Schematic Diagram of BCD Output Module.

Diagrams 11 and 12 are the two block circuit diagrams of the BCD Output Module circuit. Diagrams 1 to 10 can be found in the DMM manual.

Information regarding circuit descriptions, component locations, printed circuit board layouts, and any specific cautionary notes concerning components or testing procedures are arranged to be fully visible with the appropriate circuit diagram.

PRESENTATION OF INFORMATION

The block circuit diagrams are arranged to fold out clear to the right, with a functional description of each on the left hand text pages. The pcb layout diagram is arranged to fold out clear to the left, allowing cross reference between diagram and component location.

The functional signal flow is conventional, from left to right, with feedback lines from right to left. These rules, although generally followed, are not rigidly adhered to, due to the intricacies associated with logic circuitry. Arrows are extensively employed to indicate the direction of the logic flow.

The type of CLOCK (CK), SET (S) and RESET (R) pulses required for the less common logic devices employed are identified before each circuit description is attempted. See also Basic Logic Elements (SECTION 3).

COMPONENT LOCATION

Each circuit diagram and printed circuit board diagram are so arranged that they can be viewed together, thus aiding the identification and location of each component.

POWER RAIL NOTATION

The power rails are shown as short detatched bars with the nominal voltage annotated. All bars annotated with the same voltage are electrically connected together and correspond to the appropriate rail annotation on their respective power supplies.

The 0V rail of the 'floating section' (DIAGRAM 11) is connected to 0V on pcb 1 of the 7054/7144 DMM. The 0V (E) rail of the 'earthy section' is normally earthed at the 7054/7144 mains power supply earth but can, if required, use the peripheral earth.

It must be remembered that the voltages shown are approximate, being proportional to the load taken through the appropriate decoupling resistors. A voltage reading which is inconsistant with the value given on the diagram should not, therefore, be taken as a symptom of unserviceability without reference to other indications.

ELECTRICAL CONNECTIONS

The input to the BCD Output Module is by a 20 way Berg pin plug/socket connection and the output connector used is a 40 way BICC Burndy connector.

Transformer connections to the 'earthy section' power supply are by disconnect pins.

Connection between the floating section and the 'earthy section' is by transformer coupling, complete with guard ring protection.

Link Pins

One set of link pins render the BCD Output Module suitable for the 7054 and the 7144 DMM, identified by DMM type number.

Spare ICs

Unused ICs have their inputs connected to one of the voltage rails.

WARNING

CMOS Integrated Circuits are used on this pcb.

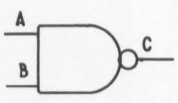
It is therefore advisable to take every precaution to reduce the risk of their damage by static charges.

BASIC LOGIC ELEMENTS

Positive logic is employed in the BCD Output Module, and the following devices are used extensively. Their logical functions are explained in the accompanying truth tables where:-

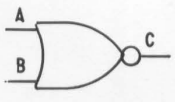
1 = Hi = Bit present

0 = Lo = Bit absent



NAND Gate

A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

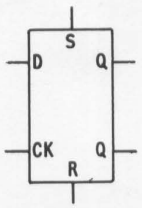


NOR Gate

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

Exclusive - OR Gate

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0



D Type Flip-Flop

INPUTS				OUTPUTS	
CLOCK	DATA	SET	RESET	Q	$\overline{Q}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
¬	X	0	0	Q	$\overline{Q}$ *
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	INV	INV

⌐ = Level Change X= 1 or 0

* = No Change INV=Invalid

SALIENT FEATURES OF PCB

The various important features of the 7054/7144 BCD Output Module are identified in Fig. 3.2. Plug PLC is a 40 way, double sided edge connector and, in order to ensure correct orientation with the 70505/71405 Cable Adaptor socket, a slotted keyway has been incorporated.

NOTE:- Test Edge Connectors A and B are used during production testing in the factory but may be used when fault finding.

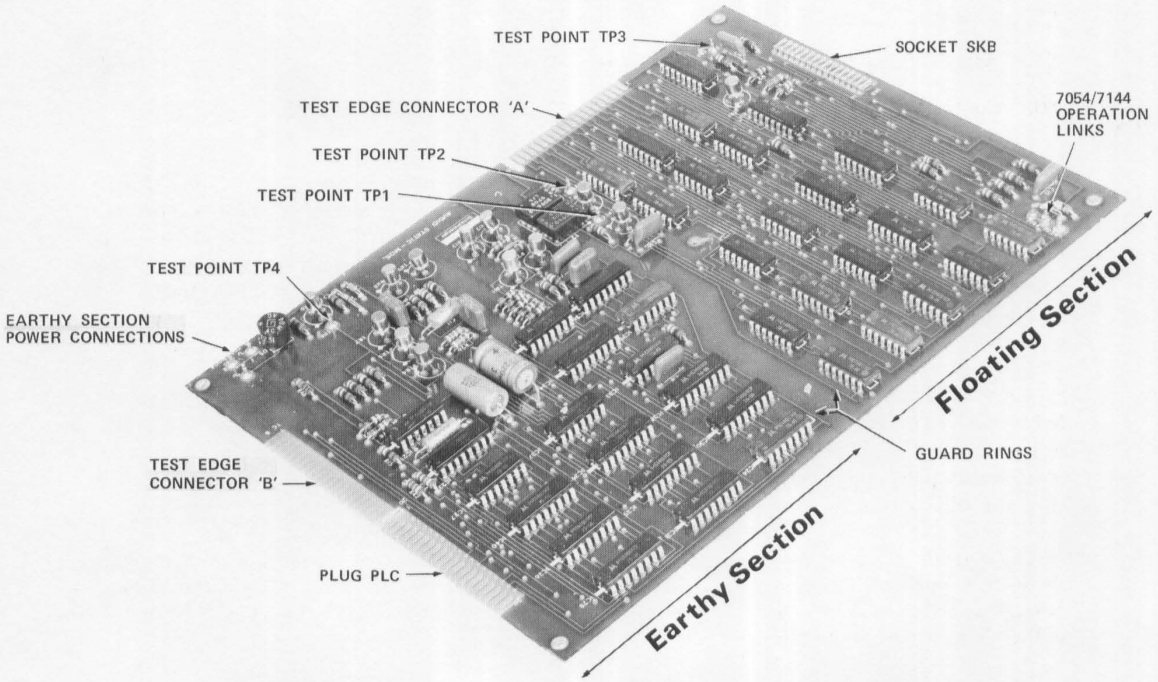


Fig. 3.2 Salient Features of the BCD Output Module.

FUNCTIONAL DESCRIPTION (FIG. 3.3)

Four parameters from the 7054/7144 DMM are used to control the operation of the BCD Output Module. They are:-

Drift Correct Pulse.
Clock Pulse.
First Decade Character Drive (A1).
Second Decade Character Drive (A2).

} See Diagram 8 of DMM (PLB)

The conversion of the 7 segment display data into the isolated parallel BCD output is achieved in two stages, being converted into serial denary first. For this only five of the 7 segment drives are required, with the decimal point drive line needed to determine the range.

The earliest time the BCD Output Module can use new data in any given measurement sequence is decided by the 'display load' command, internally generated in IC7 pcb 1 of the DMM. This waveform is inaccessible, and the substitute used is the DRIFT CORRECT pulse leading edge with a 40 CLOCK pulse initiated delay added. The data conversion into serial denary commences on the arrival of the first A1 pulse after the 40 pulse count. A five state Control Counter controls this and other operations of the Module. The five states are:-

S0:- Control Counter reset

S1:- Allocation of New Data Aquisition (DRIFT CORRECT period starts)

S2:- Calculation of Acquisition Start Time (40 CLOCK pulses after S1)

S3:- New Data Conversion to serial denary (First A1 pulse after S2)

S4:- Range Determination (Second A1 pulse after S2)

S0:- Control Counter reset (Third A1 pulse after S2 followed by the end of DRIFT CORRECT pulse)

During state S3, the five segment drive lines are compared with five outputs of a decade counter driven BCD - 7 segment decoder. The decade counter is arranged to count up to 10 for every drive period, being driven by CLOCK ÷ 2 pulses. A comparator detects when parity exists between the two sets of outputs and latches the decade counter clock, thus producing a 7 segment to serial denary conversion, e.g. a 7 segment input of 3 produces three output clock pulses during that decade drive period. At the end of each decade drive period an END OF DECADE pulse is generated.

The serial denary pulses, produced during states 3 and 4, and the END OF DECADE pulses are fed to the 'earthy section' via two transformers. The END OF DECADE pulses clock an 8 bit shift register which, if a sample has been called for, selects in turn each of seven counters and steers the serial denary pulses to be counted, starting with the most significant decade, A1. The BCD counters store the BCD output information until the next sample is called for.

The seventh counter is used to store the BCD range number. This is not determined until state S4 of the Control Counter sequence. The range number is derived from the position of the decimal point, this being further modified by the instrument mode and the setting of the 7054/7144 link in the 'floating section' of the pcb.

An overload condition is identified by detecting a '1' during the A1 drive period followed by a blank A2 drive period (Decade drives A2 to A6 are blanked by the LS1 MOS integrated circuit on DMM pcb 1). The BCD output depicting an overload condition is decimals ± 110000 for the 7054 and ± 11000 for the 7144.

State S4 ends with the arrival of the third A1 pulse, this resets the Control Counter to state S0 and in doing so initiates all the other required resets. When the DRIFT CORRECT pulse ends, the positive going edge is used as a check reset of the Control Counter.

All BCD outputs are buffered to maintain TTL compatibility.

The normal sample/print command closed loop system is used as defined in the specification Section (SECTION 6).

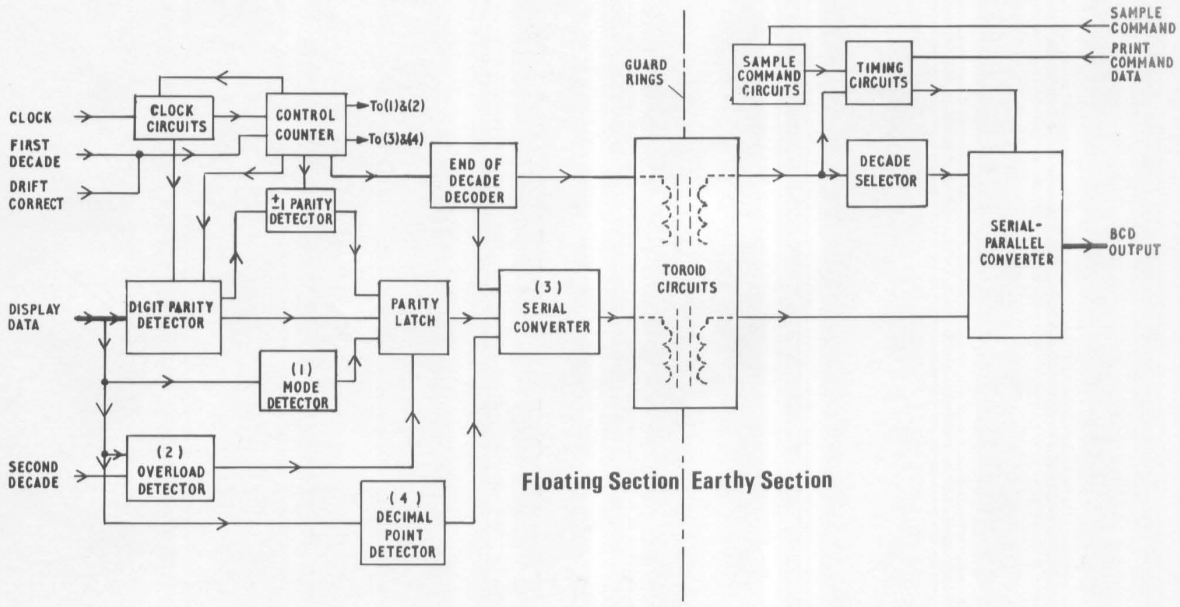


Fig. 3.3 Functional Block Schematic Diagram of BCD Output Module.

TEST WAVEFORMS

Four test points, TPs 1 to 4, are incorporated on the pcb, providing the following facilities.

TP1:- For examination of the END OF DECADE pulses.

TP2:- For examination of the DENARY pulses.

TP3:- Useful where synchronisation with the DMM Clock is required.

TP4:- Provides a monitoring point for the +5V supply voltage.

An example of a typical CLOCK waveform is shown in the DMM Technical Manual, identified under Frame 3B - 5.

The following test waveforms illustrate the output from the Serial Converter and the End of Decade Decoder during Control Counter states 3 (Decades A1 to A6 on illustration) and 4 (Range Number on illustration) on a 7054 DMM.

NOTE:- The Serial Converter pulses during Range Number determination can be entirely CLOCK ÷ 20 pulses or CLOCK ÷ 2 and CLOCK ÷ 20 pulses, dependent on the DMM measurement mode.

FRAME 3 - 1

UPPER TRACE

This is taken from TP2, oscilloscope settings

Time/cm = 200μs

Volts/cm = 5V

The serial denary pulses are clearly seen and when counted from the left, give:-

Decades	Pulses	BCD Output	Readout
A1:-	1 (CK ÷ 2)	–VE sign	–
A2:-	1 (CK ÷ 2)	001	1
A3:-	2 (CK ÷ 2)	010	2
A4:-	3 (CK ÷ 2)	011	3
A5:-	4 (CK ÷ 2)	100	4
A6:-	5 (CK ÷ 2)	101	5
Range Number:-	4 (CK ÷ 20)	100	4

Mode is '**V.DC**'

Interpretation of Module output = INTEGRATOR OUTPUT x 10^{-n}V where n = Range Number

= -12345×10^{-4}V

= –1.2345V

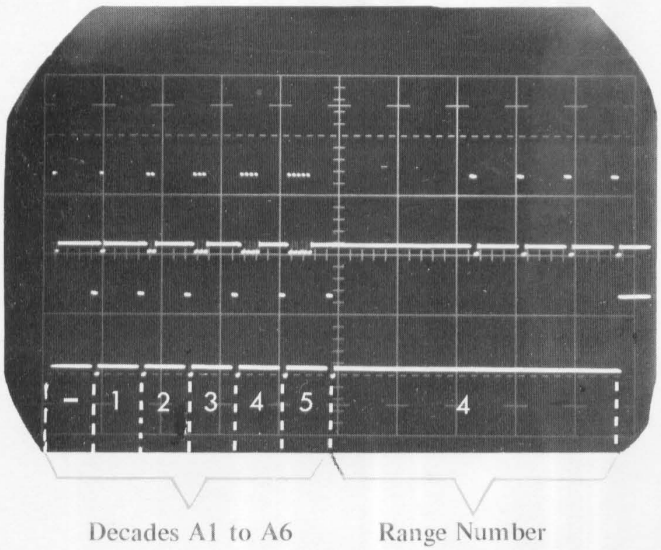
LOWER TRACE

This is taken from TP1, oscilloscope settings

Time/cm = 200μs

Volts/cm = 5V

The END OF DECADE pulses are clearly seen, including the effect on test point TP1 as the Control Counter reverts to state S0.



Frame 3.1

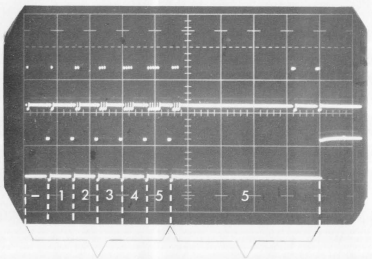
FRAME 3 - 2

It can be seen that the serial denary pulse count during Control Counter state S3 (Decades A1 to A6 on the illustration) are identical to those of Frame 3 - 1. The Range Number, however, differs in that the Mode Detector has introduced the three extra CLOCK ÷ 2 pulses which, when added to the two CLOCK ÷ 20 pulses, give a Range Number of 5.

i.e. Interpretation of Module output = -12345×10^{-5} V (Mode is '**V.DC**')
= $-.12345$V
= -123.45mV

The oscilloscope settings are the same as Frame 3 - 1.

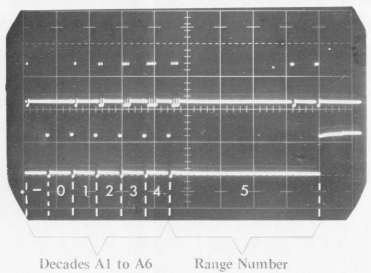
The remaining frames, at the same oscilloscope settings as Frame 3 - 1, illustrate the following Module output interpretations.



Frame 3.2

FRAME 3 - 3

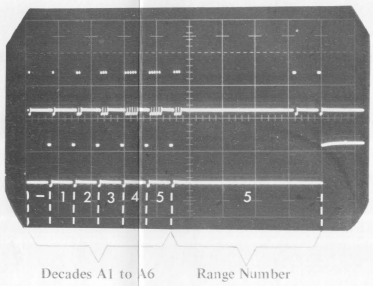
Interpretation of Module output = -01234×10^{-5} V (Mode is '**V.DC**')
= $-.01234$V



Frame 3.3

FRAME 3 - 4

Interpretation of Module output = 12345×10^{-5} mA (Mode is '**μA.DC**')
= $-.12345$mA

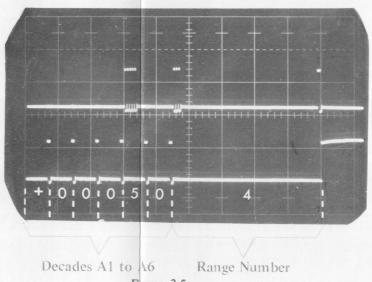


Frame 3.4

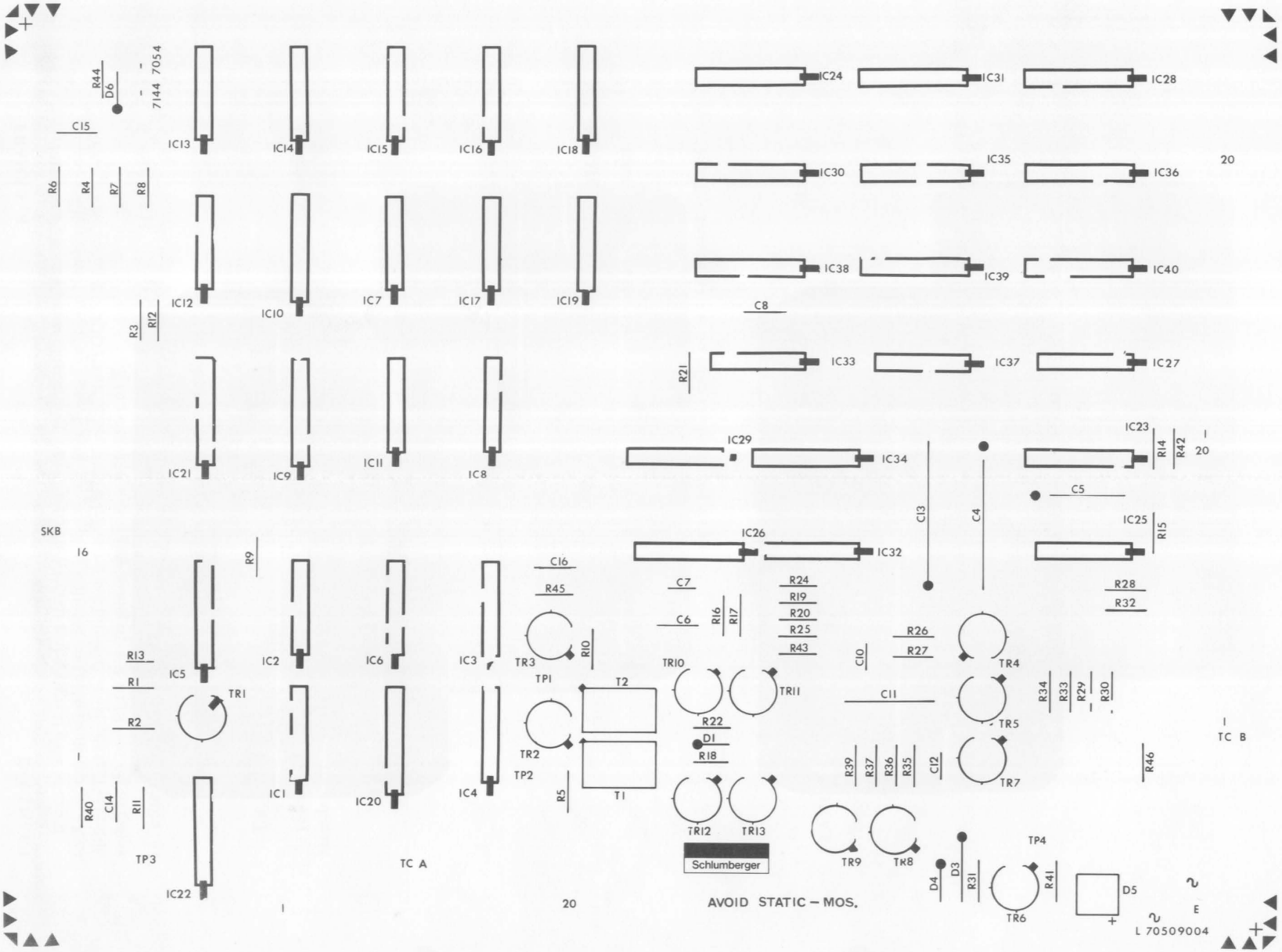
FRAME 3 - 5

Interpretation of Module output = $+00050 \times 10^{-4}$ kΩ (Mode is Ω)
= $+0.0050$kΩ

NOTE:- Decade A1 has no pulse i.e. indicating + sign.



Frame 3.5


R44
D6
7144 7054
C15
IC13
IC14
IC15
IC16
IC18
R6
R4
R7
R8
IC12
IC10
IC7
IC17
IC19
R3
RI2
IC21
IC9
IC11
IC8
SKB
16
R9
IC5
TR1
RI3
RI
R2
IC2
IC6
IC3
C16
R45
TR3
RI0
TP1
T2
TR2
TP2
T1
R5
IC1
IC20
IC4
R40
C14
RI1
TP3
IC22
TC A
20
AVOID STATIC – MOS.
Schlumberger
IC24
IC31
IC28
IC30
IC35
IC36
20
IC38
IC39
IC40
C8
R21
IC33
IC37
IC27
IC29
IC34
IC23
R14
R42
20
C5
IC26
IC32
C13
C4
IC25
R15
C7
C6
RI6
RI7
R24
RI9
R20
R25
R43
R28
R32
TRI0
TRI1
R22
D1
RI8
TRI2
TRI3
C10
R26
R27
TR4
C11
TR5
R34
R33
R29
R30
TC B
R39
R37
R36
R35
C12
TR7
R46
TR9
TR8
D4
D3
R31
TP4
TR6
R41
D5
E
L 70509004

FRAME 3 - 6

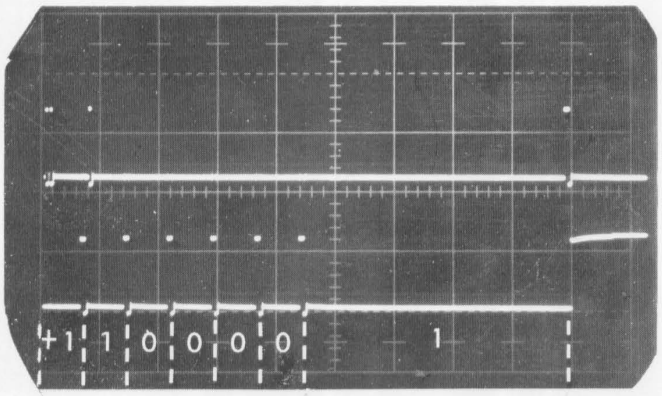
This is the OVERLOAD indication when the instrument is in the Ω mode.

OVERLOAD INDICATIONS

The following OVERLOAD indications exist for the modes and instrument type stated:-

MODE	7054	7144
V.AC/V.DC	± 110000 2	± 11000 1
Ω	+ 110000 1	+ 11000 0
μA.DC	± 110000 2	± 11000 1

the last digit being the Range Number.



Decades A1 to A6 Range Number

Frame 3.6

← *Fig. 3.4 PCB COMPONENT AND COPPER TRACK LAYOUT.*

SUB-SECTION 3a-Floating Section

This sub-section deals with the conversion of the 7 Segment Display data from the DMM into Serial Denary pulses for further transformation into BCD in the 'earthy section' (SUB-SECTION 3b).

FUNCTIONAL DESCRIPTION (DIAGRAM 11)

SEQUENCE CONTROL

The Control Counter is switched through it's various states by the DRIFT CORRECT, 1st DECADE (A1) and CLOCK ÷ 20 pulses. Whilst in it's various states, the Control Counter enables selected gates in other functional blocks, and applies the necessary SETS and RESETS throughout the circuit.

The Clock Divider produces the CLOCK ÷ 2 and CLOCK ÷ 20 pulses during all Control Counter states except S2 (the wait period between the end of the 40 pulse count and the arrival of the following A1 pulse). The CLOCK ÷ 2 pulse is used as the gating pulse for the serial denary pulses. The CLOCK ÷ 20 pulse is used to produce the END OF DECADE pulse, and is also used as the 'counting pulse' for Decimal Point detection.

CIRCUIT ACTION

It is assumed that the Control Counter sequence is in state S0.

State S0:- All circuit RESETS are applied and the CLOCK pulses are inhibited in the Clock Divider. The DRIFT CORRECT period starts and the –ve going edge of it's waveform switches the Control Counter to state S1.

State S1:- The RESETS are removed from the two decade counters and the Clock Divider is enabled, allowing CLOCK pulses to be counted. A pulse is generated by the End of Decade Decoder to initiate the serialise delay in the Timing Circuits (DIAG. 12). Both Parity Detectors operate continuously during the decade counter's counting periods but their outputs to the Parity Latch are disabled by the Control Counter, thus no pulses are allowed through the Serial Converter. After 40 CLOCK pulses have been counted through the Clock Divider, the Control Counter goes to state S2.

State S2:- The Clock Divider is disabled, producing no output pulses. The Parity Latch is still disabled. The first A1 pulse arrives, taking Control Counter to state S3.

State S3:- The following circuits are enabled for one complete cycle of display multiplexing, to allow determination of digit and overload information:-

± 1 Parity Detector
Digit Parity Detector
End of Decade Decoder
Serial Converter
Overload Detector

While decade A1 bar data are applied, CLOCK pulses are gated through the Serial Converter until parity is detected by the ± 1 Parity Detector. The Parity Latch is then operated, disabling the Serial Converter. Also during the A1 data application, the Overload Detector is searching for a possible overload condition, i.e. the presence of a '1'. At the end of decade A1, the End of Decade Decoder produces the END OF DECADE pulse and also generates the Parity Latch RESET pulse. Decade A2 bar data are then applied and CLOCK pulses gated through the Serial Converter until parity is detected by the Digit Parity Detector, when the Parity Latch will again be operated,

disabling the Serial Converter. Simultaneonsly, the Overload Detector analyses A2 and, should A2 be fully blanked, it will operate the Parity Latch using the SET input. Otherwise, the Overload Detector holds off this SET action. Again an END OF DECADE pulse is generated along with the Parity Latch RESET pulse. Decades A3 to A6 receive similar treatment from the Digit Parity Detector and Parity Latch.
When the next A1 pulse arrives, the Control Counter goes to state S4.

State S4:- The following circuits are disabled, allowing determination of range information only:-

± 1 Parity Detector
Digit Parity Detector
End of Decade Decoder
Overload Detector

The RESET is removed from the Decimal Point Detector, and the Mode Detector is enabled. Decade A1 bar data are searched for the presence of either modes Ω, **mV** or **μA**. If one of those modes is present, the operation of the Parity Latch is delayed by 3 decade counter (Clock Divider) counting pulses, which are counted through. Decades A2 to A6 are then searched by the Decimal Point Detector until the decimal point is found, after which CLOCK ÷ 20 pulses (one for each decade after decimal point detection) are gated through the Serial Converter.
i.e. Pulses counted during state S4 consist of:-

For modes Ω, **mV** or **μA**:-

3 serial denary pulses and 1 CLOCK ÷ 20 pulse per decade after the decimal point detection.

All other modes:-

1 CLOCK ÷ 20 pulse per decade after decimal point detection.

NOTE:- In the case of the 7144 Module, the Decimal Point Detector is arranged to delay the gating of the CLOCK ÷ 20 pulses after decimal point detection, causing the loss of one CLOCK ÷ 20 pulse. This is to compensate for the difference in scale lengths between the 7054 and 7144.

When the next (third) A1 pulse arrives the Control Counter goes to state S0, applying all the RESETS.

State S0:- All circuits are reset, and when the DRIFT CORRECT period ends, the +ve going edge of it's waveform is used to carry out a 'check reset' on the Control Counter.

The circuit descriptions of the individual functional blocks in the 'floating section' follow.

CONTROL COUNTER

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

ICs 16, 17 and 19/1-5:- (a) Produce the required logic levels at points S0 to S4 in the correct sequence, thus controlling the operation of the various functional blocks in the circuit.

(b) Control the reset of (a) Decade counters, IC10.
(b) Decimal Point Detector, IC13 (b).
(c) Parity Latch, IC4 (a).

IC7/11-13:- Activates decade counter reset during Control Counter states S0 and S2.

C15/R44/D6 differentiate the +ve going edge when the DRIFT CORRECT period ends, providing a 'check reset' pulse.

IC13(a):- Produces CLOCK ÷ 40 pulses at $\overline{Q}$ output.

ICs 14 (3 gates) & IC15:- Control the switching sequence of ICs 16 and 17 as shown in Tables 3a.1 and 3a.2, with IC15/9 providing the common clock input.

IC 14 PIN NUMBERS									IC 15 PIN 9	CIRCUIT SEQUENCE
8	9	10	12	13	11	5	6	4		
0	1	1	1	0	1	0	0	1	0	State S0 assumed.
0	1	1	1	1	0	0	0	1	1	DRIFT CORRECT period starts (–ve going edge).
1	1	0	0	1	1	0	0	1	1	Counter goes to state S1. The 40 CLOCK pulse count starts.
1	0	1	0	1	1	0	0	1	0	After 20 CLOCK pulses.
1	1	0	0	1	1	0	0	1	1	40 CLOCK pulse count completed.
0	1	1	0	1	1	1	0	1	0	Counter goes to state S2, waiting on the first decade A1 pulse.
0	1	1	0	1	1	1	1	0	1	First decade A1 pulse arrived.
0	1	1	0	1	1	1	1	0	1	Counter goes to state S3, data conversion starts with A1.
0	1	1	0	1	1	1	0	1	0	Decades A2 to A6 are processed.
0	1	1	0	1	1	1	1	0	1	Second decade A1 pulse arrives.
0	1	1	0	1	1	1	1	0	1	Counter goes to state S4. Range determination starts.
0	1	1	0	1	1	1	0	1	0	Second decades A2 to A6 are scanned for decimal point.
0	1	1	0	1	1	1	1	0	1	Third decade A1 pulse arrives.
0	1	1	1	1	0	0	0	1	1	Counter reverts to state S0, resets activated.
0	1	1	1	0	1	0	0	1	0	DRIFT CORRECT pulse ends, providing 'check reset' pulse.

Table 3a.1

COUNTER STATE	OPERATING FUNCTION	IC16		IC17		IC19
		Q.1	Q.13	Q.1	Q.13	1
S0	END OF DRIFT CORRECT (VIA C15)	1	0	0	0	0
S1	START OF DRIFT CORRECT	0	1	0	0	0
S2	STATE S1 + 40 CLOCK PULSES	0	0	1	0	0
S3	FIRST A1 PULSE AFTER S2	0	0	0	1	0
S4	SECOND A1 PULSE AFTER S2	0	0	0	0	1
S0	THIRD A1 PULSE AFTER S2	1	0	0	0	0

Table 3a.2

Table 3.2 shows the states of the Q outputs of ICs 16, 17 and the output of IC19 as the sequence detailed in Table 3.1 occurs.

CLOCK DIVIDER

DECADE COUNTER LOGIC

CLOCK	INHIBIT	RESET	ACTION
⌐	0	0	INCREMENT COUNTER
⌐	1	0	COUNTER INHIBITED
X	X	1	ALL OUTPUTS GO TO 0

⌐ = Level Change X = 1 or 0

CIRCUIT DESCRIPTION

IC1 :- Gates the CLOCK pulses.

IC4(b) :- Produces CLOCK ÷ 2 pulses.

IC10(a) :- Performs two functions:-

(a) Produces the BCD output to feed the BCD to 7 segment decoder, IC9.

(b) Together with IC4(b) and IC14/1-3 produces a CLOCK ÷ 20 trigger pulse for IC13(a) and the End of Decade Decoder.

END OF DECADE DECODER

IC8/8-10 :- Gates the CLOCK ÷ 20 pulses during state S3 i.e. 1 pulse per decade scanned.

IC8/11-13 :- 1. Gates the END OF DECADE pulses received from IC8/10.

2. Is enabled by the arrival of DRIFT CORRECT and this action produces the trigger pulse for the serialising delay monostable, IC26(b), (DIAGRAM 12).

± 1 PARITY DETECTOR

DECADE COUNTER LOGIC

CLOCK	INHIBIT	RESET	ACTION
⌐	0	0	INCREMENT COUNTER
⌐	1	0	COUNTER INHIBITED
X	X	1	ALL OUTPUTS GO TO 0

⌐ = Level Change X = 1 or 0

PARITY DETECTOR LOGIC

FIRST DECADE DISPLAY	DECADE COUNTER OUTPUT			NUMBER OF PULSES COUNTED
	A	B	C	
+VE (Blank)	0	0	0	0
−VE (BAR 'g')	1	0	0	1
+1 (BARs 'b' & 'c')	0	1	0	2
−1 (BARs 'b', 'c' & 'g')	1	1	0	3
———	0	0	1	INHIBITED

CIRCUIT DESCRIPTION

IC10(b) :- Counter is subjected to the normal decade count cycle but is self-inhibited on the 4th pulse.

IC2/10-13 :- Gate fully enabled when parity exists during the 1st Decade scan under Control Counter state S3.

IC11 & IC19:- These are the logic gates for the 1st Decade parity detection, with IC19 gating IC2/10-13, resulting in the denary pulse output as stated in the Parity Detector Logic table.

DIGIT PARITY – DETECTOR

BCD - 7 SEGMENT DECODER LOGIC

BCD INPUTS				7-SEGMENT OUTPUTS (5of)					DECIMAL NUMBER
D	C	B	A	a	b	f	g	e	
0	0	0	0	1	1	1	0	1	0
0	0	0	1	0	1	0	0	0	1
0	0	1	0	1	1	0	0	1	2
0	0	1	1	1	1	0	1	0	3
0	1	0	0	0	1	1	1	0	4
0	1	0	1	1	0	1	1	0	5
0	1	1	0	0	0	1	1	1	6
0	1	1	1	1	1	0	0	0	7
1	0	0	0	0	1	1	1	1	8
1	0	0	1	1	1	0	1	1	9

CIRCUIT DESCRIPTION

IC9 :- Decodes each BCD output from IC10(a) but parity is only effected on Decades A2 to A6.

IC15 & IC7 :- Included logic to compensate for the different decimal six presentation i.e.

Input from DMM uses top segment 'a' while decoder, IC9, does not.

IC11 & IC12:- Detect parity between 'BAR' Inputs and decoder, IC9 output.

IC5 :- Performs the AND function on

(a) Parity detectors ICs 11 & 12
(b) $\overline{\text{CLOCK}}$ and CLOCK ÷ 2 pulses
(c) $\overline{\text{A1}}$ (i.e. Decades A2 to A6)

IC1 :- Gates the parity signal from IC5/14 during state S3 only.

PARITY LATCH

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC2 :- Gates:- (a) the parity signal from IC2/10 or
(b) the parity signal from IC1/4 or
(c) the Mode Detector signal

IC8 :- In conjunction with C14/R40 produces a reset pulse for IC4(a):-

1) Before Control Counter state S3 is selected
2) During state S3, on each END OF DECADE pulse.

IC4(a) :- The parity latch, activated as follows

On RESET:- $\overline{\text{Q}}$ is Hi with Serial Converter enabled. Unlatched.

On SET:- $\overline{\text{Q}}$ goes Lo stopping Serial Converter (Overload condition). Latched.

On CLOCK:- $\overline{\text{Q}}$ goes Lo stopping Serial Converter. Latched.

SERIAL CONVERTER

CIRCUIT DESCRIPTION

IC1/8-10 :- Enabled by IC6/8-10 during Control Counter states 3 and 4 only, transfers CLOCK pulses to gate IC3/3-6

IC3/3-6 :- Enabled by Parity Latch IC4(a), and CLOCK ÷ 2 pulses, transfer a CLOCK pulse during a CLOCK ÷ 2 period to IC3/10-13.

IC3/10-13 :- This gate transfers pulses to the Toroid Driver TR2 either from

(a) IC3/4-6 or
(b) the Decimal Point Detector.

DECIMAL POINT DETECTOR

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC8 :- Enabled by IC6, transfers the CLOCK ÷ 20 pulses to the Toroid Driver TR2, via the Serial Converter.

ICs13(b) & 6 :- Gate the CLOCK ÷ 20 pulses through IC8 as follows:-

Linked for 7054

$\overline{\text{BAR 'p'}}$:- $\overline{Q}$ is Hi (reset by Control Counter) holding IC6 gate off, disabling IC8.

BAR 'p' :- $\overline{Q}$ goes Lo, IC6 enables IC8, which gates CLOCK ÷ 20 pulses to the Serial Converter, one pulse for each remaining decade scanned.

Linked for 7144

$\overline{\text{BAR 'p'}}$:- $\overline{Q}$ is Hi, CK is Lo and IC6 disables IC8 as before.

BAR 'p' :- CK goes Hi taking IC6/2 with it. $\overline{Q}$ goes Lo but IC6 is still disabled.

$\overline{\text{BAR 'p'}}$:- The reversion to this state on the next decade to be scanned takes CK Lo and IC6 enables IC8. CLOCK ÷ 20 pulses are gated through, one pulse for each remaining decade to be scanned.

This skip action compensates for the smaller scale length (5 digits) of the 7144.

IC13b is held in RESET, being released during Control Counter state S4 only.

MODE DETECTOR

CIRCUIT DESCRIPTION

IC6:- Enables gate IC1 when $\overline{\text{BAR 'a'}}$ and/or $\overline{\text{BAR 'f'}}$ input conditions exist.

Note:- During the scan of decade A1 this is the condition for either of the following modes:- Ω, **mV** or μ**A**.

IC7:- Delays the switching of IC1 by 3 decade counter IC10(a) counting pulses.

IC1:- Will enable IC2 if gating conditions for IC6 are present.

IC2:- Provides for delayed Parity Latch operation during the scan of decade A1, under Control Counter state S4, in modes Ω, **mV** or μ**A**. Then, the Serial Converter is allowed to produce the extra 3 denary pulses. Otherwise, the Parity Latch is operated directly the decade A1 scan commences.

OVERLOAD DETECTOR

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC15:- Detects the presence of a '1' in the 1st Decade (A1) during Control Counter state S3 and produces a SET pulse for IC18(a).

IC18(a):- Conditions the data input (D) of IC18(b).

IC18(b):- Conditions the gate IC3 relative to whether the 2nd Decade (A2) is present or blanked.

The action of the two flip-flops (IC18) is dependent upon the conditions of A1 and A2 prevailing as follows:-

1. **A1:- Blank A2:- Present or blank**

IC15/3 is Lo, IC15 is disabled, no SET pulse available for IC18(a)
IC18(a) has been reset during Control Counter state S0
i.e. Q = Lo
IC18(b) held in reset condition during A1 scan
i.e. Q = Lo and IC3 is disabled.

At the end of A1 both flip-flops are released. During the A2 scan period, no change in IC18(b) output occurs as both flip-flops are clocked, since both data inputs are Lo, thus IC3 remains disabled.

2. **A1:- Present A2:- Present**

IC15 sets IC18(a) Q = Hi
IC18 (b) held in reset during A1 scan
i.e. Q = Lo

At the end of A1 both flip-flops are released. When A2 pulse arrives

IC18(a) is clocked Q = D = Lo = IC18(b) input D
IC18(b) is clocked (after IC18a) Q = D = Lo
IC3 remains disabled.

3. **A1:- Present A2:- Blank (Overload Conditions)**

IC15 sets IC18(a) Q = Hi
IC18(b) held in reset during 1st Decade scan
i.e. Q = Lo

At the end of A1 both flip-flops are released. Since A2 is missing, IC18(a) Q output remains Hi = IC18(b) input D. IC18(b) is clocked by the second pulse produced by decade counter IC10(a) and output Q goes Hi enabling IC3. This produces the latching SET pulse for the Parity Latch, thus disabling the Serial Converter.

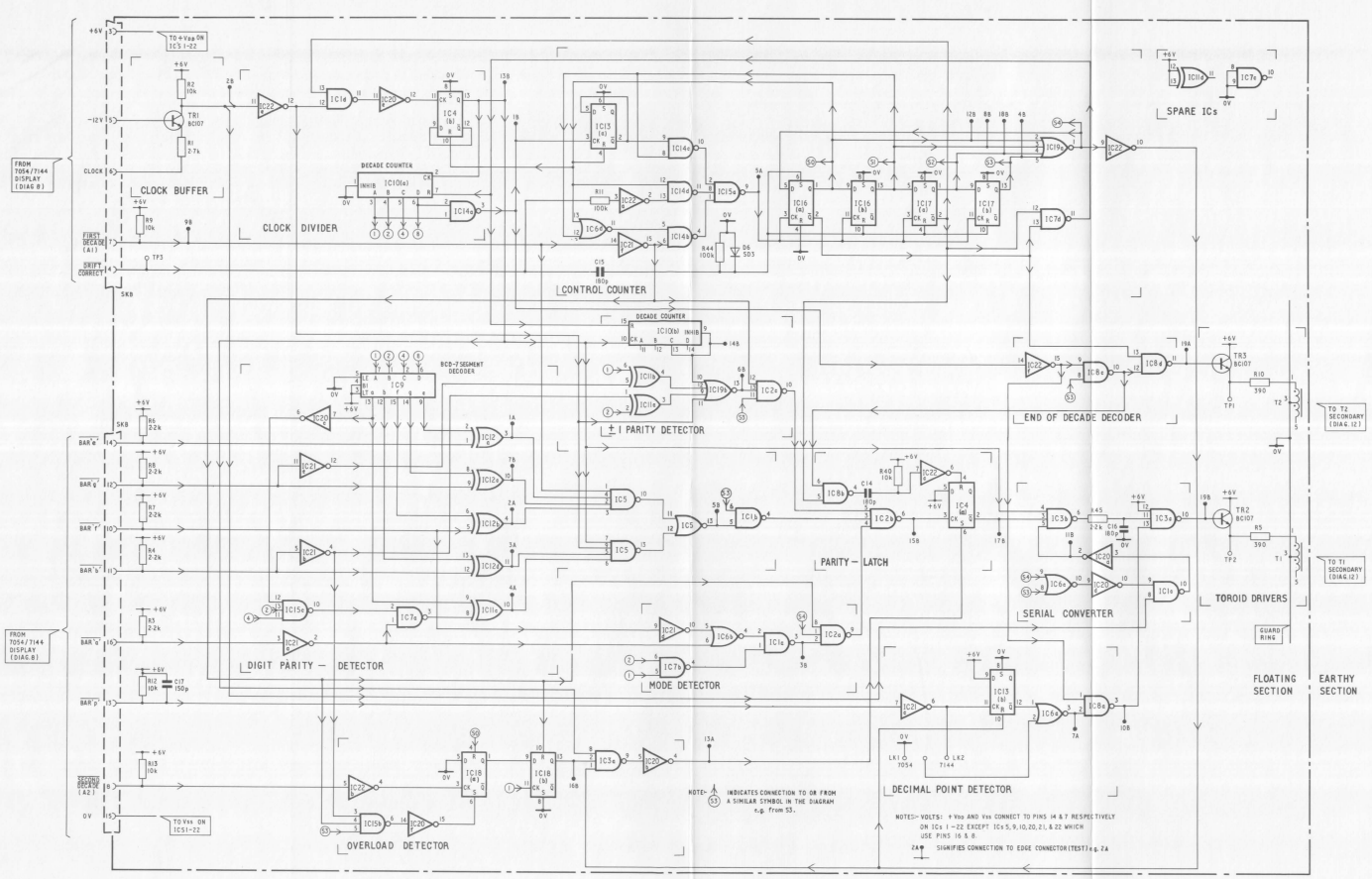
Note:- The first decade counter pulse, which would have produced decimal 0 parity, has allowed one serial denary pulse through the Serial Converter.

During A1, the ± 1 Parity Detector produces the most significant digit, +1 or −1. The second most significant digit, 1, is produced by the single serial denary pulse allowed through the Serial Converter by delayed latching during A2.

TOROID RECEIVERS

CIRCUIT DESCRIPTION

TRs 2 and 3 receive the denary pulses and END OF DECADE pulses respectively, having as their emitter loads the primary windings of transformers T1 and T2.



See Page 3.8 for PCB LAYOUT DIAGRAMS

11 *BCD OUTPUT MODULE FLOATING SECTION CIRCUIT DIAGRAM*

SUB-SECTION 3b-Earthy Section

This sub-section deals with the conversion of the Serial Denary pulses into Isolated Parallel BCD, under the control of the normal Sample/Print Command closed loop control system.

FUNCTIONAL DESCRIPTION (DIAGRAM 12)

MODULE CONTROL

Data conversion in the earthy section is only carried out when a CONTACT SAMPLE, or a PULSE SAMPLE, has been received. Then, the Timing Circuits (Fast Rate Delay) produce a pulse which provides the DMM with a digitising period before a PRINT COMMAND is issued. The Fast Rate Delay pulse enables the gating of the serial denary pulses and counter reset pulses to the Serial-Parallel Converter. When extra time is required by the DMM, e.g. ac measurement, the DATA IS CHANGED control line can be used to switch in the Slow Rate Delay.

A Serialise Delay is incorporated, to allow sufficient time for the serial denary pulses to be steered by the Decade Selector to their respective BCD counters. The leading edge of this pulse resets the BCD counters, while its trailing edge, in conjunction with the ending of the 'sample initiated' delay, is used to produce the PRINT COMMAND pulse. As each decade is steered through, the Serialise Delay is retriggered, ensuring a full conversion before a PRINT COMMAND is given.

Two feedback signals are produced, PRINT COMMAND and DATA CAN CHANGE.

The END OF DECADE pulses are used to step the Decade Selector through the correct gate-operating sequence for the BCD counters.

CIRCUIT ACTION

The serial denary pulses from the 'floating section' are shaped by the Toroid Receiver, and fed to the Serial-Parallel Converter gate but no further, unless a sample is called for. The decade pulses shift the Decade Selector, thus enabling each BCD counter gate in turn (most significant decade first). They also re-trigger the serialise delay after each decade. These actions are continuous whilst the DMM is operating.

When a SAMPLE command is received, the Timing Circuits delays are initiated, the BCD counters are reset and the serial denary pulses are gated through to the counter by gates which are opened in sequence by the Decade Selector. The feedback signal state is:-

$\overline{\text{PRINT COMMAND LEVEL}}$

$\overline{\text{DATA CAN CHANGE}}$

The decades continue to be scanned and up-dated during the Rate Delay (sampling and digitising period). At the end of this period, and when the existing Serialise Delay pulse ends, a PRINT COMMAND pulse is generated. The feedback signal state then is:-

PRINT COMMAND LEVEL

DATA CAN CHANGE

The circuit reverts back to its non-converting state at the end of the PRINT COMMAND delay with the signal states $\overline{\text{PRINT COMMAND LEVEL}}$ and $\overline{\text{DATA CAN CHANGE}}$ again present, awaiting the next SAMPLE command.

The circuit descriptions of the individual functional blocks follow.

TIMING CIRCUITS

MONOSTABLE LOGIC (ICs 23 and 26)

1. Monostable is inhibited by the presence of a Lo on terminal 3 or 13.

2. Monostable is triggered by (a) a +ve going edge on terminal 4 or 12.
   (b) a −ve going edge on terminal 5 or 11.

   Note:- Monostable is retriggerable in both modes.

3. When triggered, terminal 6 or 10 goes Hi for time T, see Table 3b.1.

Table 3b.1

FUNCTION	TIME. T
FAST RATE DELAY (IC 23b)	$0.65s \pm 50\%$
SLOW RATE DELAY (IC 23a)	$2.4s \pm 25\%$
SERIALISE DELAY (IC 26b)	$2.5ms \pm 20\%$
PRINT COMMAND PULSE (IC 26a)	$20\mu s \pm 50\%$

FLIP FLOP LOGIC

See Basic Logic Elements (SECTION 3).

CIRCUIT DESCRIPTION

IC23 :- Produces the length of pulse required to match DMM operating rates when a sample is called for.

For FAST RATE:- IC23(a) is inhibited and only IC23(b) is activated by IC25/11 going Lo.

For SLOW RATE:- Both IC23(a) and IC23(b) are activated by IC25/11 going Lo.

IC26(b) :- Produces a pulse of sufficient length to allow the BCD Counters to count through two complete sets of decades.

Q going Hi:- (a) Sets IC34/7 Hi in readiness for shift register action.
(b) Produces the BCD Counter reset pulse if a sample has been called.

$\overline{Q}$ going Lo:- Sets IC29, only if a sample has been called for.

Q going Lo:- Takes IC34/7 Lo for next Decade Selection cycle.

$\overline{Q}$ going Hi:- (a) Clocks IC29 to Q = D.
(b) Removes the SET on IC29 if a sample is called for.

IC29 :- Provides the following functions:-

Q going Hi:- (a) Enables BCD counter reset gate, IC33/1.
(b) Enables data pulse gate, IC33/11.
(c) Produces $\overline{\text{DATA CAN CHANGE}}$ signal.

$\overline{Q}$ going Lo:- Produces $\overline{\text{PRINT COMMAND LEVEL}}$ signal.

Q going Lo:- (a) Disables gates IC33/1 and IC33/11.
(b) Triggers IC26(a) producing a PRINT COMMAND pulse.
(c) Produces DATA CAN CHANGE signal.

$\overline{Q}$ going Hi:- Produces PRINT COMMAND LEVEL signal.

Gates IC25 and IC37 control the set, and input D functions of IC29.

DECADE SELECTOR

SHIFT REGISTER LOGIC

Clocked operation only is used, the triggering being on the +ve going edge of the waveform, and in accordance with the following truth table.

INPUT	OUTPUTS	
DATA	Q_n	Q_n+1
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$
$R = 0$
$Q_0 = A$
$Q_1 = B$ etc.

CIRCUIT DESCRIPTION

Table 3b.2 illustrates a complete serialise period and the resulting logic level changes in the shift register.

INPUTS			IC34 OUTPUTS						
FUNCTION	D1	D2	A	B	C	D	E	F	G
1. INITIAL CONDITION (Assumed)	0	1	1	1	1	1	1	1	1
2. SERIALISE DELAY INITIATED*	1	1	0	1	1	1	1	1	1
3. DECADE PULSE A1 ARRIVES	1	1	1	0	1	1	1	1	1
4. " " A2 "	1	1	1	1	0	1	1	1	1
5. " " A3 "	1	0	1	1	1	0	1	1	1
6. " " A4 "	1	1	1	1	1	1	0	1	1
7. " " A5 "	1	1	1	1	1	1	1	0	1
8. " " A6 "	1	1	1	1	1	1	1	1	0
9. RANGE DATA PULSES ARE GATED	1	1	1	1	1	1	1	1	0
10. SERIALISE DELAY ENDS (IC33 closes)	0	1	1	1	1	1	1	1	0
11. NEXT SERIALISE DELAY INITIATED*	1	1	0	1	1	1	1	1	1

* ACTIVATED BY THE DRIFT CORRECT PULSE LEADING EDGE AND RETRIGGERED BY EACH DECADE PULSE.

Table 3b.2

1. IC26(b) is in quiescence, D1 of IC34 is Lo.

2. IC32/11 goes Hi clocking IC26(b) and transferring the D1 input of IC34 to its output A. IC26(b) takes IC34 D1 input Hi.

3 - 8. The decade pulses propagate the Lo through the shift register, enabling the BCD counter gates ICs 27 and 37 in the order given in Table 3b - 2.

9. The Range data pulses are gated to the seventh BCD counter.

10. IC26(b) returns to quiescence, putting a Lo on the D1 input of IC34 in readiness for the next serialisation.

11. The next serialise delay initiating pulse clocks the Lo, retained in gate G, out of the register and starts another sequence.

SERIAL – PARALLEL CONVERTER

BCD COUNTER LOGIC

CLOCK	ENABLE	RESET	ACTION
⎍	1	0	INCREMENT COUNTER
X	X	1	OUTPUTS A to D go to 0

⎍ = Level Change X = 1 or 0

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3).

CIRCUIT DESCRIPTION

IC33/1 :- Gates the serialise delay pulse to C8/R21 and IC33/5, producing the BCD counter reset pulse.

IC33/11 :- Gates the data pulses to IC27 and IC37.

ICs 27 & 37 :- Directs data pulses to be counted by the relevant counter ICs 24, 30, 35 and 38.

ICs 30, 35 & 38 :- Normal incrementation by the CLOCK (CK) input.

IC24 :- The counting action of these flip-flops is illustrated in Table 3b.3 with their relevant outputs. e.g. 2 pulses counted = + 100000

INPUT PULSE	IC 24(a)				IC 24(b)				OUTPUT
	CK	D	Q	$\overline{Q}$	CK	D	Q	$\overline{Q}$	
RESET	0	1	0	1	1	1	0	1	+VE(BLANK)
1st. DENARY	1	0	1	0	0	1	0	1	−VE
REST	0	0	1	0	0	1	0	1	
2nd. DENARY	1	1	0	1	1	0	1	0	100000
REST	0	1	0	1	1	0	1	0	
3rd. DENARY	1	0	1	0	0	0	1	0	−100000
REST	0	0	1	0	0	0	1	0	

Table 3b.3

ICs 28, 31, 36, 39 and 40 are the buffer stages, maintaining TTL compatibility.

Note: They use +10V and +5V power supplies.

TOROID DRIVERS

The decade and serial denary data pulses are differentiated by the transformers, T1 and T2. The transistors TRs 10 - 13 use the positive going spikes to trigger the latching circuits of IC32.

BUFFER

TRs 8 and 9 buffer IC23(a) from the driving peripheral.

DATA IS CHANGED = Hi (used to provide the extended sample and digitisation period).

SAMPLE COMMAND BUFFERS

TRs 4, 5 and 7 buffer IC25/11 - 13 from the peripheral driving circuits.

Contact Sample:- Pin 11B going Lo clocks IC23(a) and/or IC23(b).

Pulse Sample:- Pin 12B going Hi clocks IC23(a) and/or IC23(b).

IC25/11 - 13:- Produces the triggering pulses for IC23.

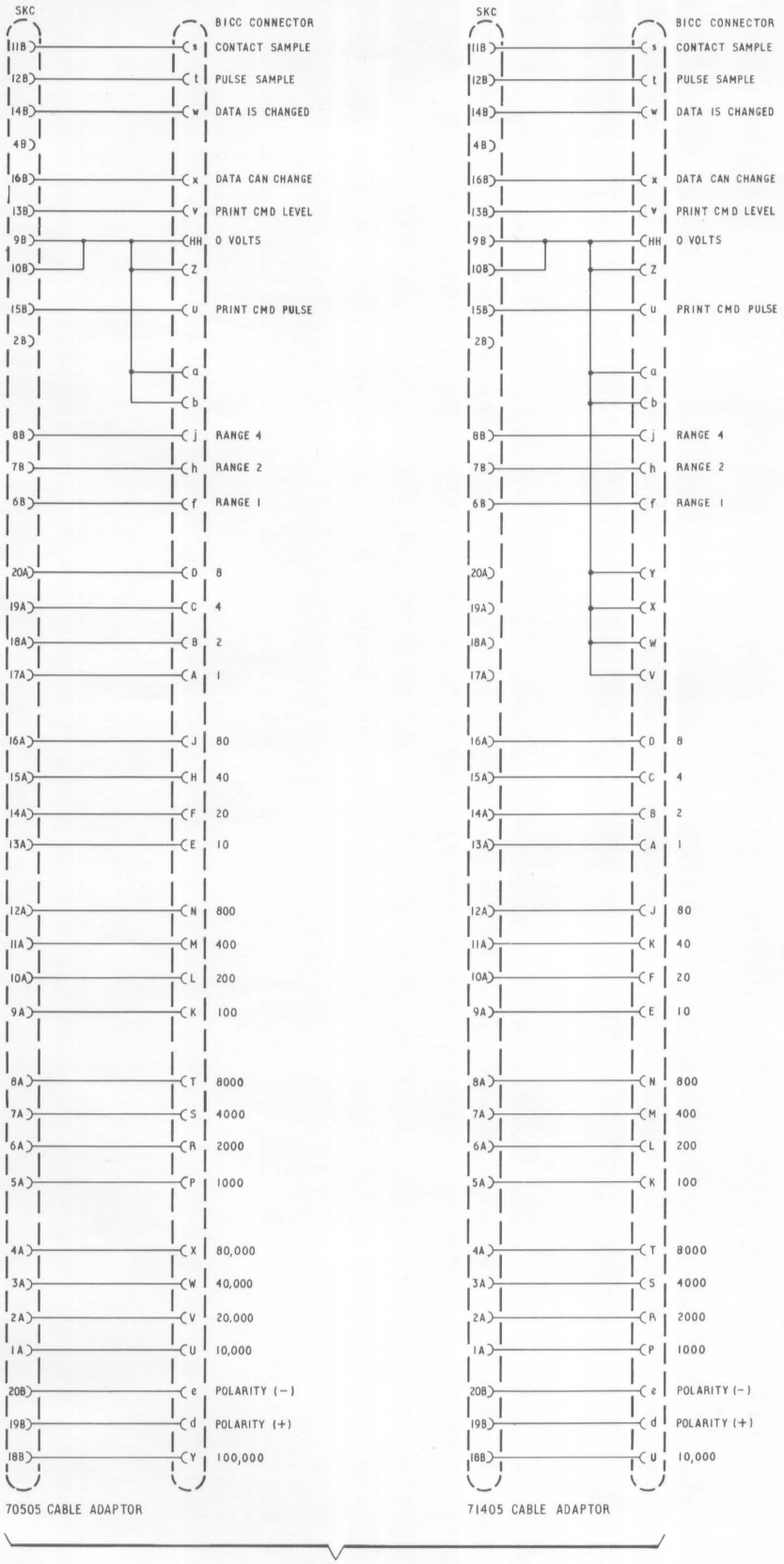
Capacitors C11 and C12 prevent triggering of the circuit by low energy noise spikes.

POWER SUPPLY

TR6, D3 and D4 provide the necessary stabilised +5V supplies for the output buffers, ICs 28, 31, 36, 39 and 40.

CABLE ADAPTORS 70505 AND 71405

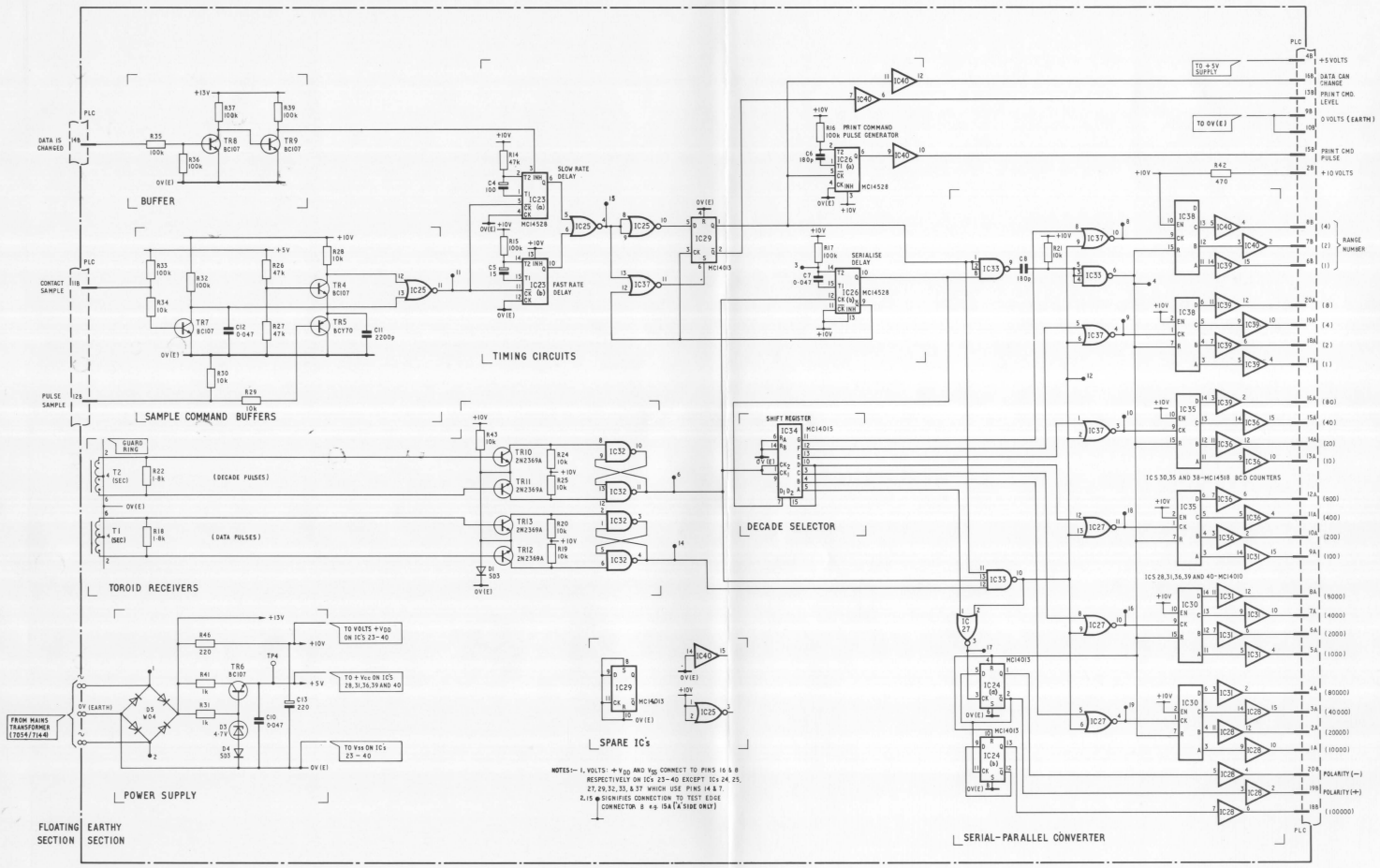
These cable adaptors are outwardly identical, differing in the socket interconnections, as shown in DIAGRAM 13.



FROM TRANS (7054

13 *DMM CABLE ADAPTOR CONNECTION DIAGRAMS*

◀ *DIAGRAM 12 - BCD OUTPUT MODULE EARTHY SECTION CIRCUIT DIAGRAM*



See Page 3.8 for PCB LAYOUT DIAGRAMS

12 *BCD OUTPUT MODULE EARTHY SECTION CIRCUIT DIAGRAM*

SECTION 4-Functional Checks

The tests detailed in this section check that the BCD output from the Module correlates with the value displayed on the DMM. Module testing is carried out using special test equipment, Solartron TG1308/G Output Reader. This item of test equipment is not available for purchase but details of the circuit diagram, and component parts, are shown in Fig. 4.1.

PRE - CHECK TESTS

It is assumed that the DMM is fully serviceable and that the BCD Output Module has been checked in accordance with Section 2.

The following test can now be carried out.

OUTPUT BUFFER AMPLIFIER POWER SUPPLY

1. Locate test point TP4 (near rectifier bridge D5) and the 0V (E) terminal.

2. Check that the voltage between TP4 and 0V (E) is:-

   $+4.7 \pm 0.5$ Volts.

PROCEDURE USING THE TG1308/G OUTPUT READER

1. Connect the TG1308/G to the DMM.

2. Switch ON the DMM and the Output Reader. Select 'VDC' on the DMM and the appropriate 7054/7144 mode on the reader.

3. Short circuit the Hi and Lo terminals of the DMM and check that the DMM reads approximately 0.00mV.

4. Set the TG1308/G to MANUAL SAMPLE, and DATA IS CHANGED to '0' (=Lo).

5. Press the MANUAL SAMPLE button and check that the Output Reader displays approximately (digit for digit correlation):-

   0.00000

NOTE:- 0.01mV is displayed on the reader as:-

0.00001

6. Set the TG1308/G to AUTO SAMPLE.

For the following inputs check that the relative readings are displayed on the DMM and the Output Reader.

NOTE:- A zero (0) and/or a positive (+) sign may be displayed in the most significant digit of the reader, dependent on type of Output Reader used.

'VDC' MODE

7054		7144	
DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
9.00mV	+ .00900	9.00mV	+ 0900
90.00mV	+ .09000	90.00mV	+ 9000
900.00mV	+ .90000	900.0mV	+ 9000
9.0000V	+ 9.0000	9.000V	+ 9.000
90.000V	+ 90.000	90.00V	+ 90.00
900.00V	+ 900.00	900.0V	+ 900.0
− 900.00mV	− .90000	− 900.0mV	− .9000
− 1.0000V	− 1.00000	− 1.000V	− 1.0000

Ω MODE

7054		7144	
DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
0.0Ω	+ 0.0000	0.0Ω	+ 0.000
900.0Ω	+ 0.9000	900.0Ω	+ .9000
9.0000kΩ	+ 9.0000	9.000kΩ	+ 9.000
90.000kΩ	+ 90.000	90.00kΩ	+ 90.00
900.00kΩ	+ 900.00	900.00kΩ	+ 900.0
9000.0kΩ	+ 9000.0	9000kΩ	+ 9000
1−−−−−kΩ	+ 11000.0	1−−−−kΩ	+ 11000

'μA' MODE

7054		7144	
DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	DMM DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
0.000μA	± 00000	0.000μA	± 0000
90.000μA	+ 90000	90.00μA	+ 9000
900.00μA	+.90000	900.0μA	+.9000

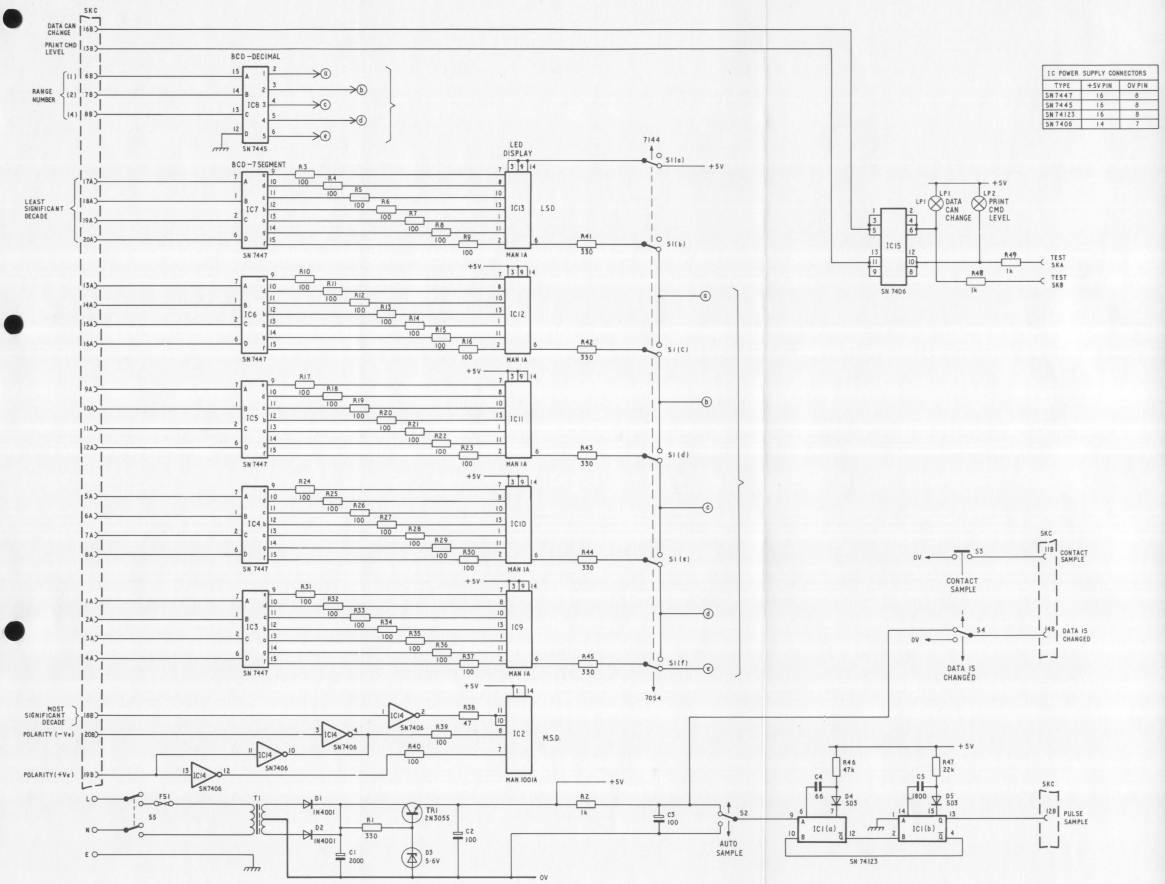
7. Set the TG1308/G to MANUAL SAMPLE.

8. Press MANUAL SAMPLE button and check:-

   After 0.9 ± 0.4 seconds (a) PRINT COMMAND LEVEL lamp lights.
   (b) DATA CAN CHANGE lamp extinguishes.

9. Set the DATA IS CHANGED to '1' (= Hi). Press the MANUAL SAMPLE button and check:-

   After 2.5 ± .5 seconds (a) PRINT COMMAND LEVEL lamp lights.
   (b) DATA CAN CHANGE lamp extinguishes.



I.C. POWER SUPPLY CONNECTORS		
TYPE	+5V PIN	0V PIN
SN7447	16	8
SN7445	16	8
SN74123	16	8
SN7406	14	7

Components List

for

Test Circuit, Fig. 4.1

Cct. Ref.	General Description		
R1	330	1/4W	10%
R2	1k	1/4W	10%
R3 to R37	100	1/4W	10%
R38	47	1/4W	10%
R39	100	1/4W	10%
R40	100	1/4W	10%
R41 to R45	330	1/4W	10%
R46	47k	1/4W	10%
R47	22k	1/4W	10%
R48	1k	1/4W	10%
R49	1k	1/4W	10%
C1	2000	30V	10%
C2	100	25V	10%
C3	100	25V	10%
C4	66	40V	10%
C5	1800p	30V	10%
D1	IN4001		
D2	IN4001		
D3	Zener 5.6V		
D4	IN914		
D5	IN914		
TR1	2N3055		
IC1	Retriggerable Monostable Multivibrator SN74123		
IC2	Light Emitting Diodes MAN 1001A		
IC3 to IC7	BCD to 7 Segment Decoder SN7447		
IC8	BCD to Decimal Decoder SN7445		
IC9 to IC13	Light Emitting Diodes MAN 1A		
IC14	Hex Inverters and Buffers SN7406		
IC15	Hex Inverters and Buffers SN7406		
LP1	Lamps 6V		
LP2	Lamps 6V		
S1	Rotary Switch (6 pole x 2 way)		
S2	Switch (1 pole x 2 way)		
S3	Button Switch (Push to make)		
S4	Switch (1 pole x 2 way)		
S5	Main ON/OFF Switch (2 pole x 2 way)		
T1	Transfer 12 - 0 - 12, 700mA		
FS1	Fuse 650mA		

NOTE:- Resistor values are in OHMS.
Capacitor values are in MICROFARADS, except when followed by a ' p ', signifying PICOFARADS.

Fig. 4.1 TG1308/G BASIC CIRCUIT DIAGRAM

SECTION 5-Parts List

Component Parts List

for

BCD Output Module 70509004

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	2.7k	1/8W	±10	172032700
R2	CACP	1.0k	1/8W	±10	172041000
R3 AND R4	CACP	2.2k	1/8W	±10	172032200
R5	CACP	390	1/8W	±10	172023900
R6 to R8	CACP	2.2k	1/8W	±10	172032200
R9	CACP	10k	1/8W	±10	172041000
R10	CACP	390	1/8W	±10	172023900
R11	CACP	100k	1/8W	±10	172051000
R12	CACP	10k	1/8W	±10	172041000
R13	CACP	10k	1/8W	±10	172041000
R14	CACP	47k	1/8W	±10	172044700
R15 to R17	CACP	100k	1/8W	±10	172051000
R18	CACP	1.8k	1/8W	±10	172031800
R19 to R21	CACP	10k	1/8W	±10	172041000
R22	CACP	1.8k	1/8W	±10	172031800
R24	CACP	10k	1/8W	±10	172041000
R25	CACP	10k	1/8W	±10	172041000
R26	CACP	47k	1/8W	±10	172044700
R27	CACP	47k	1/8W	±10	172044700
R28 to R30	CACP	10k	1/8W	±10	172041000
R31	CACP	1k	1/8W	±10	172031000
R32	CACP	100k	1/8W	±10	172051000
R33	CACP	100k	1/8W	±10	172051000
R34	CACP	10k	1/8W	±10	172041000
R35 to R37	CACP	100k	1/8W	±10	172051000
R39	CACP	100k	1/8W	±10	172051000
R40	CACP	10k	1/8W	±10	172041000
R41	CACP	1k	1/8W	±10	172031000
R42	CACP	470	1/8W	±10	172024700
R43	CACP	10k	1/8W	±10	172041000
R44	CACP	100k	1/8W	±10	172051000
R45	CACP	2.2K	1/8W	±10	172032200
R46	CACP	220	1/8W	±10	172022200
C4	TANW	100	20V	±20	265881000
C5	TANW	15	20V	±20	265871500
C6	MICA	180p	500V	±5	250321800
C7	ESTM	0.047	100V	±10	225444700
C8	MICA	180p	500V	±5	250321800
C10	ESTM	0.047	100V	±10	225444700
C11	ESTF	2200p	160V	±10	221332200
C12	ESTM	0.047	100V	±10	225444700
C13	ALME	220	16V	+100 −10	273382200
C14	MICA	180p	500V	±5	250321800
C15	MICA	180p	500V	±5	250321800
C16		180p	500V	±5	250321800
C17	CERM	150p	500	±20%	241321500

Cct. Ref.	General Description				Solartron Part No.
D1	SD3				300522160
D3	Zener	4.7V	0.4W	±5	300521470
D4	SD3				300522160
D5	WO4	1A	400V		300524700
D6	SD3				300522160
TR1 to TR4	BC107				300553320
TR5	BCY70				300553590
TR6 to TR9	BC107				300553320
TR10 to TR13	2N2369				300552390
IC1	MC14011				510001660
IC2	MC14023				510001670
IC3	MC14023				510001670
IC4	MC14013				510001740
IC5	MC14501				510001710
IC6	MC14001				510001630
IC7	MC14011				510001660
IC8	MC14011				510001660
IC9	MC14511				510001850
IC10	MC14518				510001840
IC11	MC14507				510001700
IC12	MC14507				510001700
IC13	MC14013				510001740
IC14	MC14011				510001660
IC15	MC14023				510001670
IC16	MC14013				510001740
IC17	MC14013				510001740
IC18	MC14013				510001740
IC19	MC14002				510001650
1C20 to 1C22	MC 14049/CD 4049 AE				510001730
IC23	MC14528				510001770
IC24	MC14013				510001740
IC25	MC14001				510001630
IC26	MC14528				510001770
IC27	MC14001				510001630
IC28	MC14010				510001720
IC29	MC14013				510001740
IC30	MC14518				510001840
IC31	MC14010				510001720
IC32	MC14011				510001660
IC33	MC14023				510001670
IC34	MC14015				510001890
IC35	MC14518				510001840
IC36	MC14010				510001720
IC37	MC14001				510001630
IC38	MC14518				510001840
IC39	MC14010				510001720
IC40	MC14010				510001720
T1	Pulse Transformer				309605702
T2	Pulse Transformer				309605702

Component Parts List

for

Accessories - 70505/71405 Cable Adaptors

Cct. Ref.	General Description	Solartron Part No.
SKC	Connector 20 + 20 way	352520020
	Cover	33010015
	LID Moulding	33010023
	Screw M3 x 6 LG C'SK.HD. (2 off)	406403060
	Connector, 50 way Shell with Clamp	354003370
	Sockets, hyfen (36 off)	354003270
	Wire, 7/.20 x 0.3mm Wall White PVC DEF 16.12	480011090

SECTION 6-Specifications

This section contains a copy of the technical specification applicable to the 7054/7144 BCD Output Module. The module is designed and manufactured to a higher specification than is claimed commercially. In order that the user may benefit as appropriate, this technical manual may relate to a superior performance. In the event of contraditions between specifications, no additional claims are made for the module above those claimed in the current product data sheet.

General

BCD Output

Type of Logic: Positive

Scale Length: 109999 max. for 7054

10999 max. for 7144

Polarity Indications: Positive and negative

Overload Indication:

Mode	7054	7144
V.AC	+1100.00	+1100.0
V.DC	± 11000.0	± 11000
Ω	+1100.00	+1100.0
μA*	± 1100.00	± 1100.0

*Position of decimal point is invalid.

Range Data:

Instrument Range	Range No. 7054	Range No. 7144
> 1000V	2	1
1000V	2	1
100V	3	2
10V	4	3
1V	5	4
100mV	N/A	5
> 10MΩ	1	0
10MΩ	1	0
1MΩ	2	1
100kΩ	3	2
10kΩ	4	3
1kΩ	N/A	4
> 1mA	2	1
1mA	5	4
100μA	6	5
10μA	N/A	6

N/A = Not Applicable

Environment

Working Temperature Range: $0^{o}C$ to $+45^{o}C$

Storage Temperature Range: $-30^{o}C$ to $+70^{o}C$

Maximum Relative Humidity: 70% at $40^{o}C$

Power Supply

Floating Section: + 6V (from the DMM Power Rail)

Earthy Section: $+10V^{+3V}_{-2V}$

$+4.7V \pm 0.5V$

Output Levels

All outputs are TTL compatible and are staticised.

$+2.4V <$ logic $1 < +6.0V$

$-0.5V <$ logic $0 < +0.5V$ capable of sinking 5 standard TTL loads.

Input Levels

All inputs are TTL compatible.

Sample Command (Input)

Contact Sample: A sample is initiated by a contact closure between pin 11B and 0V for $>$ 4ms. A current of approximately 50μA will pass through the contacts.

Pulse Sample: A positive going pulse of $>$ 10μs duration and between 3V and 8V amplitude will initiate a sample. This pulse is applied to pin 12B on which the input impedance is approximately 10kΩ.

Data is Changed (Input)

For normal use pin 14B should be held at $+2V < V < +10V$. This is achieved by connecting pin 14B to pin 4B. In this mode of operation each measurement will take approximately 3 seconds, which allows the DMM time to change range and settle on new reading.

When it is known that the input will not change sufficiently to result in a DMM range change, the measuring time may be reduced to approximately 1 second. To do this, ensure that pin 14B is kept at $-0.5V < V < 1V$ (i.e. connect it to 0V, pin 10B).

Long period = 2.4s ± 50%

Short period = 650ms ± 50%

Numerical Output

Parallel BCD 1 - 2 - 4 - 8 code on:-

7054 DMM: Pins 1A to 20A (5 decades) with the most significant digit (100 000) on pin 18B.

7144 DMM: Pins 1A to 16A (4 decades) with the most significant digit (10000) on pin 18B.

Range Information (Output)

Data output indicating position of the decimal point is given in BCD code on pins 6B, 7B and 8B. If

n = Decimal equivalent of the BCD number

the readings conform with the equation.

Value = Reading (as an integer) x 10^{-n} V

or = Reading (as an integer) x 10^{-n} kΩ

or = Reading (as an integer) x 10^{-n} mA

Note:- The equation is incorrect for an OVERLOAD condition in the μA mode.

Polarity Output

Logical 1 on pin 19B for positive polarity.

Logical 1 on pin 20B for negative polarity.

Print Command Pulse (Output)

Positive going pulse of 10μs to 30μs duration issued on completion of a reading. May be used to stimulate a printer or similar output device.

Print Command Level (Output)

Pin 13B is held at logic 0 following a sample command and changes to logic 1 when the new reading is available at the output connector.

Data can Change (Output)

This is the complement of Print Command Level and is available on pin 16B.

Isolation

Resistance between BCD output pin 9B (0V) and the DMM front panel Lo terminal $> 10^9\Omega$ at 500V.

70505/71405 Cable Adaptor Options

Each option consists of a socket which fits into the rear of the DMM. This socket mates with the Module pcb edge connector and has it's cable terminating in a BICC BURNDY socket, so enabling direct compatibility with other Solartron equipment. The socket allocations for each option are shown in Diagram 13.