AN2577

4¾ - Digit (±39999 count)
0.005% Accuracy, Ultra-High Performance
DIGITAL PANEL INSTRUMENT

DESCRIPTION

The AN2577 is a premium performance 4¾-digit digital panel instrument which enhances Analogic's broad line of high performance digital panel instruments. The full scale readout (±39999 count) provides a resolution of ±0.0025% with a guaranteed accuracy of ±0.005%. The input amplifier has a bipolar differential input circuit with an input impedance of 10^9 ohms. It is protected against overvoltages up to ±100 volts. The AN2577 is offered with either of two full-scale ranges: the ±3.9999-volt range provides 100μV/count sensitivity; the ±399.99 millivolt range provides a 10μV/count sensitivity.

The 3-phase, dual-slope A/D converter includes an automatic zero feature for long-term accuracy. The "unknown" integration period is optimized to yield a Normal Mode Rejection Ratio (NMRR) in excess of 90dB. The entire input amplifier and A/D converter are isolated (floated) up to ±300 volts with respect to digital ground. This level of isolation yields a Common Mode Rejection Ratio (CMRR) of up to 140dB.

The digital portion includes the drivers for the large LED red, planar display, and several status and control lines. Control signal inputs are included to BLANK the display, HOLD the last value, TEST the display, and to select the decimal point location. The AN2577 may be externally triggered for up to 10 conversions per second. Status signals include converter STATUS and OVERRANGE. The standard AN2577 includes a universal ac power supply for either 110Vac or 220Vac ±20%, from 50 to 500Hz (@ 2.7 Watts). The power supply provides up to 1400 volts dc or ac peak isolation between the digital ground and ac power line, and between the analog ground and ac power line.

The optional parallel BCD outputs are microprocessor-compatible, word-programmable, tri-state outputs. This feature allows the data from one or more digital panel instruments to be transferred over a single set of data lines.

The standard AN2577 is packaged in a rugged DIN/NEMA high-Impact molded plastic case which is UL94V-0 rated. An optional all-metal case provides additional EMI/RFI shielding and protection. Every AN2577 is subjected to comprehensive testing under Analogic's Quality Assurance program which includes a 100-hour temperature-cycled burn-in, from 0°C to +50°C, with power ON/OFF cycling. Every instrument is vibration tested, calibrated, and shipped with a detailed calibration certificate, certified by Analogic's Quality Assurance Department. The AN2577 is covered by a full 12-month warranty.

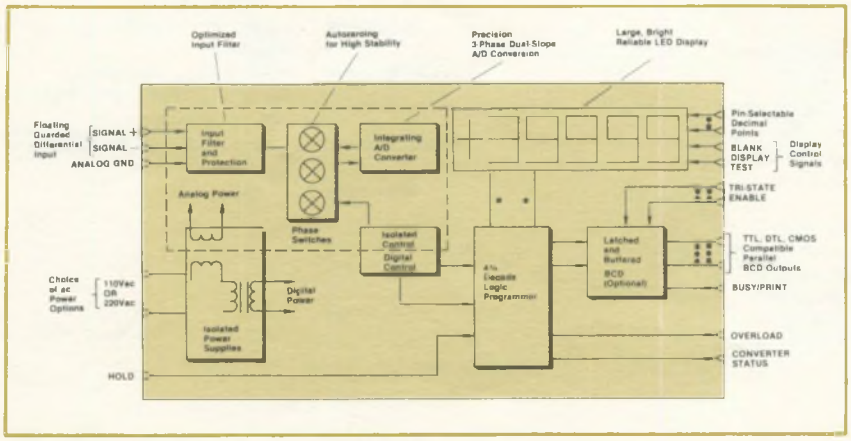

Fig. 1. AN2577 Functional Block Diagram.

FEATURES

- High Performance – Low Cost
- Accuracy of ±0.005% of Reading ±1 Count
- 10 microVolt Sensitivity (for ±399.99mV FS)
- ±0.0025% Readout Resolution for 39999 Counts
- Floating Bipolar Differential, Guarded FET input
- Ultra Low Bias Current (Less Than 50 picoAmps)
- Automatic Zero for Long-Term Stability
- Input Protection for more than 100 Volts
- Floating & Isolated Input (1400 Volts)
- High Input Impedance (1000 Megohms)
- CMRR Greater Than 140 dB
- NMRR Greater Than 90 dB
- One Line Cycle Integration Period for highest NMRR and CMRR
- DISPLAY TEST, HOLD, BLANK, OVER-RANGE and Converter Status Control Signals
- TRI-STATE BCD Output, Word-Programmable; Optional
- Ratiometric Capability, 3-Wire; Optional
- Large .43" (11mm) LED Display for Maximum Readability
- Universal Power Options Include:
  110VAC ±20% @ 2.7 Watts
  220VAC ±20% @ 2.7 Watts
- DIN/NEMA Standard Case; UL94V-0 Rated
- 12-Month Recommended Recalibration Interval
- Rear Screw Terminal Connector Available

APPLICATIONS

- Precision Analytical Instrumentation
- High Accuracy Digital Process Indicators With Universal Computer Bus Interface
- Industrial Weighing and Scaling Systems
- Laboratory Digital Phase Angle Indicators
- High Resolution Strain Gauge Digitizers

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AN2577 SPECIFICATIONS

ANALOG INPUT

Configuration	Bipolar, isolated and floating differential input.
Full Scale Range	±3.9999Vdc or ±399.99mVdc.
Input Resistance	>1000 Megohms.
Bias Current @ 25°C	50pA typical, 100pA max.
Input Protection	
±3.9999Vdc Full Scale	±100Vdc or ac rms continuous without damage.
±399.99mVdc Full Scale	±20Vdc or ac rms continuous without damage.
Input Filter	Single-pole, optimized signal-enhancement filter.
Normal Mode Rejection Ratio	90dB typical, 70dB min. @50 or 60Hz.
Ratiometric Operation	3-wire ratio input for use with external reference (Consult factory).

COMMON MODE

Signal Return to Digital Ground Voltage (CMV)	±300Vdc or ac peak.
dc Rejection Ratio;(CMRR)	140dB typical, 120dB min.
ac Rejection Ratio;(CMRR)	120dB typical, 100dB min. @ 50 to 60Hz.
Digital Ground to ac Power Line Voltage (CMV)	1400Vdc or ac peak.
ac Rejection Ratio;(CMRR)	160dB min. @ 50 to 60Hz.

PERFORMANCE

Accuracy	±0.005% of reading ±1 count.
Resolution	±0.0025% for ±39999 counts.
Range Tempco	±5ppm of reading/°C typical, ±10ppm of reading/°C max.
Zero Stability	Autozero: ±0.2μV/°C typical for 399.99mV full scale; ±2μV/°C typical for 3.9999Vdc full scale.
Step Response	Less than 100msec for ±0.005% of reading accuracy for a "+" or "−" full-scale step input.

DISPLAY AND CONTROLS

Type of Display	7-segment planar, red LED, 0.43" (11mm) high.
Polarity Indication	Automatic, "+" or "−" sign displayed.
OVERRANGE Indication	All digits blanked to prevent erroneous readout, "+" or "−" sign and decimal point remain on.
Decimal Points	4-position, user-selectable at rear connector.
TRIGGER/HOLD Input	Logic 0 holds last reading, logic 1 allows a nominal 2.5 conversion/second rate. A positive pulse with a rise time <200nsec and a pulse width of >2 μsec will trigger a new conversion up to 8 conv./sec. (L5) or 10 conv./sec. (L6). CMOS compatible (0 to +5Vdc).
BLANK INPUT	Logic "0" (open collector or equivalent) blanks display.
DISPLAY TEST INPUT	Logic "0" (sink 0.2mA to digital ground). Tests all 35 segments of display by displaying "88888"

ANALOG TO DIGITAL CONVERSION

Technique	Dual-slope, 3-phase conversion with automatic zero correction. Complete conversion each cycle.
Rate	2.5 conversions per second nominal, for best visual interpretation. For high speed, see Application Data.

Analog To Digital Conversion (continued).

Input Integration Period	20.00 milliseconds nominal for optimum 50Hz rejection. 16.67 milliseconds nominal for optimum 60Hz rejection.

DIGITAL OUTPUTS

All outputs are TTL/CMOS compatible (0 to +5VDCpositive true logic except as noted).

Parallel BCD (Optional)	Latched and buffered word-programmable TRI-STATE outputs are available for computer bus interfacing. The 20 bits of digital data are available as parallel output or organized for a 4, 8, 12, 16 or 20-bit data bus. A separate TRI-STATE ENABLE input (CMOS compatible 0 to +5V) controls each of the 4-bit bytes. BUSY and $\overline{\text{BUSY}}$ provide the user with output register status. (One TTL load each).
POLARITY	Logic "1" indicates a "+" displayed.
OVERLOAD (OVLD)	Logic "0" indicates that output exceeds ±39999 counts.
CONVERTER STATUS	A logic "1" indicates that the converter is busy. A TRIGGER or HOLD command will be ignored at this time.

POWER

Choice of 2 ac Power Inputs	110Vac rms ±20%, 47 to 500Hz @ 2.7 watts nominal (88 to 132 Vac input range). 220Vac rms ±20%, 47 to 500Hz @ 2.7 watts nominal (176 to 264 Vac input range).

ENVIRONMENTAL & PHYSICAL

Operating Temperature Range	−10°C to +50°C.
Storage Temperature Range	−40°C to +85°C.
Relative Humidity	0 to 90%, noncondensing.
Case	DIN/NEMA standard, high-impact molded plastic case UL94V-0 rated; metal case available. (See Ordering Guide).
Dimensions	DIN/NEMA (See Fig. 14).
Weight	12 oz. (360 grams).
EMI/RFI	Shielding on five sides with metal case option.
Special Line Noise Suppression	Provision made for surge suppressor varistor and line input passive filtering for industrial applications. (Consult factory).

RELIABILITY

MTBF	>60,000 Hours, calculated.
Burn-In	100 hours with 0 to +55°C temperature cycles and power on/off cycles.
Vibration	Each unit vibrated at 5g's for 30 seconds.
Calibration	NBS traceable, detailed certificate of calibration shipped with each unit.
Recalibration	Recommended at 12-month intervals.
Warranty	12 Months.

PIN DESIGNATIONS

J1 (BOTTOM OF CASE)

*Ratio Input	A	1	Signal IN
Analog Ground	B	2	Signal Rtn.
Guard	C	3	Guard
Spare	D	4	Spare
Digital Ground	E	5	Digital Ground
TRIGGER/HOLD	F	6	BLANK/OVERLOAD
DISPLAY TEST	H	7	Conversion Rate
CONVERTER STATUS	J	8	Spare
N.C.	K	9	Spare
Decimal Point 1	L	10	Decimal Point 3
Decimal Point 2	M	11	Decimal Point 4
Digital Ground	N	12	+5 Volts
N.C.	P	13	N.C.
N.C.	R	14	N.C.
ac Power IN	S	15	ac Power IN

*Consult factory.

J2 (TOP OF CASE) TRI-STATE BCD OUTPUTS

BCD Digit 3: 100	A	1	1 BCD Digit 1
200	B	2	2
400	C	3	4
800	D	4	8
Enable Digit 3	E	5	Enable Digit 1
BCD Digit 4: 1K	F	6	10 BCD Digit 2
2K	H	7	20
4K	J	8	40
8K	K	9	80
Enable Digit 4	L	10	Enable Digit 2
BUSY	M	11	10K
Dig. Gnd.	N	12	20K
BUSY	P	13	OVERRANGE Digit 5
+5 Volts	R	14	Polarity
Spare	S	15	Enable Digit 5

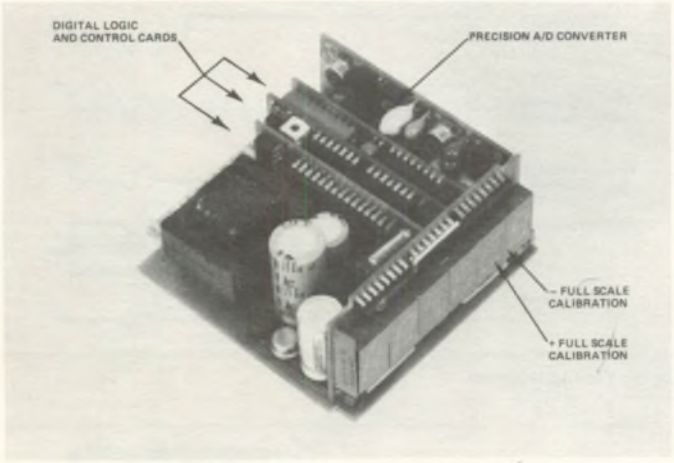

Fig. 16. Internal View.

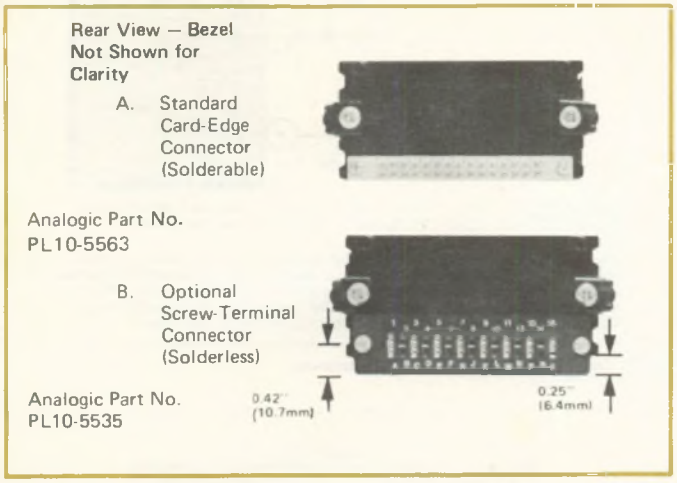

Fig. 17. Rear Panel Connectors.

ORDERING GUIDE

AN2577 — [ ] — [ ] — [ ] — [ ] — [ ]

Full Scale Range	
±3.9999 Volts	1
±399.99 mV	01
Without BCD	X
With Parallel Tri-State BCD	1
Power Requirements	
110 Volts ac ±20%	1
220 Volts ac ±20%	2
Integration of Unknown	
20.00 msec. (50 Hz Rejection)	L5
16.67 msec. (60 Hz Rejection)	L6
Case	
Plastic Case UL94V-0 RATED	P
Metal Case	M

(Connectors Optional See Fig. 17)

NEED APPLICATION HELP?

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APPLICATION DATA

PRINCIPLES OF OPERATION

The AN2577 utilizes an autozeroed, 3-phase dual-slope analog-to-digital converter which includes an input filter, a buffer stage, an integrator and a comparator. The input filter is optimized* and provides over-voltage protection with FET input clamp diodes. The input buffer is a voltage follower with a FET input stage which features high (gigaohm) input impedance and low (picoAmp) bias currents. A gain of 10 is provided in the buffer for the ±399.99mV full-scale option.

In each conversion cycle, the internal offset voltages are sensed and compensated for automatically (Autozero Phase). The displayed data is the digitized ratio of the input signal to the precision reference located in the instrument. Optionally, the user may introduce his own reference (scaled for +1 volt dc), where the output count of 10000 would represent an input equal to the full value of the external reference. (Display = V_{in}/V_{ref} x 10000).

A front panel-accessible span control permits the user to calibrate the precision internal reference to system standards. Analogic's precision reference is calibrated and traceable to NBS standards.

Signal return is separated from digital ground through the pulse transformer interface between the analog and digital circuits.

All timing and control functions are performed by a proprietary CMOS integrated circuit which drives the LED display in a multiplexed BCD format.

**Maximum filtering, while allowing a full-scale input step to settle to 1 count within 1 conversion period.*

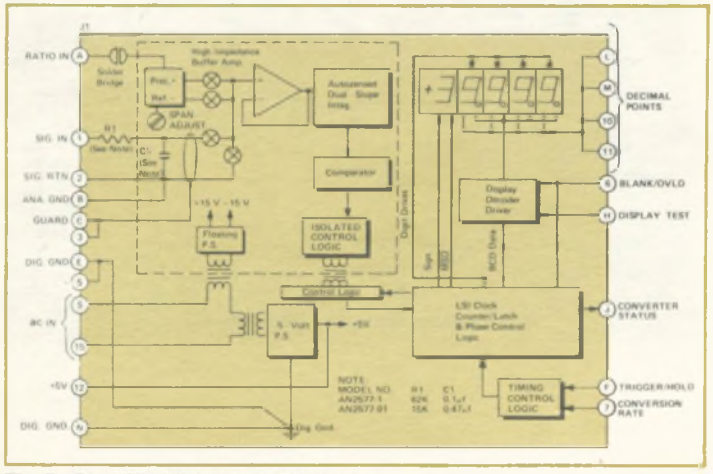
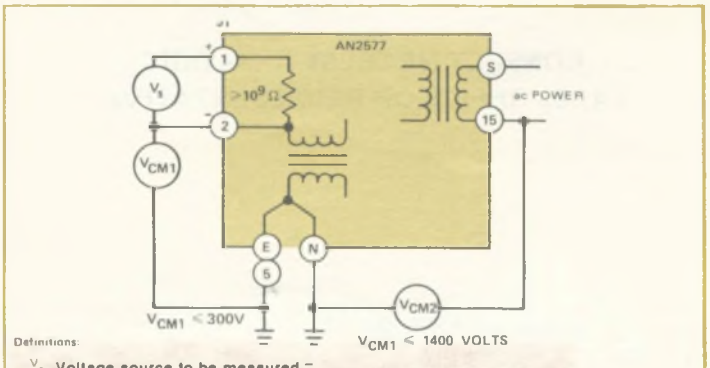


Fig. 2. Simplified Schematic Diagram.



Definitions:

V_s Voltage source to be measured.

V_{cm1} Common mode voltage between pins ② and Ⓔ. Typically this would be due to ground loops or other system noise. Note that only a differential input such as in the AN2577 can reject this type of noise and interference.

V_{cm2} Common mode voltage (isolation potential) between power line and digital ground.

Pin ① Positive input for voltage to be measured.

Pin ② Negative input (return) for voltage to be measured.

Pin Ⓝ Digital ground. Internally connected to analog ground via Kelvin connection. All digital signals such as Decimal Points, HOLD, BLANK, EOC, DISPLAY TEST, OVER-RANGE, BCD etc., should be returned to this point.

Fig. 3. Input Configurations and Common Mode Voltages.

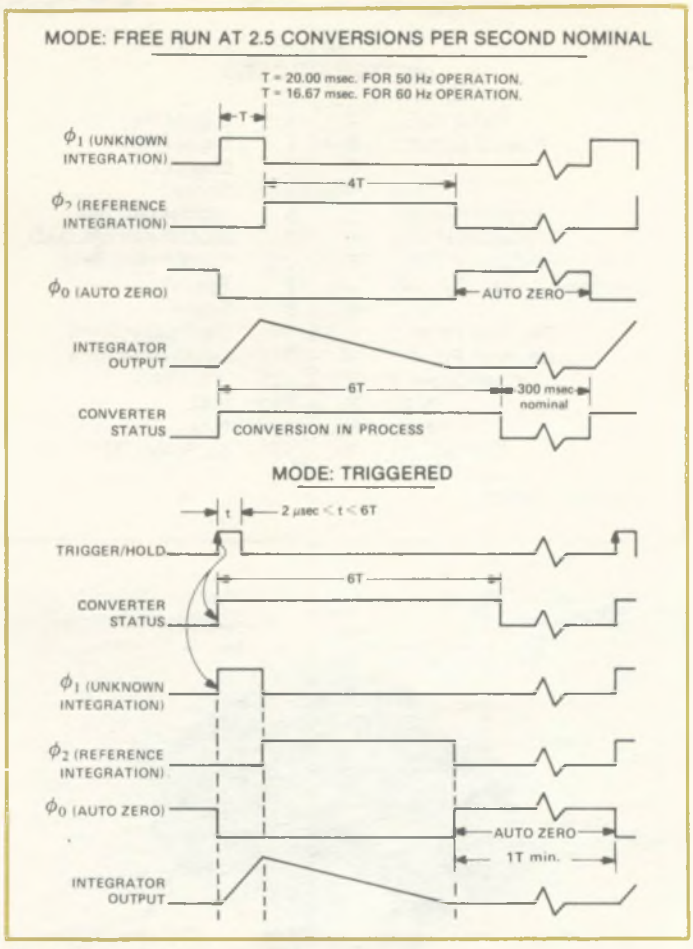
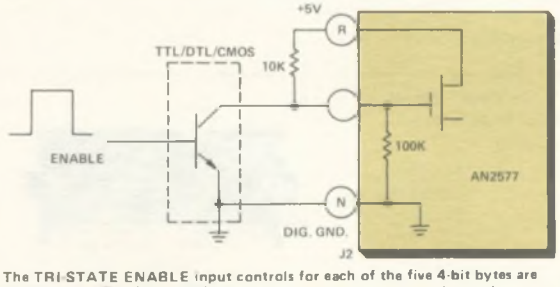


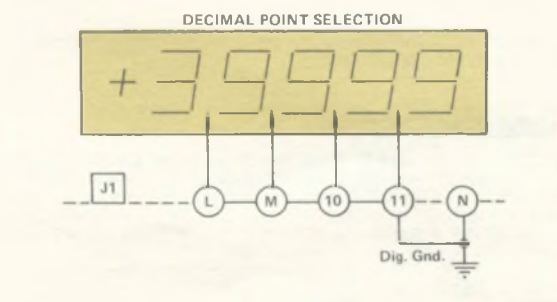
Fig. 4. Timing Diagram



The TRI-STATE ENABLE input controls for each of the five 4-bit bytes are CMOS compatible (0 to +5V). Multiple lines may be tied together and enabled simultaneously.

The BCD output is automatically enabled by an internal 100K ohm pull-down resistor and can be disabled by an external 10Kohm pull-up resistor, connected between the appropriate ENABLE input and J2 pin R (+5V) as shown. This allows data to be controlled by a mechanical switch, TTL, DTL or CMOS logic. (Note: External 10Kohm resistor not required for CMOS interface).

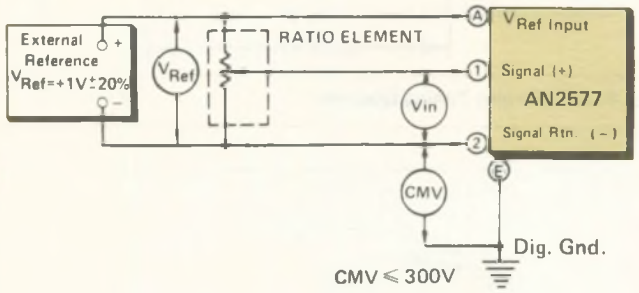
Fig. 5. Interfacing to BCD Enable Inputs.



To display the desired decimal point, simply connect the appropriate pin as shown to Digital Ground (J1, Pin N) using a jumper lead.

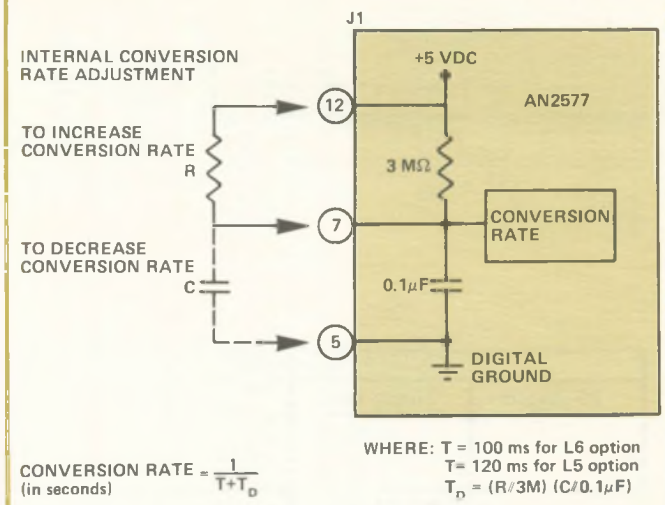
Fig. 6. Decimal Point Position Terminals.

APPLICATION DATA



NOTE: (Consult Factory for Ratiometric Option).
A voltage ratio measurement can eliminate the need for a costly precision power supply to provide transducer excitation. This is accomplished by the dual-slope integrating A/D converter which displays the digitized ratio of V_{in}/V_{ref} x 10000. Thus, if the external reference varies, the signal voltage will change proportionally. This makes the long term accuracy of the external reference supply noncritical and it need only be stable during the measurement period.

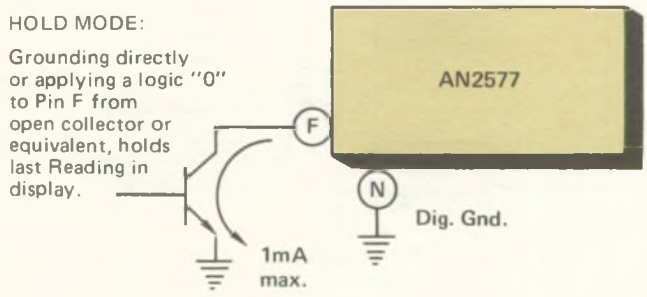
Fig. 10. Using AN2577 for 3-Wire Ratiometric Measurements.



CONVERSION RATE = $\frac{1}{T+T_D}$ (in seconds)

WHERE: T = 100 ms for L6 option
T= 120 ms for L5 option
T_D = (R//3M) (C//0.1μF)

Fig. 11. Conversion Rate Control.

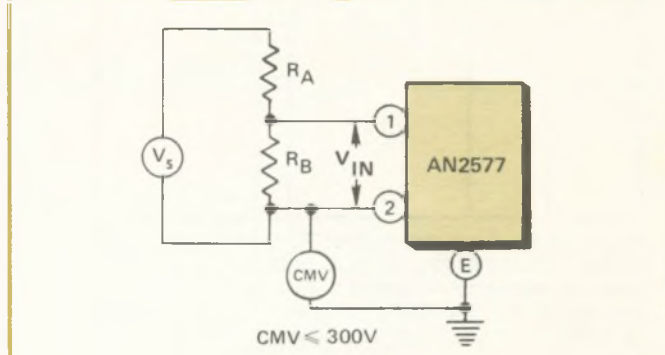


TRIGGER MODE:

- A new conversion can be initiated anytime the CONVERTER STATUS output (J1 pin J) is low. A positive trigger pulse, (logic "1" CMOS compatible, 0 to +5 Vdc) with a rise time of less than 200 nsec., will start a new conversion.

NOTE: A trigger pulse at any other time will be ignored by the converter and the conversion in process will continue until complete.

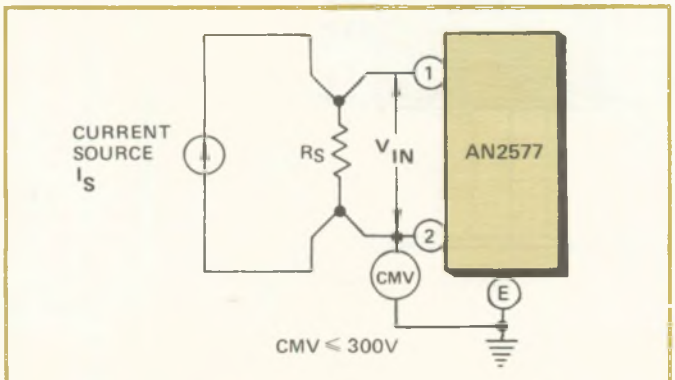
Fig. 12. TRIGGER/HOLD Control.



For signal voltages V_s greater than 4 Volts, select R_A and R_B for proper scaling such that V_{in} is ≤ 4 Volts for a "3.9999" Display.* Program Decimal Point accordingly (See Fig. 6).

*According to $V_{IN} = \left(\frac{R_B}{R_A + R_B}\right) \times V_s$

Fig. 13. Input Scaling.



Select shunt resistance R_S according to following:

$$R_S = \frac{\text{Desired Full Scale Count}}{\text{Full Scale Range of Input Current}} \times K$$

where

K = 0.0001 for 3.9999 V_{IN}

K = 0.00001 for 0.39999 V_{IN}

Fig. 14. Current Input.

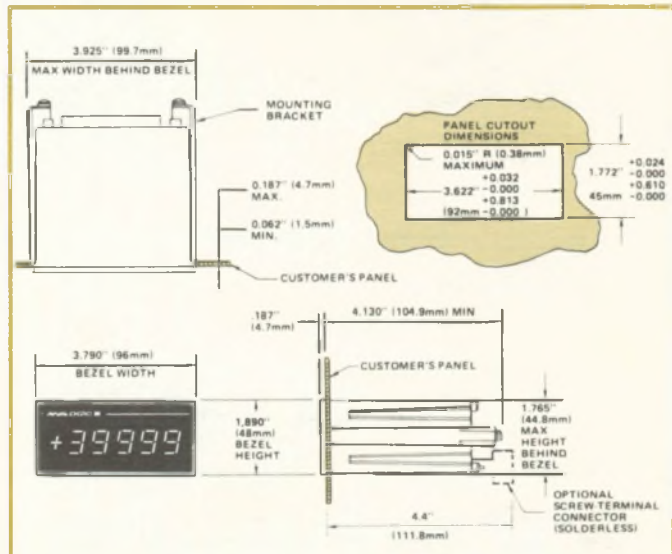
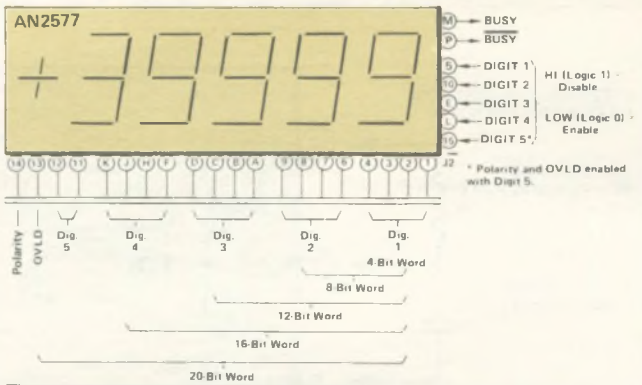


Fig. 15. Installation Dimensions.



Word Programming		
Bits/Word	Enable Pins	Digits Enabled
20	N/A	All Digits plus OVLD and Polarity
16 16	5 & 10 & E & L 15	1 & 2 & 3 & 4 5, OVLD, Polarity
12 12	5 & 10 & E L & 15	1 & 2 & 3 4 & 5, OVLD, Polarity
8 8 8	5 & 10 E & L 15	1 & 2 3 & 4 5, OVLD, Polarity
4 4 4 4 4	5 10 E L 15	1 2 3 4 5, OVLD, Polarity

When the word-programmable TRI-STATE BCD option is installed, 20-bits of latched and buffered parallel BCD outputs are available on connector J2 and are automatically enabled. BUSY and BUSY indicate when data is valid. The same BCD option can be used when the AN2577 must interface with a data bus structure which requires data in 4, 8, 12, 16 or 20 bit bytes. This can be accomplished simply by jumpering the DIGIT ENABLE lines together, according to the word size (see chart). A high level (Logic 1) disables the BCD output.

Fig. 7. Word-Programming Tri-State BCD Output.

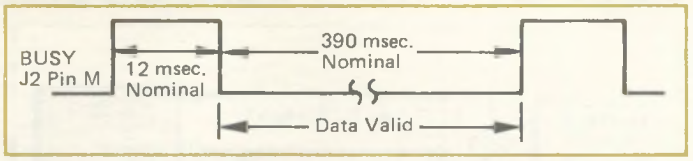
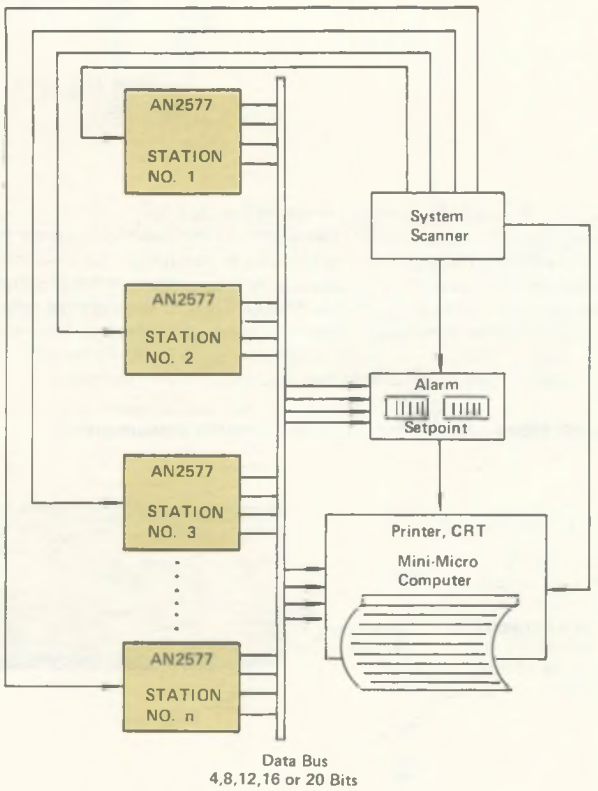
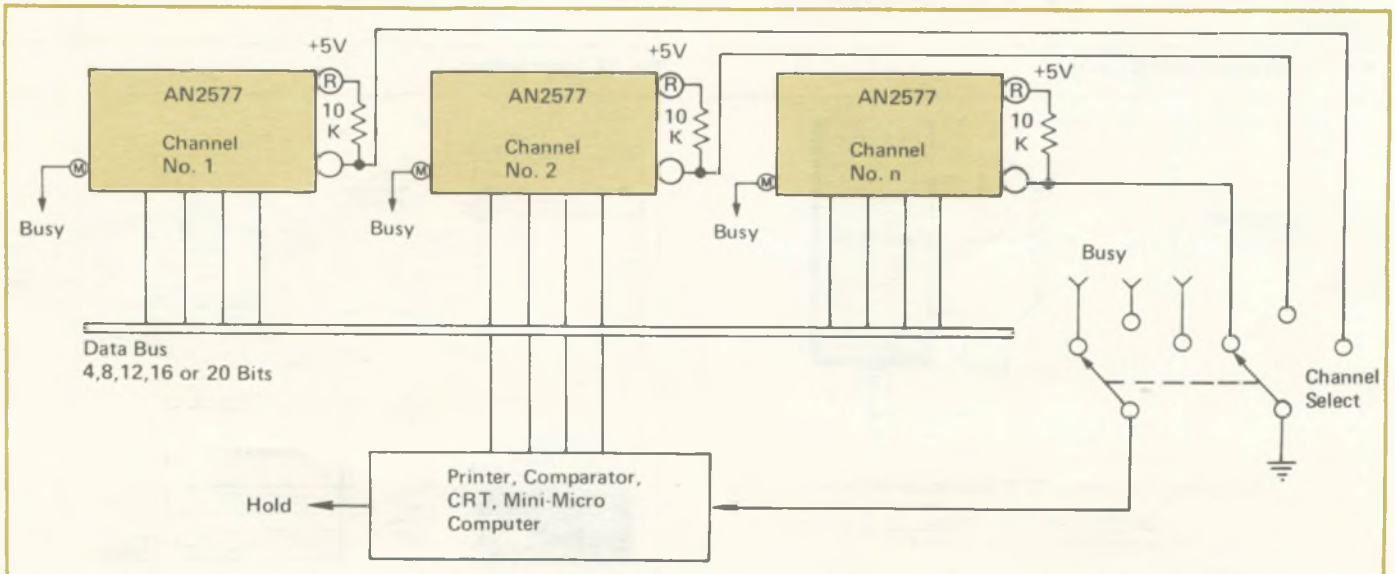


Fig. 8. BCD Output Timing Diagram.



The TRI-STATE BCD outputs of the AN2577 may be tied together into a common data bus and individually enabled for input to a single recording device, such as a printer, digital comparator, computer or other peripheral equipment. This eliminates costly external switching of multiple BCD lines and simplifies system interfacing.

Fig. 9a. Multiple Station Monitor.



The TRI-STATE BCD outputs of the AN2577 may be tied together into a common data bus and individually enabled for input to a single recording device, such as a printer, digital comparator, computer or other peripheral equipment. This eliminates costly external switching of multiple BCD lines and simplifies system interfacing.

Fig. 9b. Multiple Channel Data Acquisition.